

# Cisco Silicon One P100 Processor

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The silicon industry has always been plagued with the trichotomy of switching silicon, routing line card silicon, and routing fabric silicon. Using these three basic building blocks, silicon and system vendors created unique architectures tuned for individual markets and industries. Consequentially, forcing customers to consume and manage these disjointed and dissimilar products caused an explosion in complexity, CapEx, and OpEx for the industry.

The Cisco Silicon One™ architecture ushers in a new era of networking, enabling one silicon architecture to address a broad market space, while simultaneously providing best-of-breed devices.

At 19.2 Tbps, the Cisco Silicon One P100 builds on the ground-breaking technology of the Cisco Silicon One devices before it, while increasing the lead over all other routing silicon in the market. The P100 is one of the highest bandwidth, highest performance, most flexible, and most power-efficient routing silicon on the market.

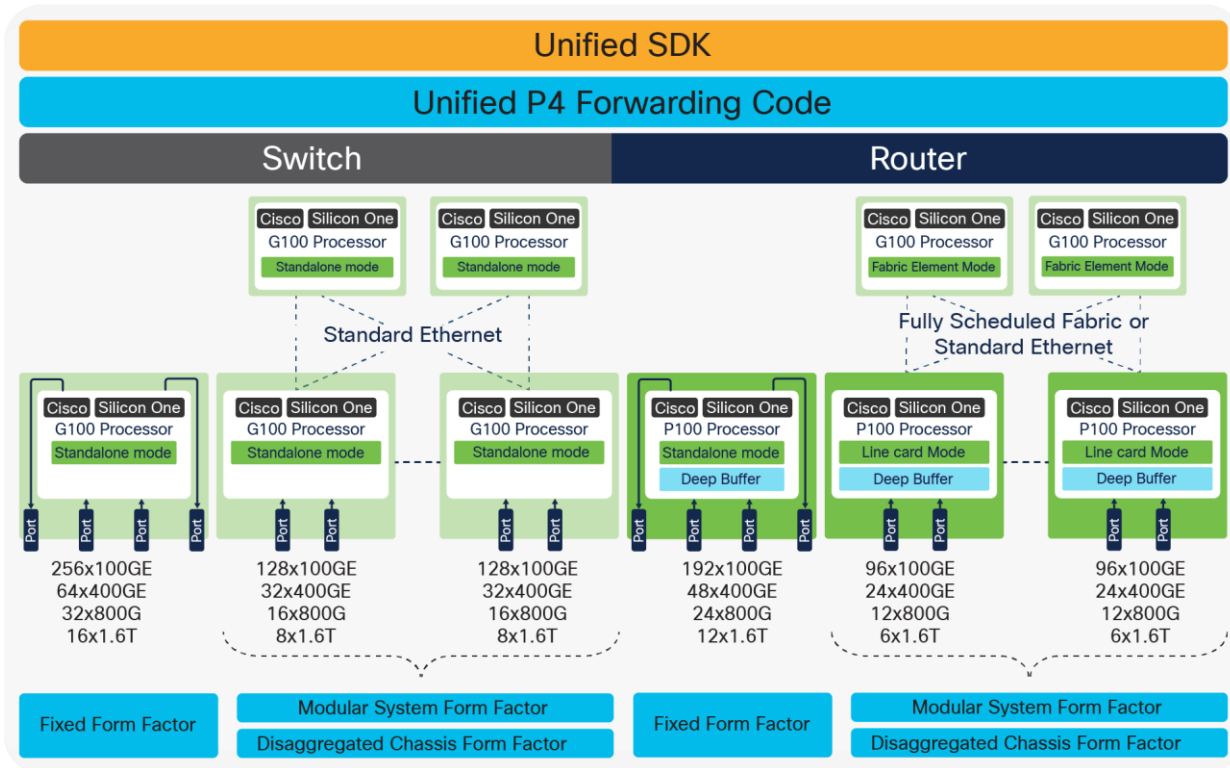
## Product overview

The Cisco Silicon One P100 processor is a 19.2-Tbps processor that can be configured as:

- 19.2-Tbps, full-duplex, standalone routing processor with deep buffers
- 9.6-Tbps, full-duplex line card routing processor with deep buffers

Using a single P100 device in a fixed box enables a true 19.2-Tbps, 24x800G system, while using just three P100 devices on a line card enables a true 28.8-Tbps, 36x800G line card.

Cisco Silicon One P100 and G100 can be used together to build a wide range of products covering fixed form factor routers and switches, modular chassis routers and switches, and multipetabit disaggregated routers and switches.



**Figure 1.**  
Form factors

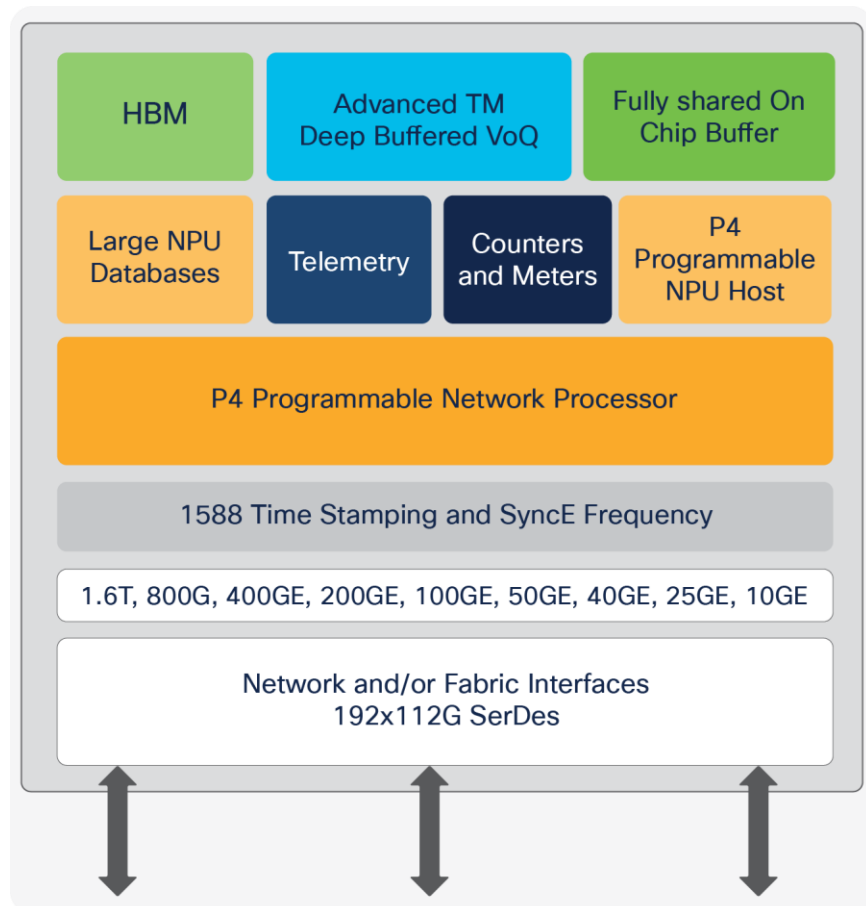
## Features and benefits

**Table 1.** Architectural characteristics and benefits

Feature	Benefit
<b>Unified architecture across multiple markets</b>	Greatly simplifies customer network infrastructure deployments
<b>Unified SDK across market segments and applications</b>	Provides a consistent point of integration for all applications across the entire network infrastructure
<b>High-bandwidth routing silicon</b>	7-nm, 19.2-Tbps routing silicon
<b>High-performance routing silicon</b>	Achieve line rate at small packet sizes
<b>Power-efficient routing silicon</b>	The power efficiency of 7 nm and the Cisco Silicon One architecture
<b>Large and fully unified packet buffer</b>	Fully shared on-die buffer with large external packet buffer
<b>Switching efficiency with routing features and scale</b>	Addresses the requirements of service provider and web-scale providers' routing applications
<b>Run-to-completion network processor</b>	Provides feature flexibility without compromising performance or power efficiency
<b>Programmable</b>	A programming processor to allow for rapid feature development

## Prominent feature

### Flexibility, performance, and scale for next-generation service provider and web-scale networks



**Figure 2.**  
Block diagram

### Features

- 192 112G SerDes; each can be configured independently to operate in 10G/25G/50G/100G using NRZ or PAM4 modulation
- Flexible port configuration supporting 10/25/40/50/100/200/400/800/1600 Gbps
- Large, fully shared, on-die packet buffer
- Large, in-package packet buffer
- 1588v2 and SyncE support with nanosecond-level accuracy
- On-chip, high-performance, programmable host NPU for high-bandwidth offline packet processing (for example, OAM processing, MAC learning)
- Multiple embedded processors for CPU offloading

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## Traffic management

- Large pool of configurable queues, supporting DiffServ and hierarchical QoS
- Support for system-level, end-to-end QoS and scheduling for both unicast and multicast traffic
- Seamless extension of on-die buffer to external packet buffer
- Support for ingress and egress traffic mirroring
- Support for link-level (IEEE802.3x), PFC priority-level (802.1Qbb) flow control and ECN marking
- Support of port extenders

## Network processor

- Run-to-completion, distributed programmable network processor
- Line rate at very small packets even with complex packet processing
- Large and shared fungible tables
- Support for complex packet processing features without impacting data rate
- Support for simple packet processing features with optimized power and latency

## Load balancing

- Flow load balancing using ECMP or LAG
- Dynamic flowlet load balancing with ability to detect and handle elephant flows
- Packet-by-packet load balancing, creating an optimal, flow-independent, end-to-end scheduled and lossless fabric

## Instrumentation and telemetry

- Programmable meters used for traffic policing and coloring
- Programmable counters used for flow statistics and OAM loss measurements
- Programmable counters used for port utilization, microburst detection, delay measurements, flow tracking, elephant flow detection, and congestion tracking
- Traffic mirroring: (ER)SPAN on drop
- Support for sFlow and NetFlow
- Support for in-band telemetry

## SDK

- APIs provided in both C++ and Python
- SAI and SONiC support
- Configurability via high-level networking objects
- Distribution-independent Linux packaging
- Robust simulation environment enables rapid feature development

## P4 programmability

- Application development is handled by an IDE programming environment
- At compilation, the application generates low-level register/memory access APIs and higher-level SDK application APIs
- Provides application support for a wide range of data center, service provider, and enterprise protocols
- Ability to develop the SDK and applications running over the SDK over a simulated Cisco Silicon One device

## Cisco P4 application

Due to Silicon One's extensible programming toolkit, we are always adding features to address new markets and new customer requirements; however, a sample of the features that are currently available with the application code is provided below:

<ul style="list-style-type: none"><li>• IPv4/v6 Routing<ul style="list-style-type: none"><li>◦ OSPF</li><li>◦ IS-IS</li><li>◦ BGP</li><li>◦ Unicast RPF</li></ul></li><li>• MPLS Forwarding<ul style="list-style-type: none"><li>◦ LDP, LDPoTE</li><li>◦ RSVP-TE</li><li>◦ SR-MPLS</li><li>◦ SR-TE</li><li>◦ L3VPN, 6PE, 6VPE</li><li>◦ BGP LU</li><li>◦ VPWS/EoMPLS</li><li>◦ VPLS</li></ul></li><li>• Ethernet Switching<ul style="list-style-type: none"><li>◦ 802.1d, 802.1p, 802.1q, 802.1ad</li><li>◦ Private VLANs</li><li>◦ VLAN translation</li><li>◦ Hardware-assisted MAC learning</li></ul></li><li>• 802.1x Network access control</li><li>• IP Tunneling<ul style="list-style-type: none"><li>◦ IPinIP</li><li>◦ GRE</li><li>◦ VXLAN</li><li>◦ SRv6</li><li>◦ EVPN</li></ul></li><li>• Integrated Routing and Bridging (IRB)</li><li>• HSRP/RRRP</li><li>• Policy-Based Routing</li><li>Security and QoS ACLs<ul style="list-style-type: none"><li>◦ User-defined Keys</li><li>◦ Object groups</li></ul></li></ul>	<ul style="list-style-type: none"><li>• ECMP and LAG (802.3ad)</li><li>• Multicast<ul style="list-style-type: none"><li>◦ PIM-SM/SSM</li><li>◦ IGMP</li><li>◦ MLDP</li><li>◦ MVPN</li></ul></li><li>• NAT/PAT</li><li>• Protection (Link/Node/Path and TI-LFA)</li><li>• QoS Classification and Marking</li><li>• Congestion Management<ul style="list-style-type: none"><li>◦ WRED</li><li>◦ ECN</li><li>◦ Priority Flow Control</li></ul></li><li>• Hierarchical scheduling</li><li>• Telemetry<ul style="list-style-type: none"><li>◦ NetFlow, sFlow</li><li>◦ (ER)SPAN</li><li>◦ Packet Mirroring with Appended Metadata</li><li>◦ Lawful Intercept</li></ul></li><li>• DDoS Mitigation<ul style="list-style-type: none"><li>◦ Control-Plane Policing</li><li>◦ BGP Flowspec</li></ul></li><li>• Hardware offload<ul style="list-style-type: none"><li>◦ BFD</li><li>◦ CFM</li><li>◦ SAT</li></ul></li><li>• Timing and Frequency Synchronization<ul style="list-style-type: none"><li>◦ SyncE</li><li>◦ 1588</li></ul></li></ul>
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## Product sustainability

Information about Cisco's environmental, social, and governance (ESG) initiatives and performance is provided in Cisco's CSR and sustainability [reporting](#).

**Table 2.** Cisco environmental sustainability information

Sustainability topic		Reference
General	Information on product-material-content laws and regulations	<a href="#">Materials</a>
	Information on electronic waste laws and regulations, including our products, batteries, and packaging	<a href="#">WEEE Compliance</a>
	Information on product takeback and reuse program	<a href="#">Cisco Takeback and Reuse Program</a>
	Sustainability inquiries	Contact: <a href="mailto:csr_inquiries@cisco.com">csr_inquiries@cisco.com</a>
Material	Product packaging weight and materials	Contact: <a href="mailto:environment@cisco.com">environment@cisco.com</a>

## For more information

[Learn more](#) about the Cisco Silicon One.

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