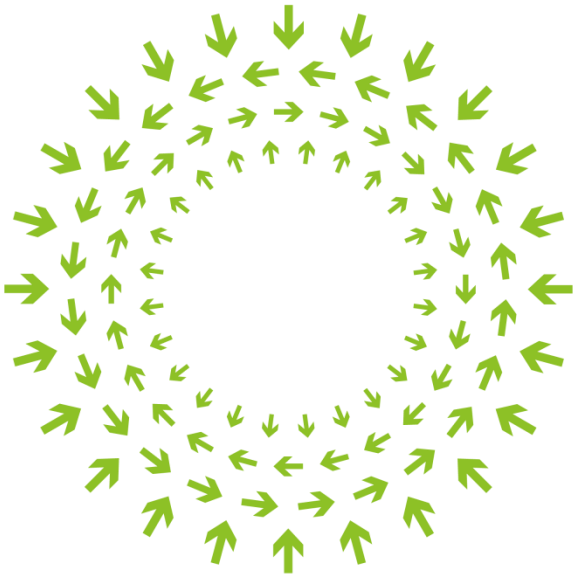

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Compute Project

Facebook Minipack 128x 100GE Switch System Specification

Rev 1.0

02/10/2019

1 Revision History

Date	Revision	Changed by	Description
02/10/2019	1.0	Xu Wang Jimmy Leung Rongchun Zhou Lingjun Wu	Initial OCP release

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3 Scope

This document outlines the technical specifications of the Facebook Minipack 128x 100GE Open Switch Platform submitted to the Open Compute Foundation. Minipack is Facebook's 4RU compact modular switch, and it can be used in multiple tiers of Facebook's data center networks. This document also introduces Minipack's software accessible interfaces, and required software actions to properly manage the hardware at the system level.

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7 Introduction

7.1 System Overview

Minipack is Facebook's next generation compact datacenter modular switching platform. The main attributes are:

- Chassis Size
  - 176mm (H) x 440mm (W) x 737mm (D)
  - 4RU
  - Designed to mount in EIA 19" rack
- Port Interface Module(PIM)
  - PIM-16Q: 16 x QSFP28 16 x 100G port interface module
  - PIM-4DD: 4 x QSFP-DD 4 x 400G port interface module
  - More options can be supported, such as DWDM transponder, MACsec PHY, etc.
- Switch Main Board(SMB)
  - Switch Main Board which has Tomahawk3 (TH3) switch ASIC
- Control plane and SCM
  - Intel Broadwell-DE CPU
  - Industry-standard COM-Express (COM-e) CPU module form-factor
  - System Control Module(SCM) carries one COM-e module.
- Data plane switch ASIC
  - Broadcom BCM56980 a.k.a Tomahawk3, 12.8Tbps
- Management plane
  - Aspeed AST2520 BMC chip
  - OOB GbE Switch for COM-e and BMC inside Minipack Chassis
  - Front panel RS232 console to BMC
  - USB debug port that supports Facebook OCP debug dongle
    - UART to CPU or BMC
    - I2C to BMC
- Power Plane
  - 2+2 redundant AC/DC PSU
  - 90VAC to 400VAC input (180VAC minimum required for full PSU output power)
  - 12V output

The following table lists the key attributes of Minipack system.

Attributes	Quantity	Notes
Port Interface Module	8	8 PIM in one Minipack chassis

SerDes Links	256	256 x 50G PAM4
Total number of Serdes Link per PIM	32	32 x 50G PAM4 per PIM, equivalent to 16 x 100G, or 4 x 400G
Total number of PCIe Link for Tomahawk3	4	PCIe Gen-3 x4 for Tomahawk3 ASIC
Total number of PCIe Link for NVMe SSD	4	PCIe Gen-3 x4 reserved for NVMe SSD
Total number of PCIe Link for IOB FPGA	1	PCIe Gen-1 x1 for IOB FPGA
Total number of PCIe Link for PIM	0	No PCIe bus to PIM
Link Speed	53.125Gbps	SerDes between TH3 and PIM
Total number of QSFP28 ports	128	128 QSFP28 100G ports, each PIM-16Q has 16 QSFP28 100G ports
Total number of QSFP-DD ports	32	32 QSFP-DD 400G ports, each PIM-4DD has 4 QSFP-DD 400G ports

Table 1: Minipack System Parameters

7.2 Common Terms

The following terms are used in Minipack project:

- 100GE – 100 Gigabit Ethernet
- 200GE – 200 Gigabit Ethernet
- 400GE – 400 Gigabit Ethernet
- Tomahawk3 – Broadcom BCM56980 12.8T switch ASIC
- SMB – Switch Main Board
- SCM – System Controller Module
- PIM – Port Interface Module
    - PIM-16Q – 16 QSFP28 100G Port Interface Module
    - PIM-4DD – 4 QSFP-DD 400G Port Interface Module
- FCM – Fan Control Module
    - FCM-T – FCM Top
    - FCM-B – FCM Bottom
- PDB –Power Distribution board
    - PDB-R – Power Distribution board Right

    - PDB-L – Power Distribution board Left
    - PDB-H – Power Distribution board Horizontal
- COM-e – COM-Express CPU module
- BMC – Baseboard Management Controller
- PSU – Power Supply Unit, Converts AC line voltage to DC 12V
- QSFP28 –Quad Small Form-factor Pluggable (QSFP) at 4 x 28Gbps, used for 100GBE
- QSFP56 –Quad Small Form-factor Pluggable (QSFP) at 4 x 56Gbps, used for 200GBE
- QSFP-DD –Quad Small Form-factor Pluggable Double Density at 8 x 56Gbps, used for 400GBE

7.3 Chassis

Minipack is a 4-RU modular switch that fits an EIA 19" rack.

- 176mm(H) x 440mm(W) x 738mm(D)

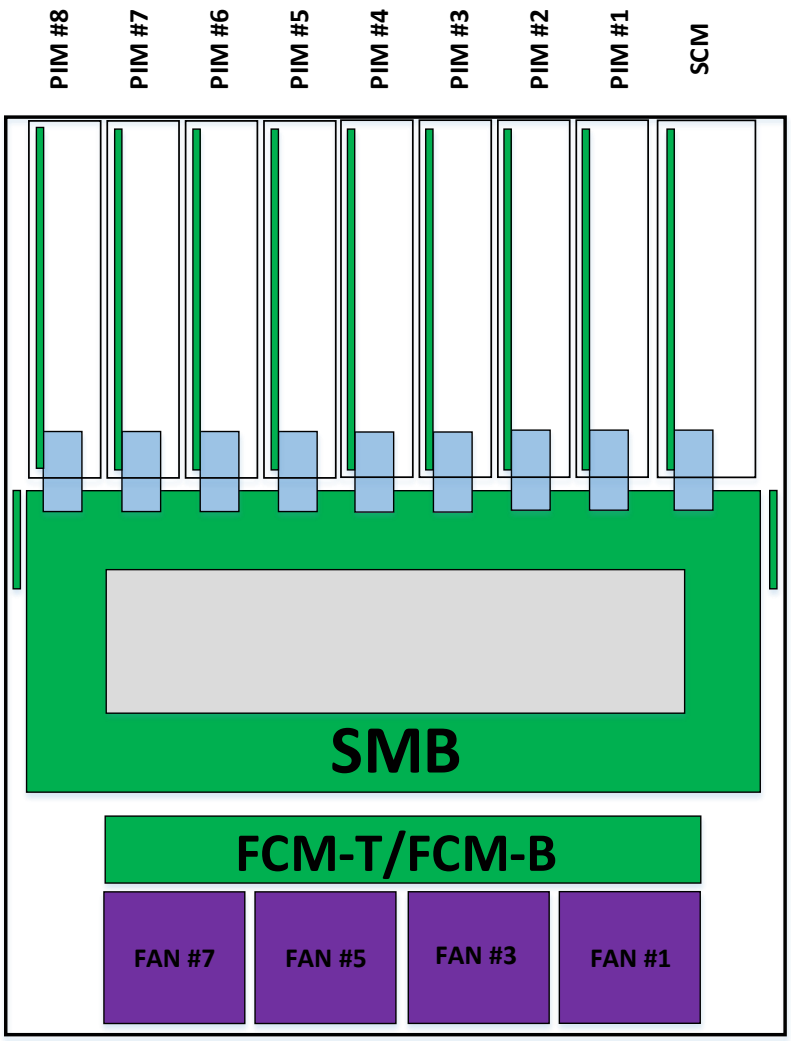


Figure 7-1: Minipack System Top View

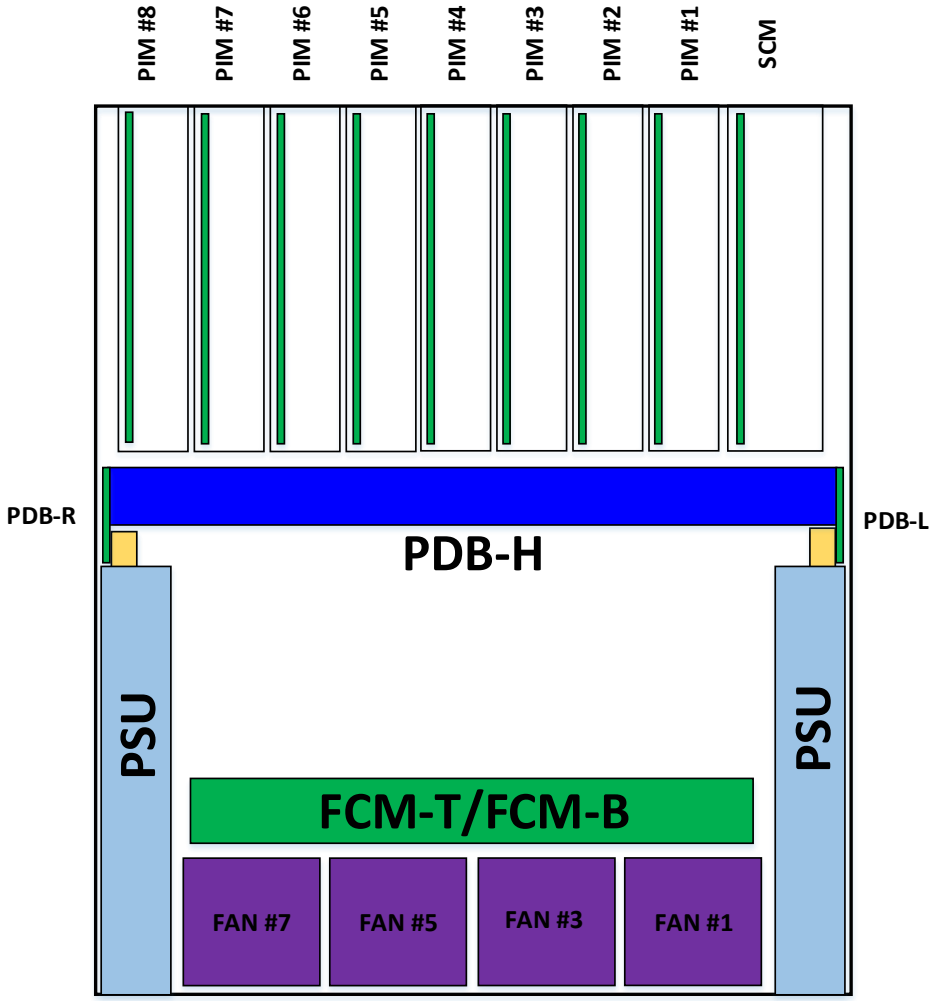


Figure 7-2: Minipack Top View w/o SMB

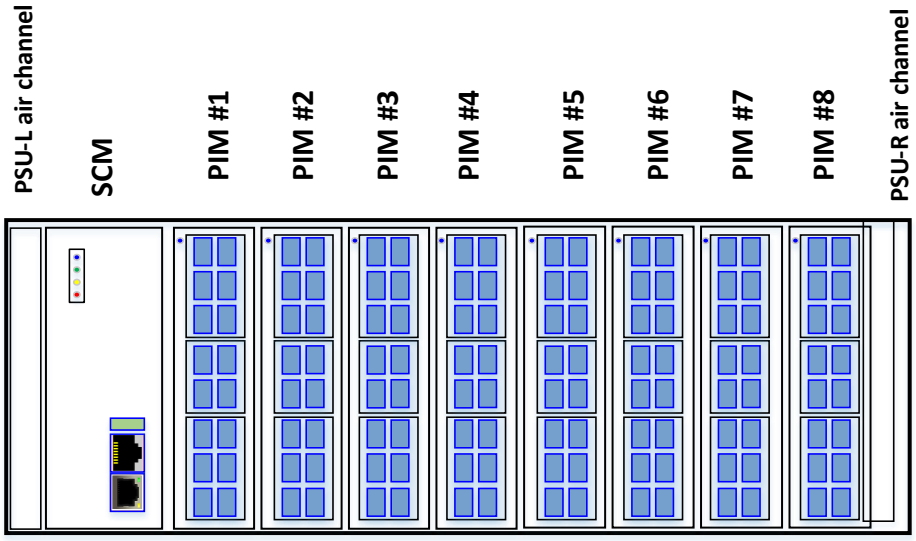


Figure 7-3: Minipack Front View

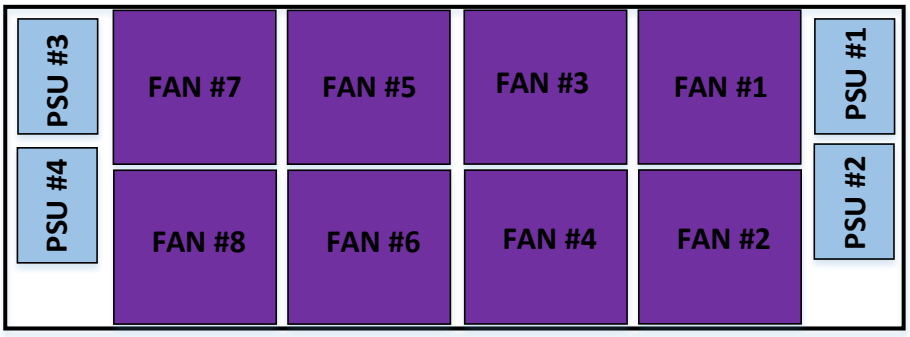


Figure 7-4: Minipack Rear View With Fan-tray

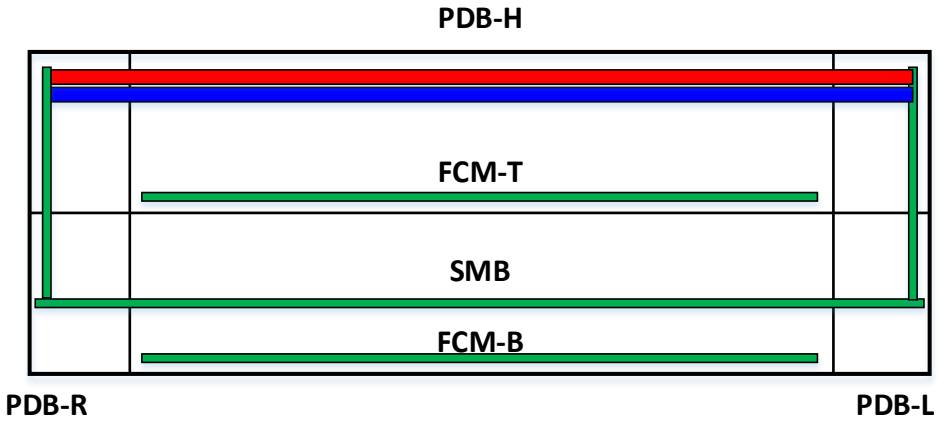


Figure 7-5: Minipack Rear View without Fan-tray

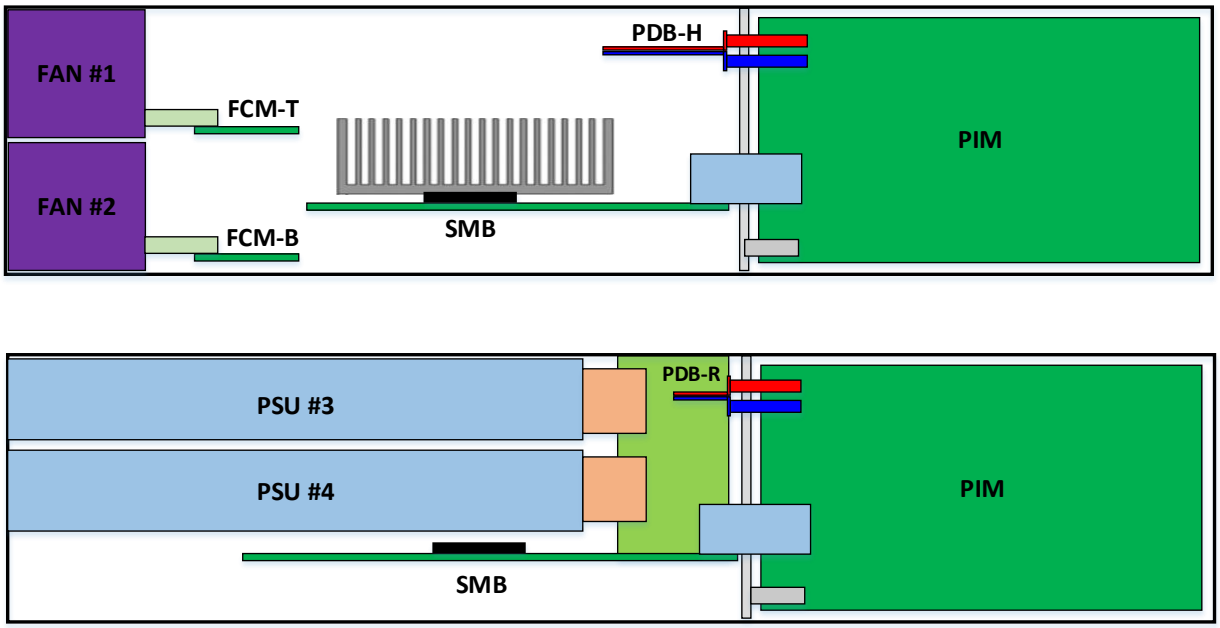


Figure 7-6: Minipack Side View

8 System Components

Minipack chassis has the following components:

- Switch Main Board (SMB)
- System Controller Module (SCM)
- Port Interface Module (PIM)
  - 16 x QSFP28 Port Interface Module (PIM-16Q)
  - 4 x QSFP-DD Port Interface Module (PIM-4DD)
- Fan Control Module (FCM)
  - Fan Control Module Top (FCM-T)
  - Fan Control Module Bottom (FCM-B)
- Power Distribution Board (PDB)
  - Power Distribution Board Right (PDB-R)
  - Power Distribution Board Left (PDB-L)
  - Power Distribution Board Horizontal (PDB-H)
- Power Supply Unit (PSU)
  - BelPower: PFE1500-12-054NAC (Further customization is required to support 277V AC line)
  - 2nd source PSU (TBD)
- Fan Tray (FAN)
  - 80mm x 80mm x80mm Fan tray FRU

The Port Interface Module (PIM) and System Controller Module(SCM) plug into the front side of the chassis. The Power Supply Unit (PSU) and Fan Tray plug into the rear side of the chassis.

FRU Type	Name	Quantity
Port Interface Module	PIM	8
System Control Module	SCM	1
PSU	PSU	4
FAN Module	FAN	8

Table 2: FRU List

8.1 System Hardware Architecture

Minipack is a single switch ASIC modular system, it only has one 12.8T Tomahawk3 switch ASIC, with 8 PIM(port interface module), one System Control Module(SCM). It is powered by four PSU, which are load sharing; and has eight 80mm x 80mm x 80mm CR fan tray to cool the system. The following diagram shows the logic architecture of Minipack switch:

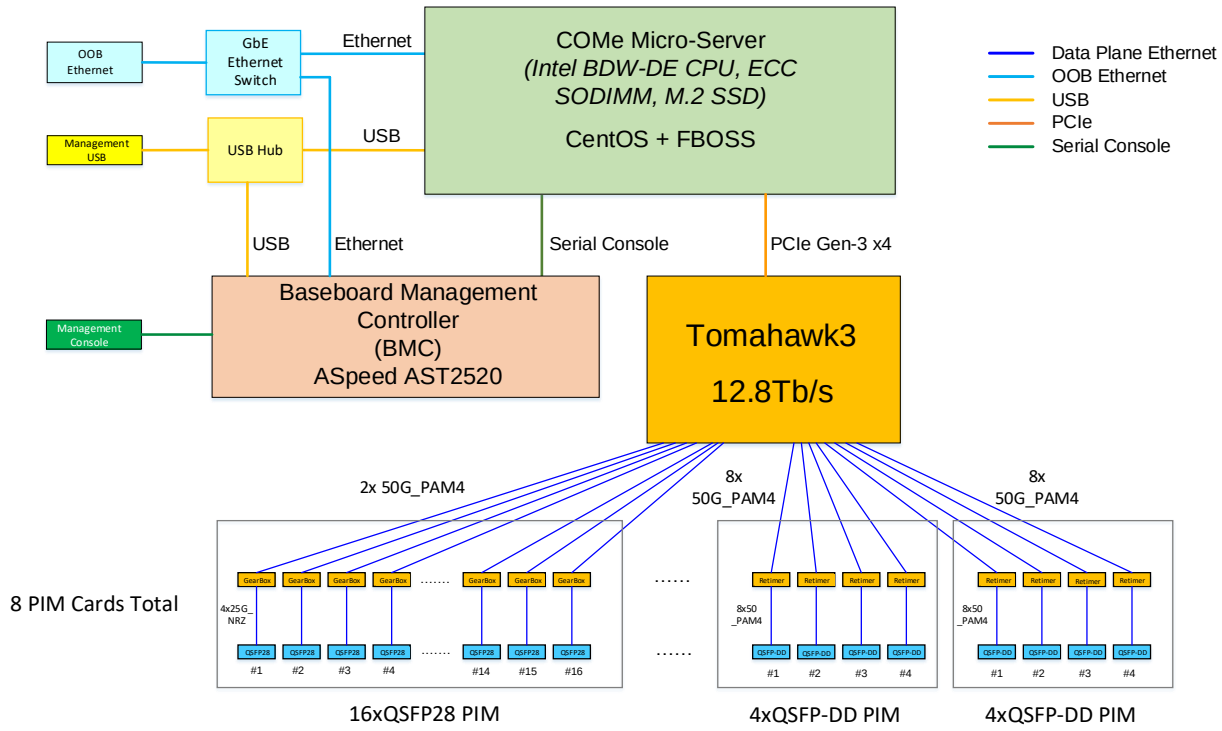


Figure 8-1: System Architecture of Minipack

The port interface module(PIM) provide network interface connectivity for Minipack. Two type of PIM are defined for Minipack:

- PIM-16Q: 16 x 100G QSFP28 Port Interface Module
- PIM-4DD: 4 x 400G QSFP-DD port interface module

More type of PIM can be introduced later if needed, such as DWDM, MACSEC, 8 x QSFP56 200G. etc.

The System Control Module(SCM) carries one COM-e Broadwell-DE CPU module, and can be plugged into front panel of the chassis. The Broadwell-DE CPU module provides the control function of Minipack.

Switch Main Board(SMB) is fixed to the chassis, it consists of Tomahawk3 switch ASIC, BMC system, and orthogonal interface to eight PIM and SCM. The Tomahawk3 switch ASIC is controlled by Broadwell-DE CPU of SCM through PCIe Gen-3 interface.

8.2 Switch Main Board (SMB)

Switch Main Board has two major function blocks:

1. Data plane function with 12.8T Tomahawk3 Switch ASIC
2. Management plane function with BMC AST2520 system

Tomahawk3 switch ASIC is controlled by BW-DE CPU at SCM through PCIe Gen-3 interface. SCM also provides secondary PCIe interface for PIM DOM FPGA control, the secondary PCIe bus need one PCIe switch to split this PCIe bus from SCM into 8 separate PCIe interface to eight PIM. The PCIe switch chip PEX8717 or equivalent chip is recommended.

SMB also provides USB to CP2112 control function for SCM CPU to access slave I2C bus on PIM.

8.2.1 Block Diagram of SMB

The following diagram shows the functional blocks of Switch Main Board(SMB).

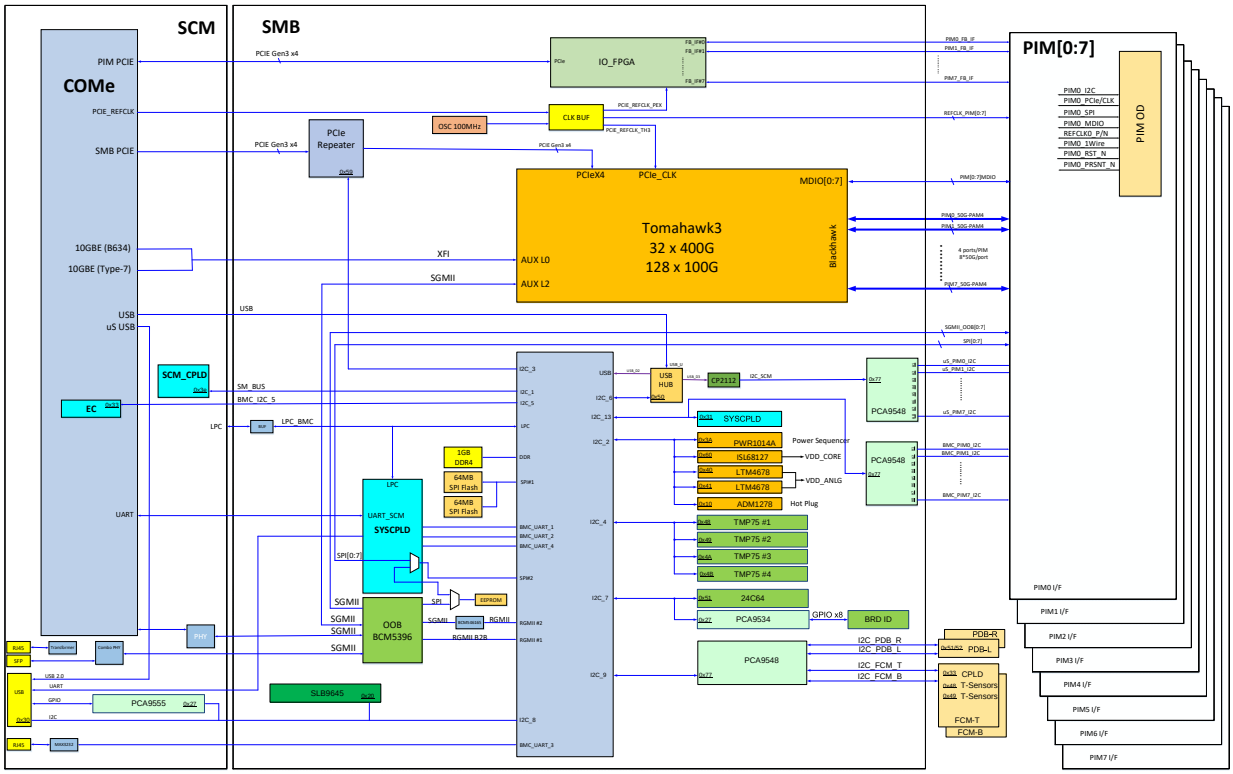


Figure 8-2: Switch Main Board Architecture

8.2.2 SMB components

SMB has the following components:

- 12.8T Tomahawk3 switch ASIC
- 64 pairs of 50G PAM4 TX and RX signals of Tomahawk3 ASIC connect to each PIM card, totally eight PIM cards are supported in Minipack system
- BMC AST2520 is used for Baseboard Management Controller.
- A 16 port SGMII GBE Switch BCM5396 is used for OOB switch to connect to SCM Front port, BMC, SCM-COM-e and Tomahawk3 Management port(configured as SGMII). And 8 ports of BCM5396 are reserved for PIM
- IOB (IO Bridge) FPGA is used to bridge CPU and PIM. IOB FPGA is a PCIe Gen-1 device of COM-e CPU, and it interfaces with eight DOM FPGA on PIM card via PIM_FB_IF bus. PIM_FB_IF is Facebook proprietary highspeed control interface to allow IOB FPGA to access DOM FPGA, gearbox, and QSFP28 optic module on PIM card. More details of

PIM_FB_IF are described in the IOB and DOM FPGA functional descriptions at 9.10 and 9.11.

- PCIe target function, MDIO access function, and QSFP28 control and status function.
- Multiple temperature sensors:
  - Front-Left
  - Front-right
  - Front-middle
  - Rear-left
  - Rear-right
- EEPROM for inventory information of Minipack chassis

8.2.3 SMB I2C Connections

The Switch Main Board I2C diagram shows the I2C architecture of Switch Main Board(SMB).

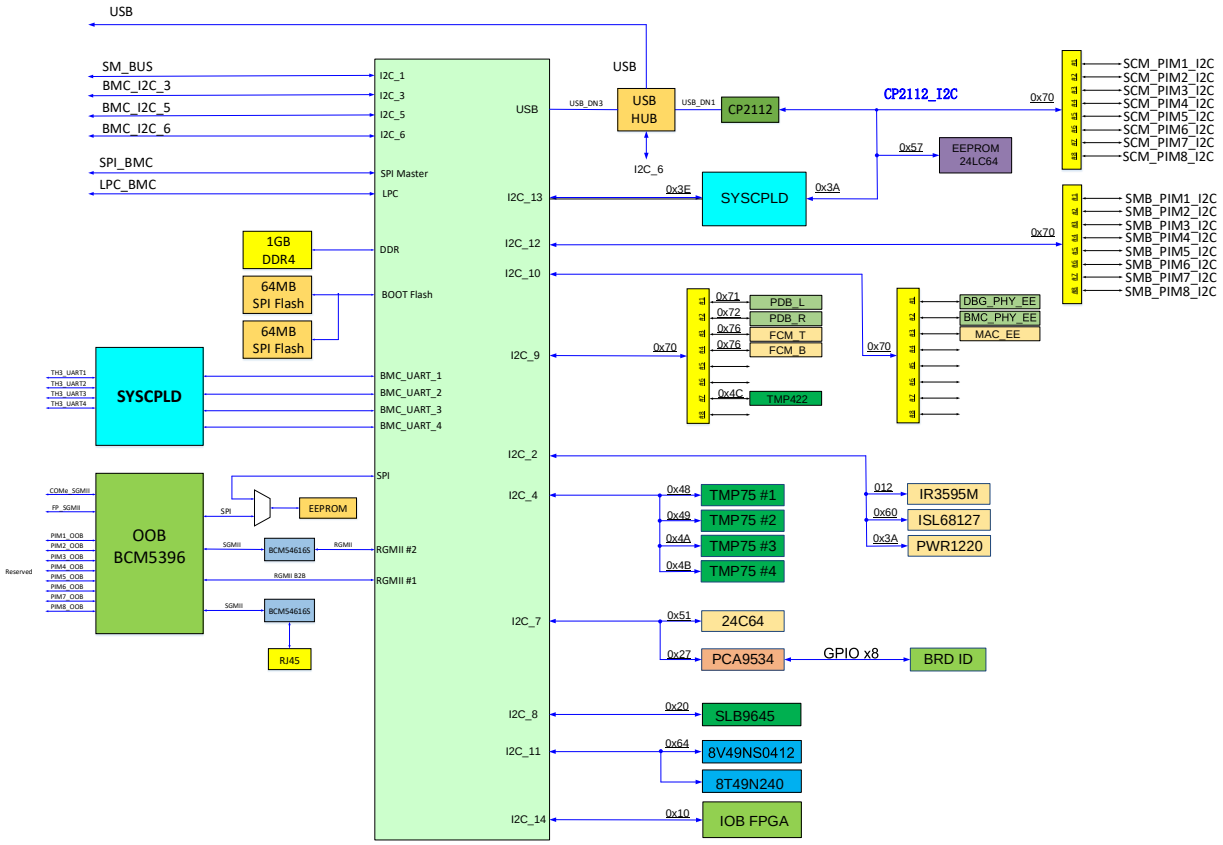


Figure 8-3: I2C Diagram of SMB

I2C Controller	I2C Address	I2C Device	
BMC_I2C_1	0x3E	SCM_CPLD	SCM Communication I2C Channel #1
BMC_I2C_2	0x3A	PWR1220	Power sequencer
	0x60	ISL68127	TH3 core voltage
	0x12	IR3595M	TH3 Analog voltage
BMC_I2C_3	0x59	PCIe Repeater	SCM PCIe interface repeater I2C ctrl channel
BMC_I2C_4	0x48	TEMP75 #1	Temperature sensor #1
	0x49	TEMP75 #2	Temperature sensor #2
	0x4A	TEMP75 #3	Temperature sensor #3
	0x4B	TEMP75 #4	Temperature sensor #4
BMC_I2C_5	0x33	EC	Embedded Controller on COM-e (Bridge IC)
BMC_I2C_6			
BMC_I2C_7	0x27	PCA9534	Board ID register
	0x51	24LC64	EEPROM for SMB inventory content
BMC_I2C_8	0x20	TPM SLB9671	SLB9671 I2C TPM
BMC_I2C_9	0x70	PCA9548	CH0: PDB-L CH1: PDB-R CH2: FCM-T CH3: FCM-B CH4: reserved CH5: reserved CH6: TMP422 for TH3 diode temperature sensor CH7: reserved
BMC_I2C_10	0x70	PCA9548	CH0: DBG_PHY_EEPROM CH1: BMC_PHY_EEPROM CH2: MAC_EEPROM CH3: reserved CH4: reserved CH5: reserved CH6: reserved CH7: reserved
BMC_I2C_11	0x64	8V49NS0412	Clock generator
		8T49N240	Clock generator
BMC_I2C_12	0x70	PCA9548	CH0: SMB_PIM1_I2C CH1: SMB_PIM2_I2C CH2: SMB_PIM3_I2C CH3: SMB_PIM4_I2C CH4: SMB_PIM5_I2C CH5: SMB_PIM6_I2C CH6: SMB_PIM7_I2C CH7: SMB_PIM8_I2C
BMC_I2C_13	0x31	SYS CPLD	System CPLD I2C interface of BMC

BMC_I2C_14	0x32	IOB FPGA	IOB FPGA I2C interface of BMC

Table 3: BMC I2C Devices

8.2.4 TH3 Power / VR

It's recommended to use Intersil's 14-phase proposal (ISL68127, ISL6617, ISL99227) for TH3 core voltage, which is implemented in Broadcom's SVK design. Other proposals could also be considered if there is better performance/cost improvement.

8.3 PIM-16Q 16x 100G Port Interface Module

PIM-16Q module supports 16 x QSFP28 interfaces. It has four BCM81724 gearbox PHY to translate 2x 50G PAM4 100G signal from Tomahawk3 switch into 4x 25G NRZ QSFP28 100G interface (CAUI-4).

8.3.1 Block Diagram of PIM-16Q

Each PIM-16Q has the following components:

- 16 QSFP28 ports, each QSFP28 port can support 3.5W 100G optic transceiver.
- 4 BCM81724 Gearbox chips. Each BCM81724 can support 8x 50G PAM4 to 16x 25G NRZ gearbox function
- 64 pairs of 50G PAM4 TX and RX signals connect to Tomahawk3 ASIC on SMB
- PIM's DOM FPGA is used to support DOM polling function, MDIO access function, and QSFP28 control and status function.
- Two temperature sensors: front and rear
- EEPROM for inventory information of PIM-16Q
- Power is provided by PDB-H, and can be controlled by hot swap controller ADM1278.
- BMC SPI interface
- BMC I2C interface
- SCM-SMB CP2112 I2C interface

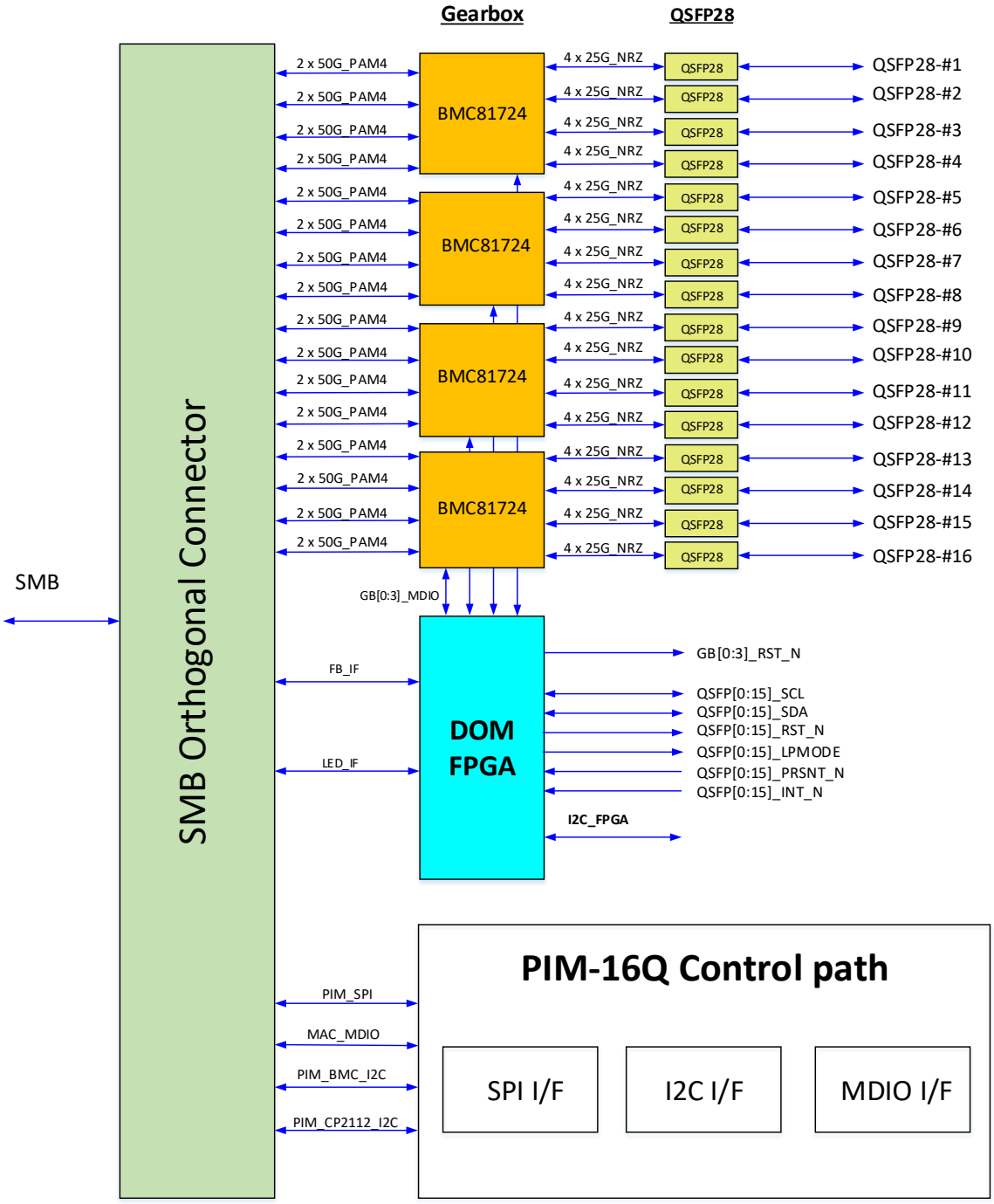


Figure 8-4: PIM-16Q Block Diagram

8.3.2 PIM-16Q QSFP28 Ports

The following diagram shows the front panel QSFP28 port numbering of PIM-16Q. each BlackHawk core support 4 x 100G, and each gearbox chip BCM81724 support 4 x 100G.

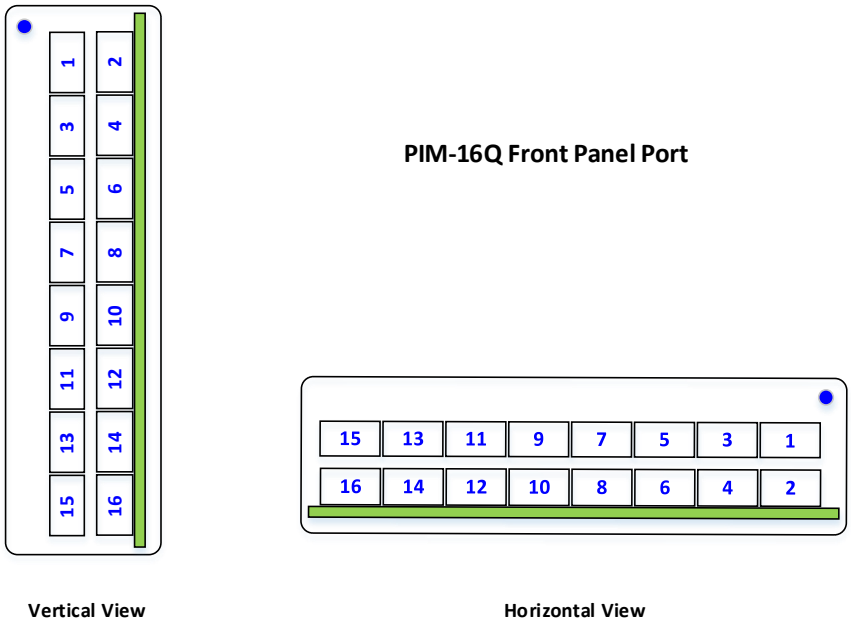


Figure 8-5: PIM-16Q QSFP28 Port Numbering

8.3.3 PIM-16Q QSFP28 Control

Each PIM-16Q has one dedicated FPGA to control QSFP28 interface. The FPGA can be accessed by both BMC and COM-e in order for software to control or check status of QSFP28 modules.

The following functions are supported by PIM FPGA:

- DOM polling function
- QSFP28 port LED control
- QSFP28 Reset Control(QSFP_RESET_N[16:1])
- QSFP28 LPMODE control(QSFP_LPMODE[16:1])
- QSFP28 Interrupt status(QSFP_INT_N[16:1])
- QSFP28 module present status(QSFP_ABS[16:1])

PIM-16Q control signals share the same 6x12 orthogonal direct connector to SMB, among those 72 differential pairs, 64 of them are used for data plane highspeed interface to Tomahawk3 switch ASIC, and the rest of 8 differential pair plus 12 single ended signals can be used for control purpose. The following table shows the control signal definition for PIM:

Signal Name	Inout	pin	Description
PIM_PCIE_TX_P	Out		PCIE Transmit from PIM to SMB
PIM_PCIE_TX_N	Out		PCIE Transmit from PIM to SMB
PIM_PCIE_RX_P	in		PCIE Receive from SMB to PIM
PIM_PCIE_RX_N	in		PCIE Receive from SMB to PIM
PIM_PCIE_CLK_P	In		PCIe clock input, positive
PIM_PCIE_CLK_N	in		PCIe clock input, negative
PIM_I2C_SCL	inout		PIM management I2C SCL
PIM_I2C_SDA	inout		PIM management I2C SDA
PIM_MDC	In		MDC from SMB
PIM_MDIO	inout		MDIO interface to Tomahawk3
PIM_SPI_CLK	In		SPI clock
PIM_SPI_CS	In		SPI Chip Select
PIM_SPI_DIN	In		SPI Data input
PIM_SPI_DOUT	Out		SPI data output
LED_CLK	In		LED clock from Tomahawk3
LED_DATA	In		LED data stream from Tomahawk3
SLOT_ID[3:0]	in		PIM Slot ID
PIM_PRSNT_N	Out		PIM present signal, tied to GND on PIM via 10 ohm resister
PIM_1WIRE_IN	In		PIM 1Wire reset input
PIM_INT_N	Out		PIM interrupt to SMB
PIM_UPDATE	IN		PIM FPGA upgrade indication from SMB

Table 4: Signals between PIM and SMB

8.3.4 PIM-16Q I2C Diagram

The I2C diagram of PIM-16Q is shown below.

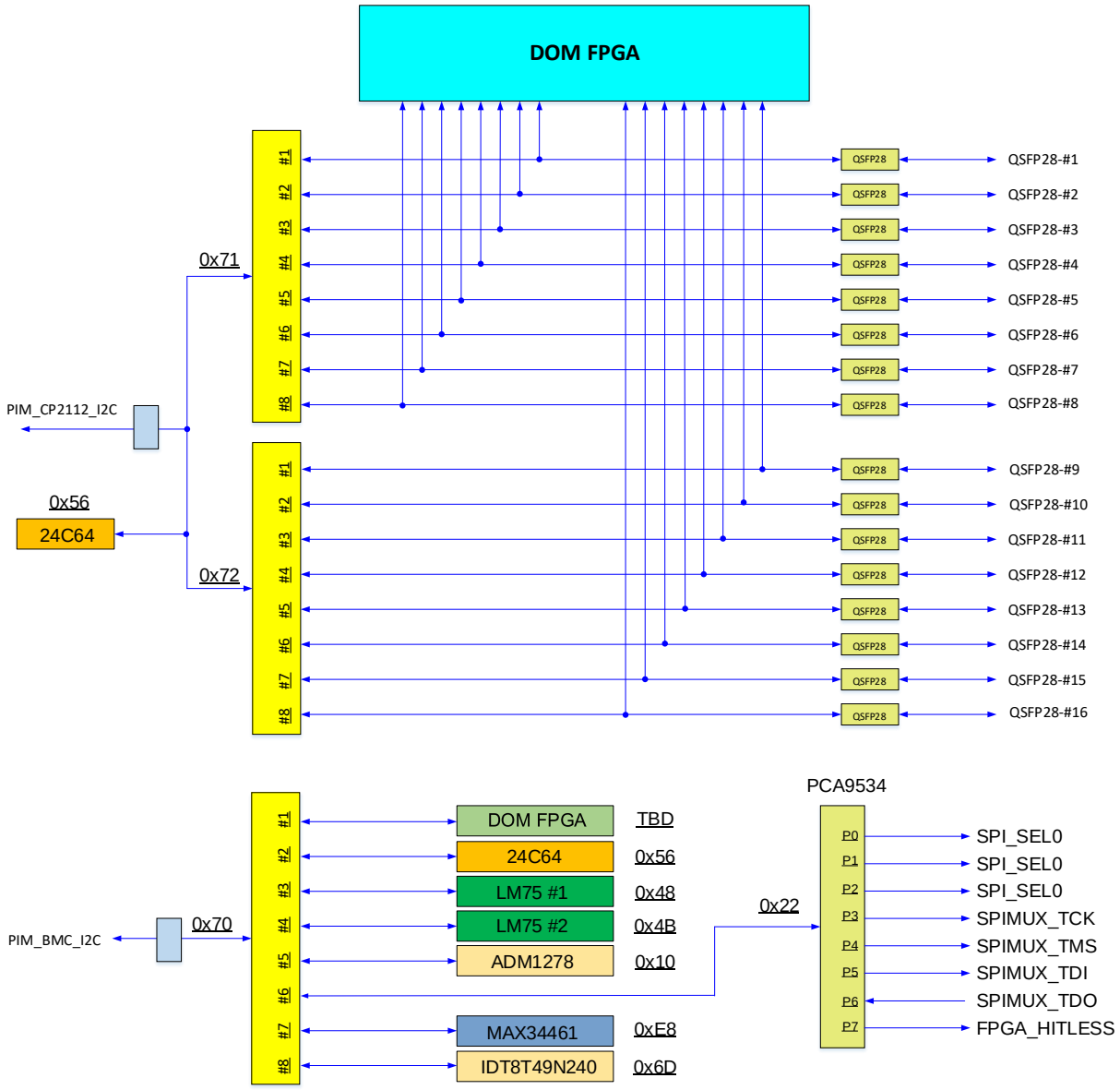


Figure 8-6: PIM-16Q I2C Diagram

BMC I2C	PCA9548	Sub-bus	I2C Device	I2C Address	
	0x70	CH #1	DOM FPGA	0x39	DOM FPGA
		CH #2	EEPROM	0x51	PIM Inventory EEPROM
		CH #3	LM75 #1	0x48	PIM Temperature sensor #1
		CH #4	LM75 #2	0x49	PIM Temperature sensor #2
		CH #5	ADM1278	0x10	Hot swap controller
		CH #6	PCA9534	0x22	SPI mux control
		CH #7	MAX34461	0xE8	Voltage monitor
		CH #8	IDT8T49N240	0x6D	Clock driver

Table 5: PIM-16Q Devices on BMC I2C Buses

CP2112 I2C	I2C	Sub-bus	I2C Device	I2C Address	
PCA9548	0x71	CH #1	QSFP28 #1	0x50	QSFP28 Port #1
		CH #2	QSFP28 #2	0x50	QSFP28 Port #2
		CH #3	QSFP28 #3	0x50	QSFP28 Port #3
		CH #4	QSFP28 #4	0x50	QSFP28 Port #4
		CH #5	QSFP28 #5	0x50	QSFP28 Port #5
		CH #6	QSFP28 #6	0x50	QSFP28 Port #6
		CH #7	QSFP28 #7	0x50	QSFP28 Port #7
		CH #8	QSFP28 #8	0x50	QSFP28 Port #8
PCA9548	0x72	CH #1	QSFP28 #9	0x50	QSFP28 Port #9
		CH #2	QSFP28 #10	0x50	QSFP28 Port #10
		CH #3	QSFP28 #11	0x50	QSFP28 Port #11
		CH #4	QSFP28 #12	0x50	QSFP28 Port #12
		CH #5	QSFP28 #13	0x50	QSFP28 Port #13
		CH #6	QSFP28 #14	0x50	QSFP28 Port #14
		CH #7	QSFP28 #15	0x50	QSFP28 Port #15
		CH #8	QSFP28 #16	0x50	QSFP28 Port #16
24C64	0x56	24C64 EEPROM for PIM-16Q			

Table 6: PIM-16Q Devices on SMB CP2112 I2C Bus

8.3.5 PIM-16Q SPI Architecture

The SPI design of PIM-16Q is shown by the following diagram:

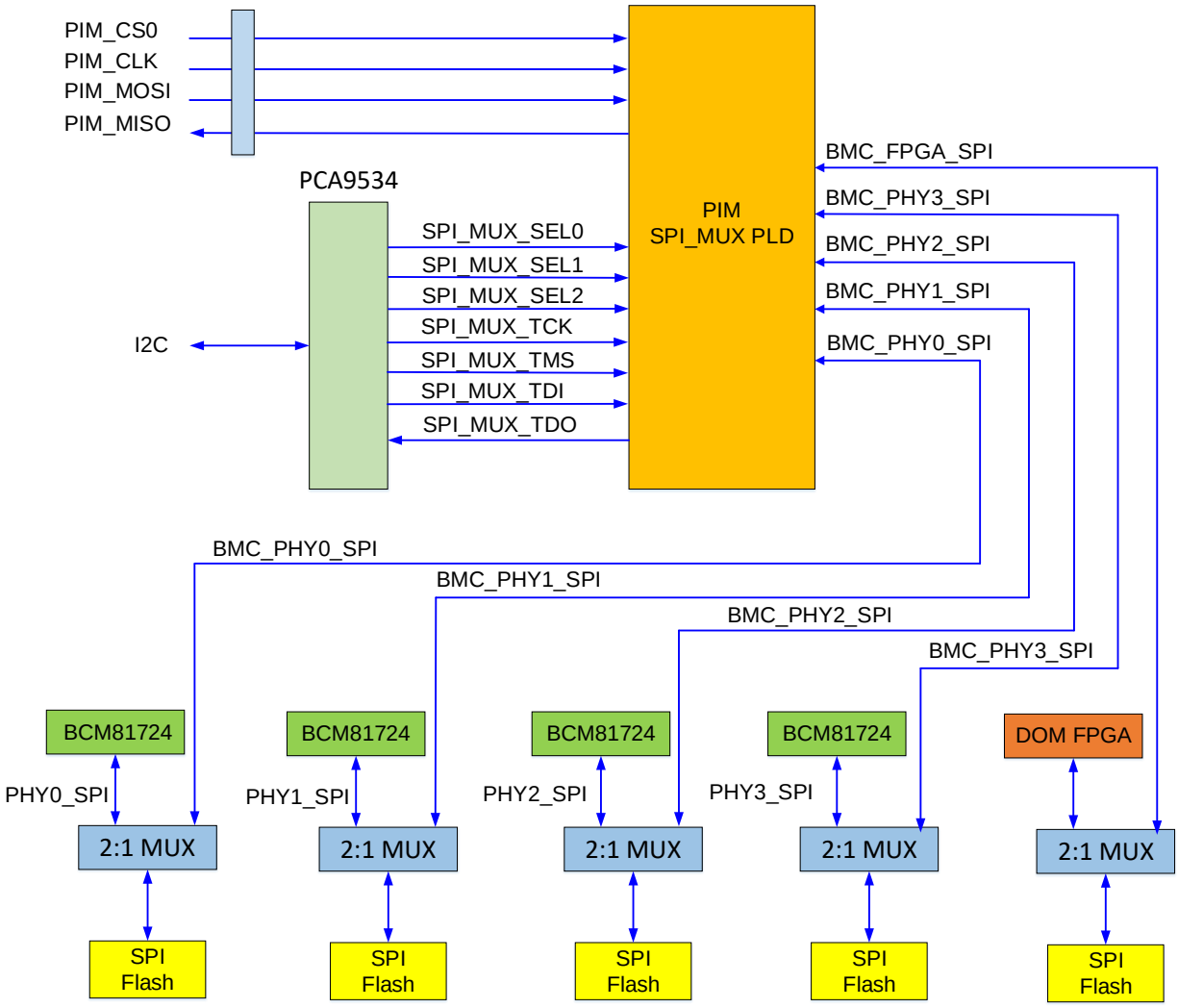


Figure 8-7: PIM-16Q SPI Architecture

8.3.6 PIM-16Q MDIO Architecture

The MDIO design of PIM-16Q is shown by the following diagram:

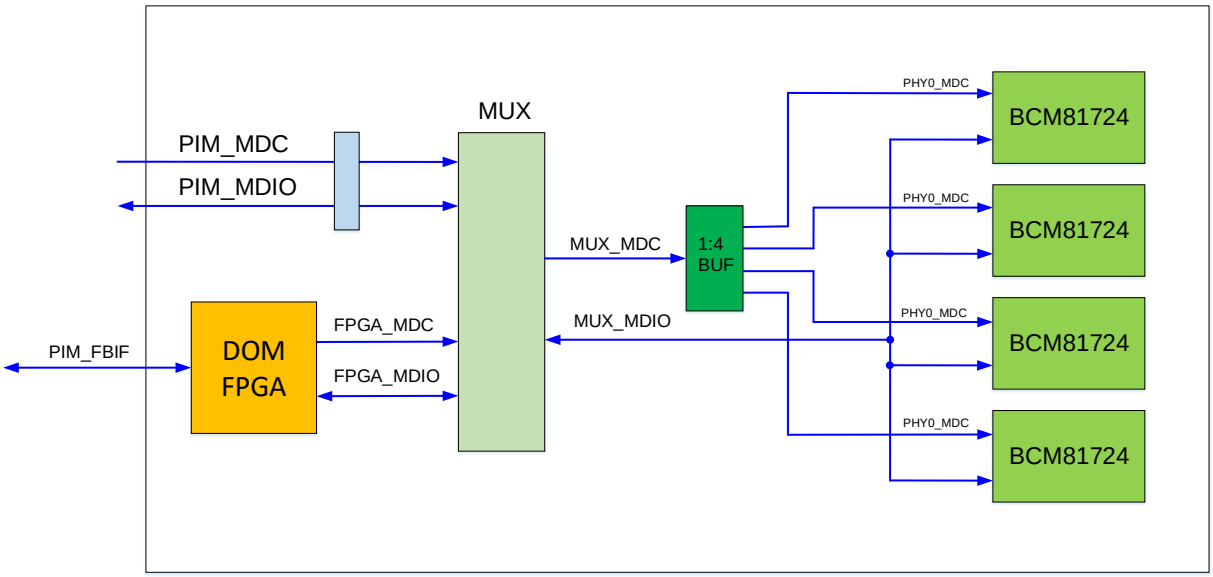


Figure 8-8: PIM-16Q MDIO Interface

8.4 PIM-4DD 4x 400G Port Interface Module

The PIM-4DD card provide 4 x 400G connection to Minipack system. each PIM-4DD card supports four QSFP-DD connector which can support 400G-DR4, 400G-FR4 optics.

8.4.1 Block Diagram of PIM-4DD

Each PIM-4DD has the following components:

- 4 QSFP-DD ports, each QSFP-DD port can support 12W QSFP-DD 400G optic transceiver.
- 4 BCM81328 Gearbox chips. Each BCM81328 can support 8x 50G PAM4 to 8x 50G PAM4 retimer function
- 64 pairs of 50G PAM4 TX and RX signals connect to Tomahawk3 ASIC on SMB
- DOM FPGA is used to support DOM polling function, MDIO access function, and QSFP-DD control and status function
- Two temperature sensors: front and rear
- EEPROM for inventory information of PIM-4DD
- Power is provided by PDB-H, and can be controlled by hot swap controller ADM1278

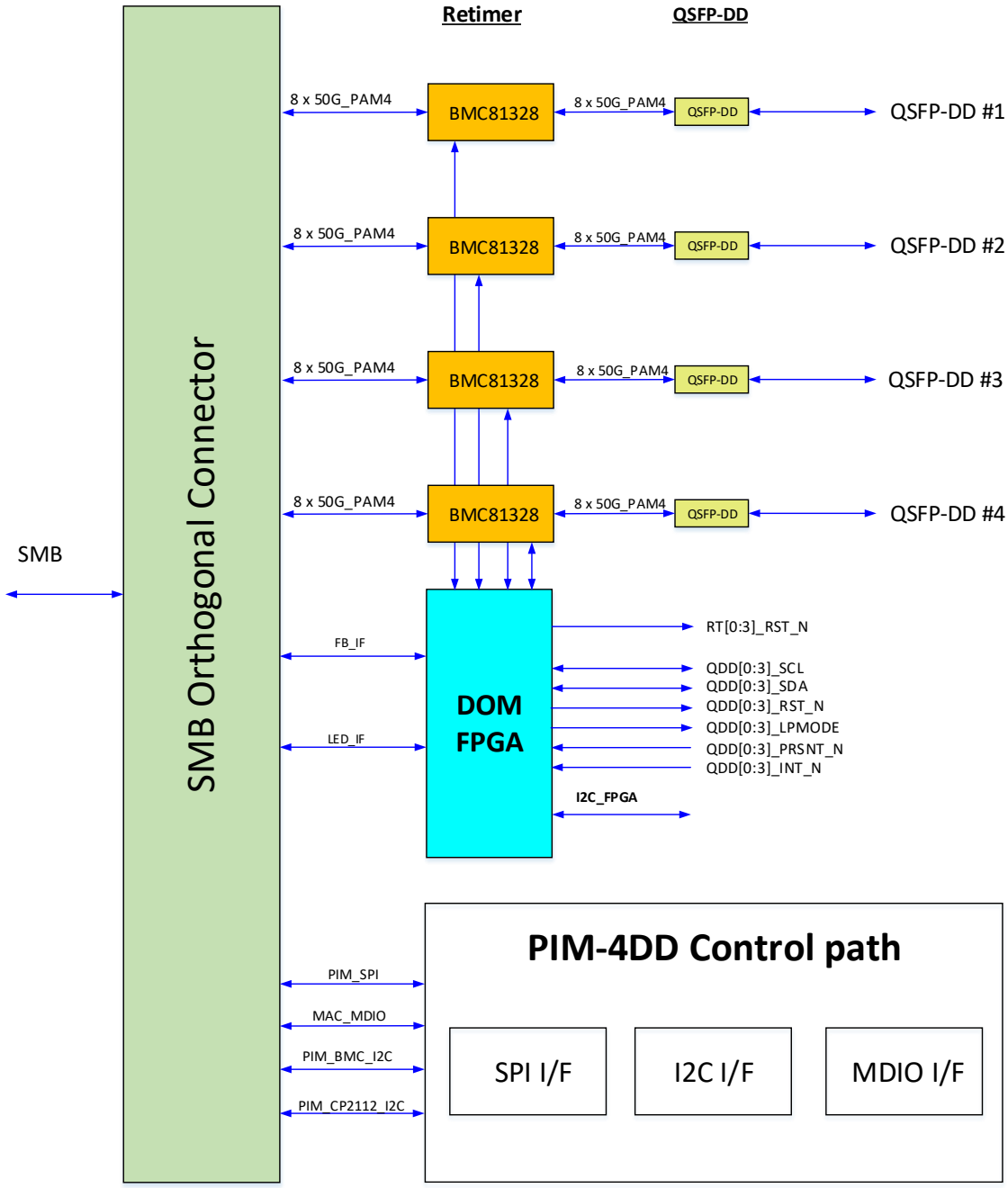


Figure 8-9: PIM-4DD 4x 400G Port Interface Module Diagram

8.4.2 PIM-4DD I2C Architecture

The I2C architecture of PIM-4DD is shown in the following diagram:

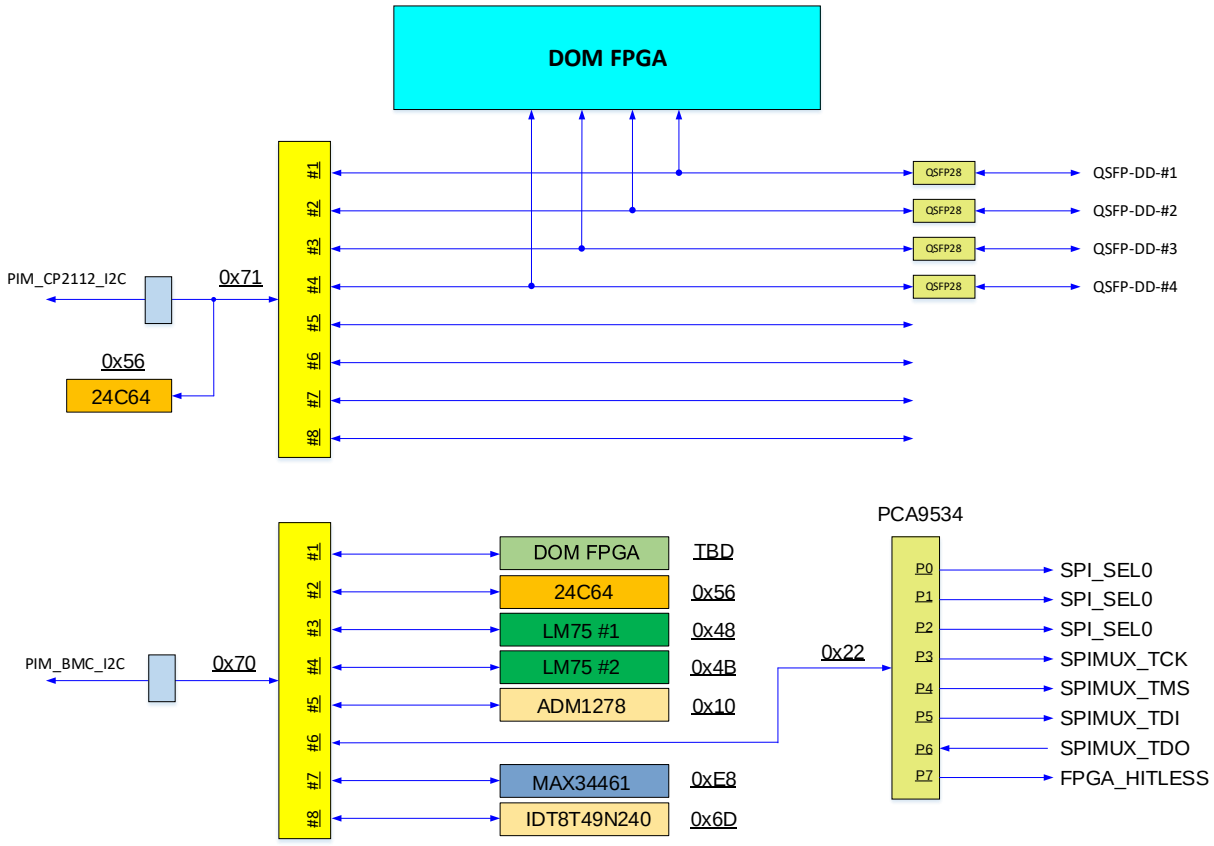


Figure 8-10: PIM-4DD I2C Architecture

BMC I2C	PCA9548	Sub-bus	I2C Device	I2C Address	
	0x70	CH #1	DOM FPGA	0x39	DOM FPGA
		CH #2	EEPROM	0x51	PIM Inventory EEPROM
		CH #3	LM75 #1	0x48	PIM Temperature sensor #1
		CH #4	LM75 #2	0x49	PIM Temperature sensor #2
		CH #5	ADM1278	0x10	Hot swap controller
		CH #6	PCA9534	0x22	SPI mux control

		CH #7	MAX34461	0xE8	Voltage monitor
		CH #8	IDT8T49N240	0x6D	Clock driver

Table 7: PIM-4DD Devices on BMC I2C Buses

CP2112 I2C	I2C	Sub-bus	I2C Device	I2C Address	
PCA9548	0x71	CH #1	QSFP-DD #1	0x50	QSFP-DD Port #1
		CH #2	QSFP-DD #2	0x50	QSFP-DD Port #2
		CH #3	QSFP-DD #3	0x50	QSFP-DD Port #3
		CH #4	QSFP-DD #4	0x50	QSFP-DD Port #4
24C64	0x56	24C64 EEPROM for PIM-16Q			

Table 8: PIM-4DD Devices on SMB CP2112 I2C Bus

8.4.3 PIM-4DD SPI Architecture

The SPI design of PIM-4DD is shown by the following diagram:

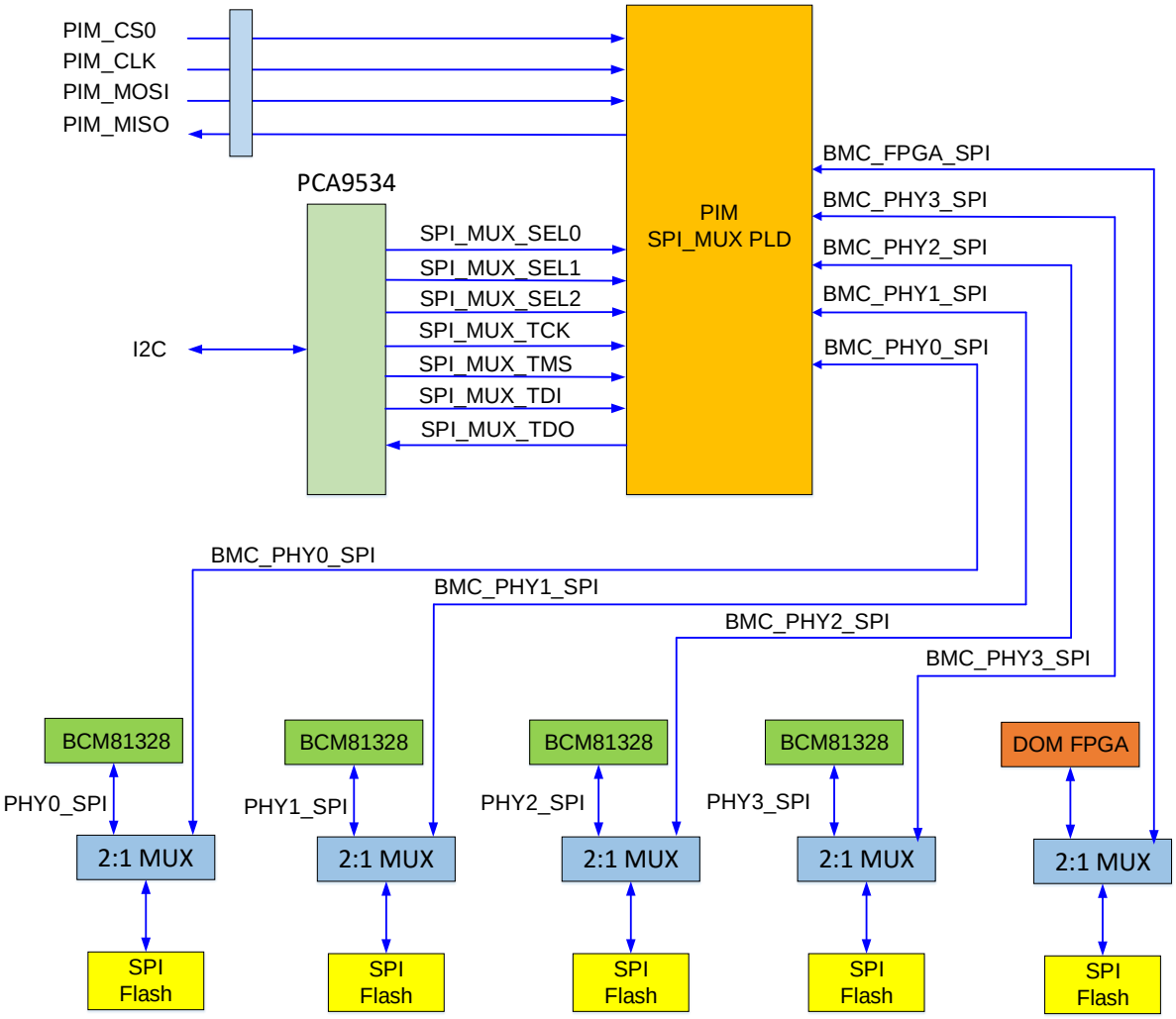


Figure 8-11: PIM-4DD SPI Architecture

8.4.4 PIM-4DD MDIO Architecture

The MDIO design of PIM-4DD is shown by the following diagram:

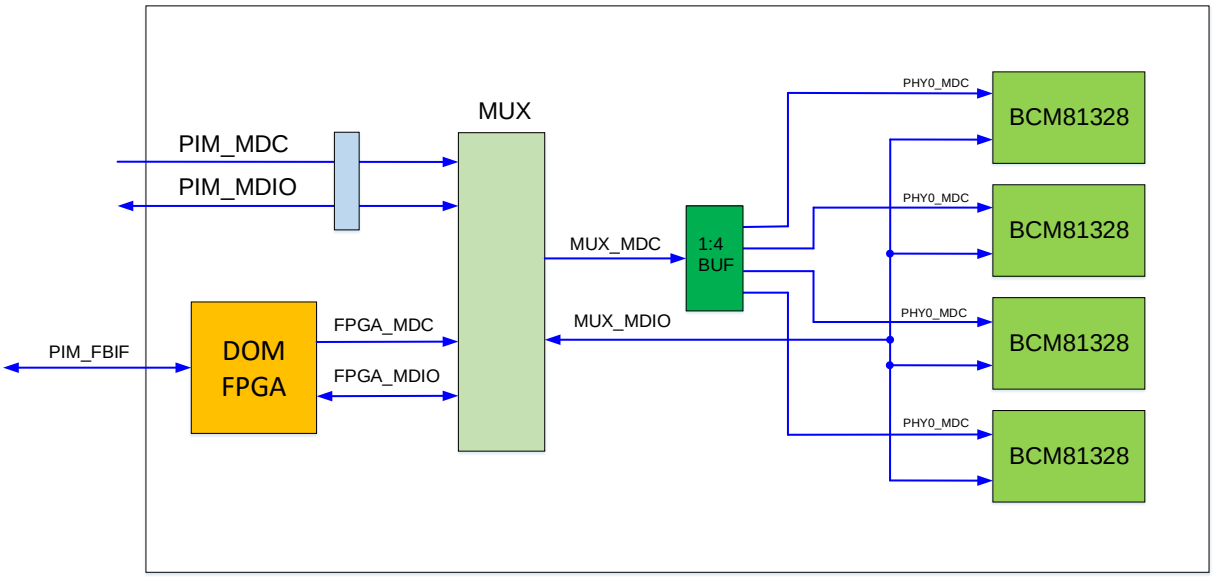


Figure 8-12: PIM-4DD MDIO Architecture

8.5 System Control Module

The System Control Module(SCM) has the host COM-e CPU for Tomahawk3 ASIC. The SCM supports one Broadwell-DE COM-e CPU module.

8.5.1 System Control Module Block Diagram

Each SCM has the following components:

- BW-DE COM-e CPU modules
- RJ45 console port
- RJ45/SFP OOB 10/100/1000Mbps ethernet port
- USB Type-A port on front panel
- One M.2 256GB SATA SSD
- One M.2 256GB NVMe SSD
- CPLD is used to provide control and management function for SCM.
- One dedicated I2C management bus for SMB BMC to access SCM
- SMB bus to SMB

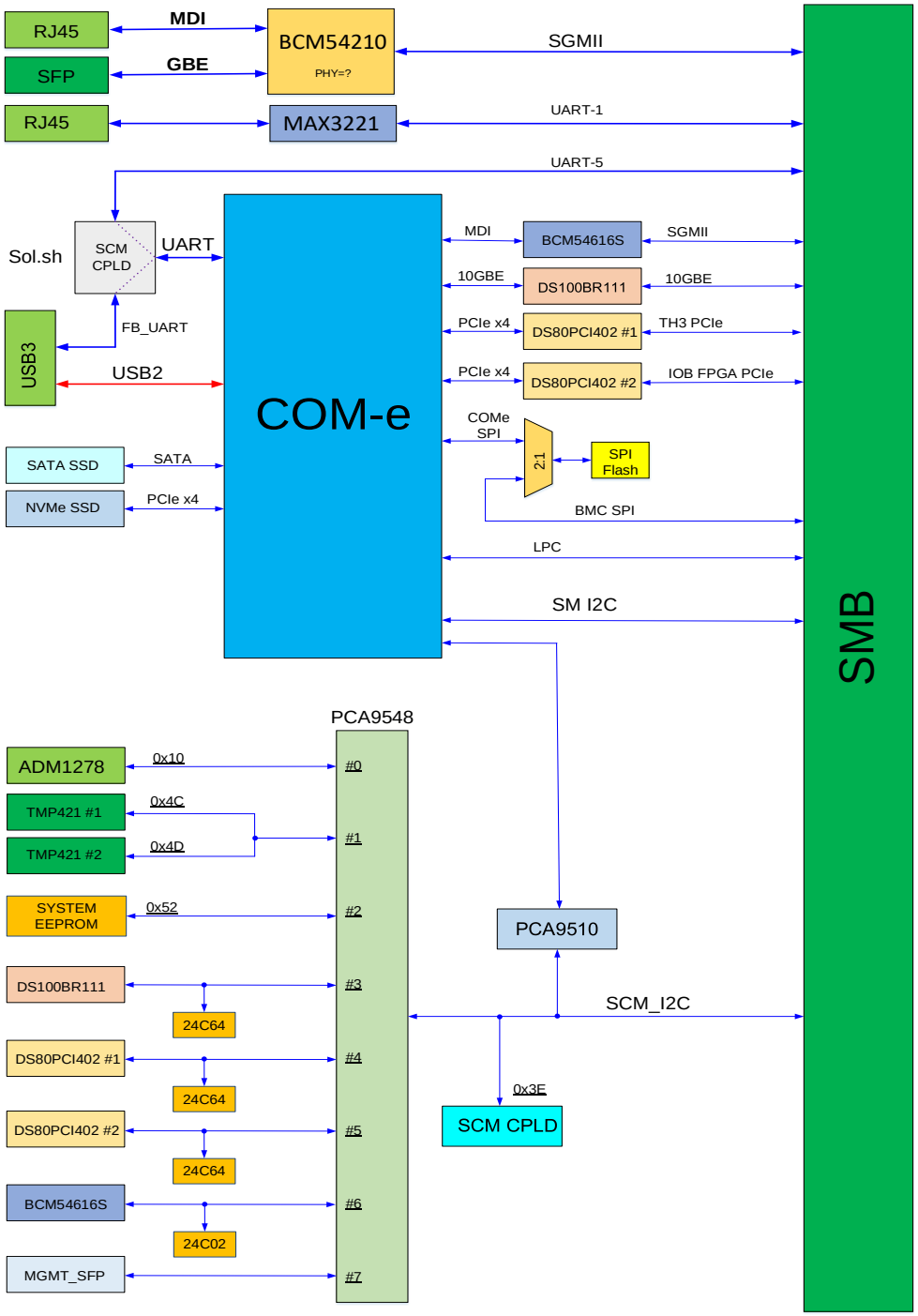


Figure 8-13: System Controller Module(SCM) Block Diagram

8.5.2 PCIe Bus

A x4 PCIe Gen-3 port of COM-e CPU module at SCM is routed across the direct-orthogonal mated connector to the Tomahawk3 switch ASIC on SMB. TI DS80PCI402SQE/NOPB may be used as repeater on the PCIe interfaces on SBM to extend the reach between SCM COM-e CPU and the switch ASIC. The DS80PCI402 is a low-power, 4-lane repeater with 4-stage input equalization, and an output de-emphasis driver to enhance the reach of PCIe serial links in board-to-board or cable interconnects.

Another single lane PCIe Gen-2 port of the CPU is connected to IO Bridge FPGA of SMB, IOB FPGA is PCIe target device of COM-e CPU, it interfaces with eight DOM FPGA via facebook proprietary PIM_FB_IF highspeed control bus.

The third PCIe x4 bus is reserved on SCM for NVMe SSD.

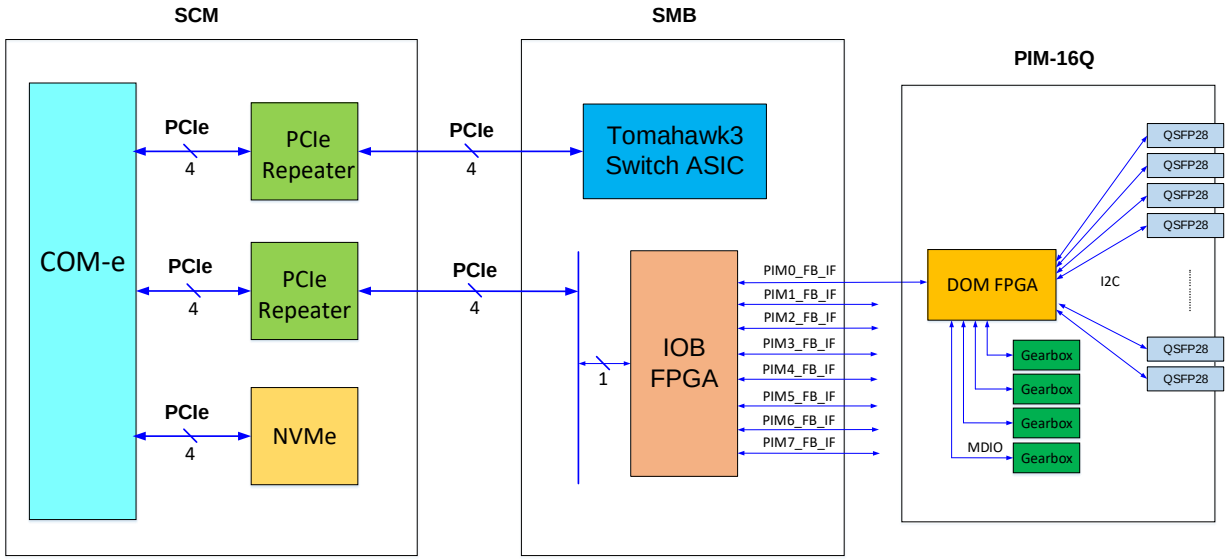


Figure 8-14: PCIe Bus of Minipack

8.5.3 MDIO Control Bus

There are two MDIO control paths in Minipack system:

- CPU-TH3-PHY MDIO interface
- CPU-IOB-DOM-PHY MDIO interface

The traditional MDIO interface goes through tomahawk3 switch ASIC, then from toamahwk3 ASIC to BCM81724 gearbox PHY or BCM81328 retimer PHY. This path is slow and not efficient.

A new MDIO control path via IOB FPGA is designed in parallel with traditional MDIO path. CPU can access BCM81724 gearbox PHY ot BCM81328 retimer PHY on PIM card via PCIe interface to IOB FPGA, through FB-IF to DOM FPGA, and then to gearbox PHY or retimer PHY. The following diagram show the two MDIO control path design.

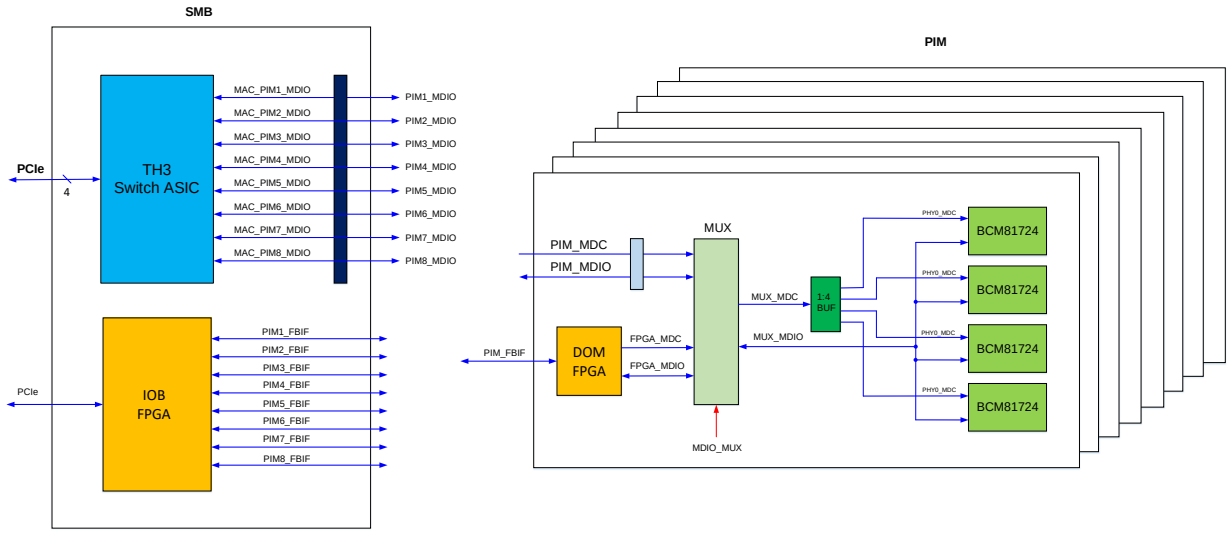


Figure 8-15: MDIO Control Path Architecture

8.5.4 SCM and SMB I2C Bus

COM-e CPU can access SMB and PIM I2C devices through USB CP2112 control path, similar to wedge100 TOR switch design. CP2112 is USB to I2C bus bridge, it can access SMB SYSCPLD, SMB inventory EEPROM, and eight PIM I2C interface via PCA9548 I2C MUX.

Infineon SLB9665TT2.0 is the TPM with LPC interface. it is implemented on minilake COM-e module, no need to be put on SCM now.

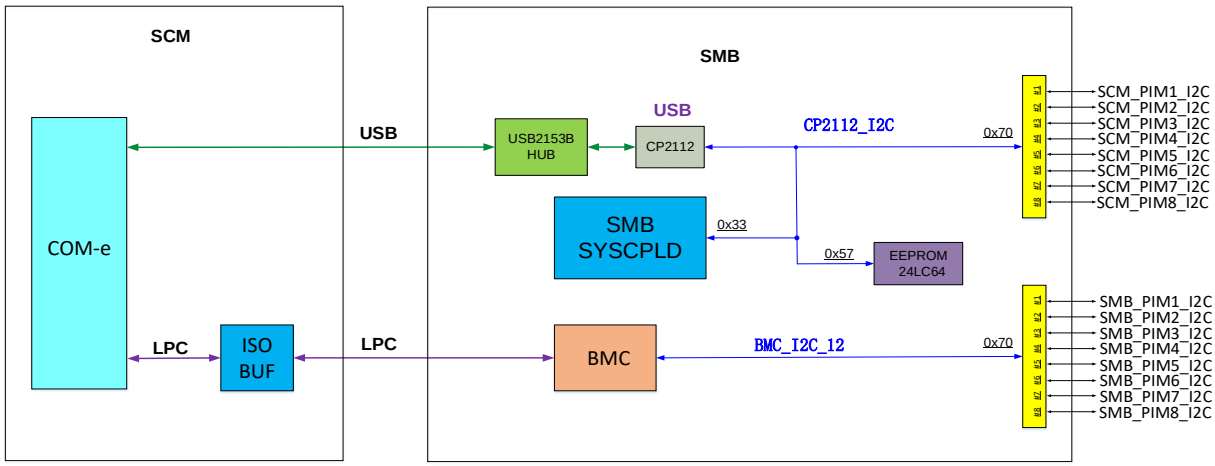


Figure 8-16: SCM and SMB I2C Bus Diagram

8.5.5 SPI Bus of SCM

COM-e local SPI bus is used for the access of second booting SPI flash of CPU, the second booting SPI flash memory is on SCM main board, which can be accessed by both COM-e CPU and BMC chip on SMB. if the COM-e CPU module is booting from second flash on main board, BMC has the capability to update booting SPI flash memory, it provides online upgrade capability of COM-e CPU BIOS, and is very useful in data center operation.

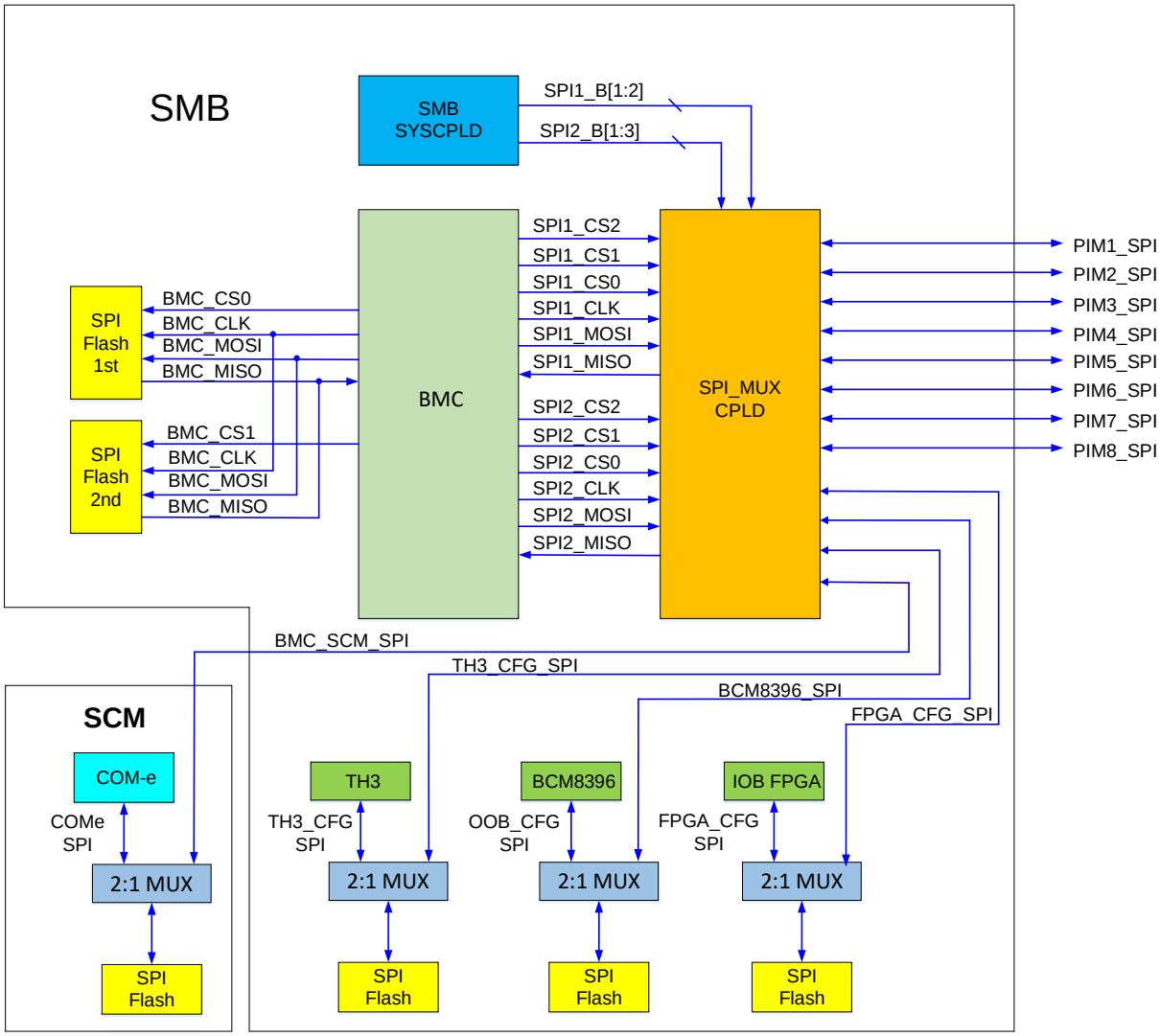


Figure 8-17: SPI Bus of SCM and SMB

8.5.6 SCM and SMB USB Architecture

The USB 2.0 interface of SCM COM-e CPU is extended across orthogonal connector and connect to SMB. A 3-port USB hub is located at SMB to provide multiple USB connection to BMC, CP2112, and one unused debug port. The following diagram shows the architecture of USB interface.

The USB 3.0 Type-A connector on the SCM front panel supports Facebook USB 3.0 debug dongle. It only supports USB 2.0, and the additional pins on the USB 3.0 Type-A connector are carrying a serial console port and an I2C bus for debug purposes.

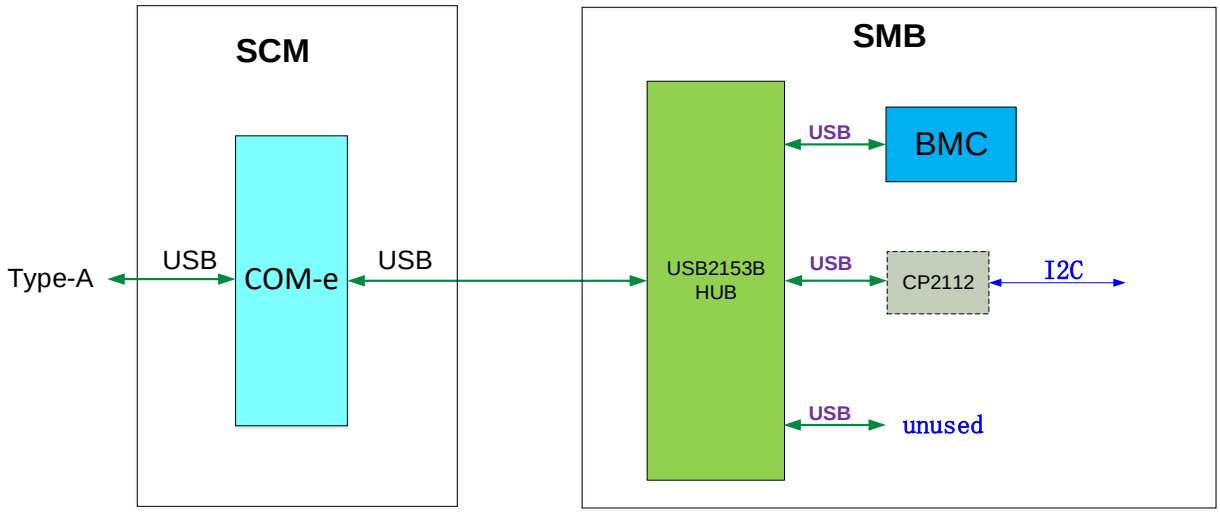


Figure 8-18: SCM USB Architecture

8.5.7 10G-KR Interface

SCM reserves one pair of 10G-KR differential signals to SMB, and it follows COM-Express Type-7 pinout for 10G-KR signals on the COM-Express module.

8.5.8 Hot Swap Design of SCM

SCM uses ADM1278 as hot swap controller, it supports current, voltage, power, temperature read back via an integrated 12bit ADC , it can be accessed using a PMBus interface.

System can read input voltage, output voltage, measured current, measured temperature via PMbus. ADM1278 PMBus address is 0x10.

8.5.9 COM-Express CPU Module

COM-e CPU module is the control CPU for the switch system. In the first EVT phase of Minipack project, Portwell PCOM-B634VG Type-6 COM-e CPU module is used. It is based on Intel Broadwell-DE Processor D1508 SOC and has an 8GB DDR4 SODIMM with ECC support.

SCM shall support both COM-Express Type-6 and Type-7 modules. The 10G-KR interface support requires Type-7 module.

For Minipack production, we have the following COM-e requirements.

- Processor
  - Intel® Broadwell-DE processor D1527, 14nm process node
  - Quad core, 2.2Ghz Base, 2.6Ghz Turbo
  - Last Level Cache 6MB
  - 35W TDP
  - Support Intel Hyper-Threading technology
  - Support Intel TXT technology
- BIOS
  - AMI BIOS
- Memory
  - Each SODIMM slot supports up to 16GB DDR4 SODIMM w/ ECC and runs up to 2133MT/s.
  - 2x 16GB DDR4 SODIMM w/ ECC @ 2133MT/s
  - One SODIMM on one IMC channel
- Storage Devices
  - M.2 2280 form factor
  - 1x SATA 3.0
  - Or, 4x PCIe Gen-3 NVMe

    - 256GB
    - Only one SSD is required as the CPU boot storage.
- Watchdog Timer
    - Programmable by embedded controller
- Expansion Interface
    - Supports up to 8 PCI Express Gen-2 lanes, and up to 16 PCIe Gen-3 lanes.
    - 1 SPI interface for BIOS on carrier board
    - 1 SMBus interface
    - 1 I2C interface
    - 1 LPC interface
- I/O Interface
    - 1 Ethernet - Onboard Intel I210IT
    - At least 1 serial ports supported by onboard EC(Embedded Controller)
    - USB
        - At least one USB2.0
    - 10G-KR support in Type-7 pinout
- Mechanic and Environment
    - Dimension - 95mm(L) x 125mm(W) x 2.0mm(H)
    - Power Supply - DC 5V~13V
    - Environment
        - Operation temperature: -20~85°C (SoC SKU dependent)
        - Storage temperature: -20~85°C
        - Relative humidity : 0~95%, non-condensing
    - MTBF
        - Over 300,000 hours at 45°C

Minipack uses the following configuration:

- Boot SPI Flash: 16Mbyte, secondary on SCM main board
- M.2 SSD: One with SATA interface and one with NVMe interface. 256GB, physically located on SCM. Only one is required as the CPU boot storage.
- Memory: 32Gbyte DDR4 with thermal sensor, two socket of 240-pin SODIMM
- BIOS: AMI UEFI
- Ethernet: 1000Base-T, BCM PHY on SCM main board to provide SGMII interface
- PCIe: 3x root ports
    - PCIe Gen-3 x4: Tomahawk3
    - PCIe Gen-3 x4: M.2 NVMe SSD
    - PCIe Gen-1 x1: IOB FPGA
- SATA: 1x SATA 6.0Gb/s for M.2 SSD access

- USB port: 1x USB 2.0 port is used SMB USB interface; 1x USB 2.0 is used for front panel port
- WDT: programmable via SW from 1s to 255min
- LPC: LPC bus at 33.33Mhz

The following is the block diagram of the COM-e module for Minipack production.

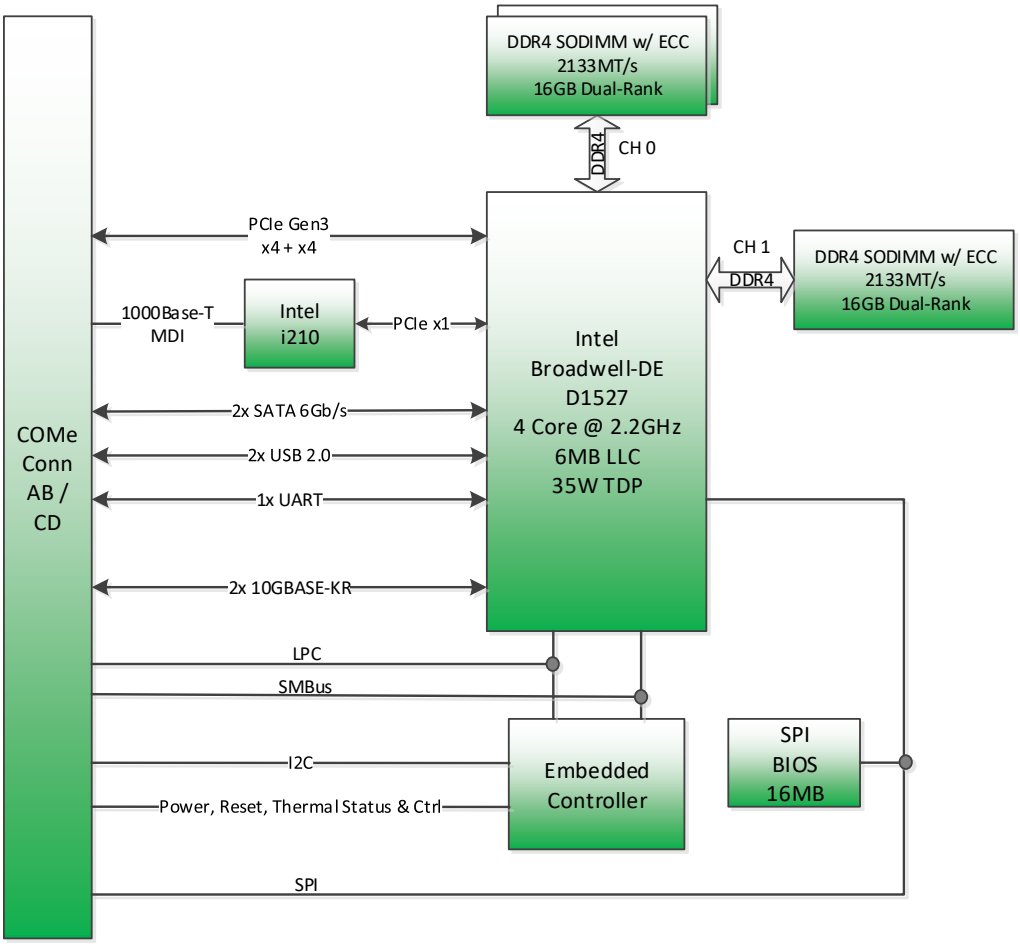


Figure 8-19: COM-e CPU Module Block Diagram

8.6 Fan Control Module (FCM) and Fan-tray

Minipack uses eight 80mm x 80mm x 80mm CR fan to provide forced air cooling to the chassis. There are two Fan Control Module(FCM) inside Minipack chassis: FCM-T and FCM-B, FCM-T controls the top four fan trays, and FCM-B controls the bottom four fan trays. Each FCM has one CPLD used for fan control and fan status monitor. The BMC of SMB can access the fan control CPLD via a system management I^2C bus.

The following diagram shows the functional blocks of fan control module:

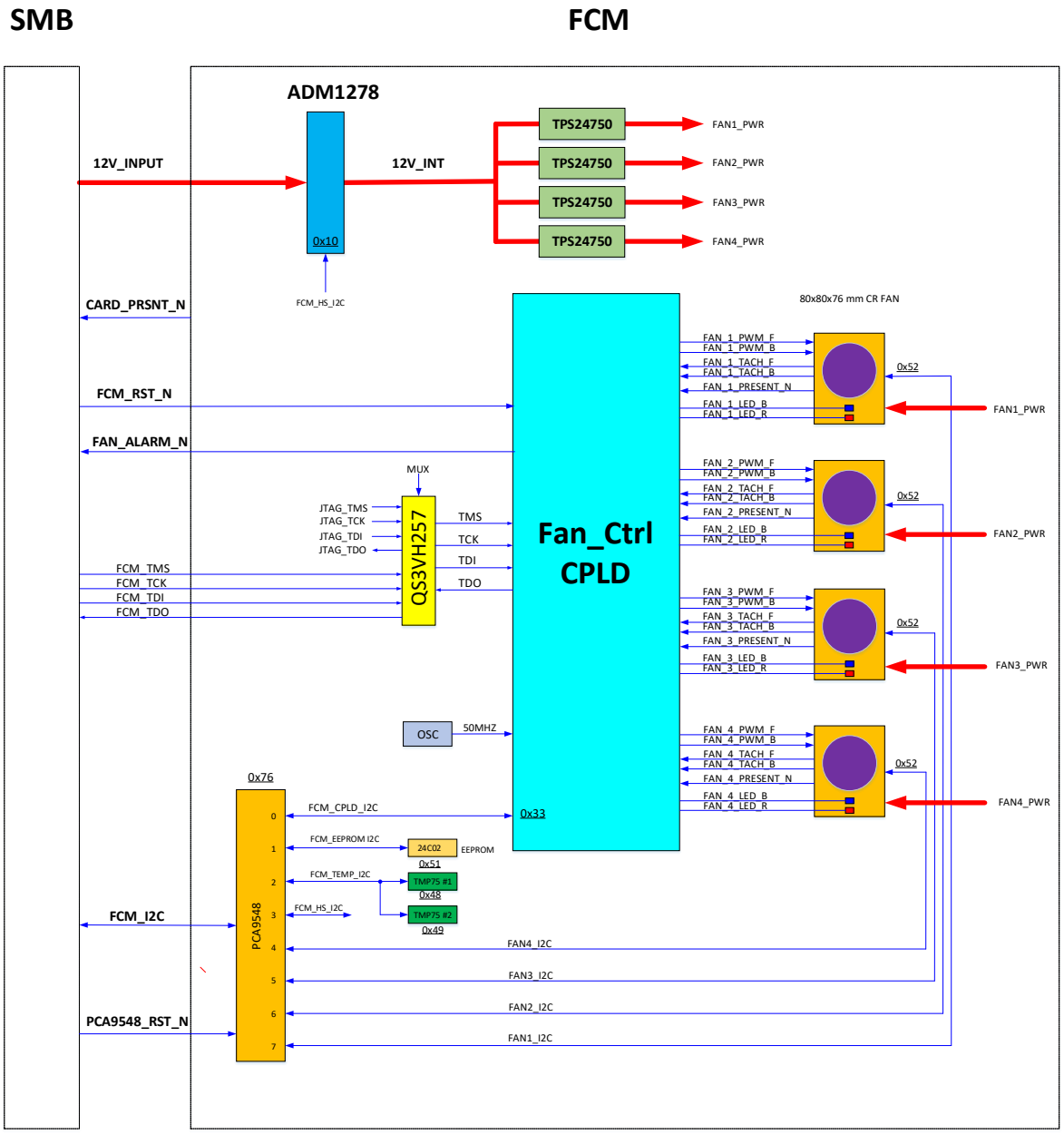


Figure 8-20: FAN Control Module (FCM)

8.6.1 Fan Control

Fan control CPLD controls the fan operation. For Minipack fan-tray, the maximal fan speed is about 12000 RPM. The period time is 200 ms, and CPLD uses

- 200ms/m = 1/2 * TS
- TS = 60/N
- N=60/TS= 60/0.4*m=150*m

SW must multiple 150 and show it as RPM (Revolutions Per Minute)

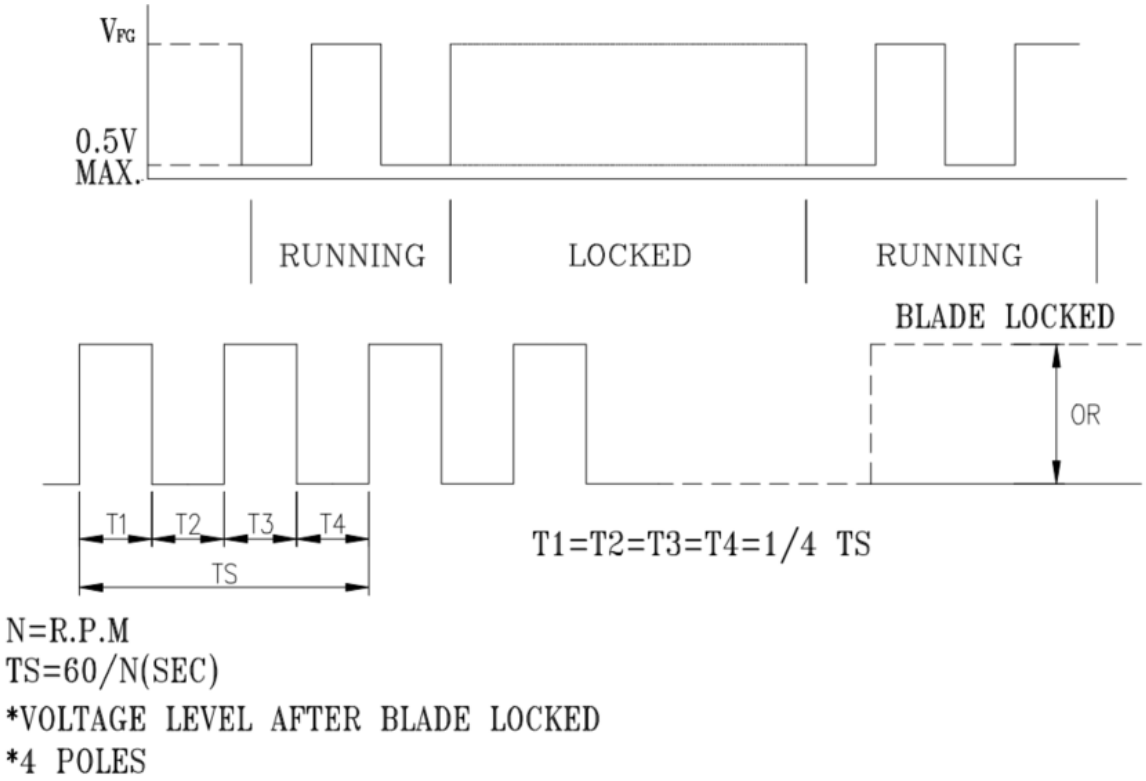


Figure 8-21: Fan Tachometer Output Waveform

Fan PWM control settings are shown in the below table.

FAN_PWM [5:0]	**Duty Cycle**
00_0000	0/63 or 0% duty cycle
00_0001	1/63 or 1.549 % duty cycle

00_0010	2/63 or 3.116 % duty cycle
00_0011	3/63 or 4.671 % duty cycle
00_0100	4/63 or 6.235 % duty cycle
00_0101	5/63 or 7.804 % duty cycle
00_0110	6/63 or 9.358 % duty cycle
00_0111	7/63 or 10.923 % duty cycle
00_1000	8/63 or 12.485 % duty cycle
00_1001	9/63 or 14.047 % duty cycle
00_1010	10/63 or 15.611 % duty cycle
00_1011	11/63 or 17.174 % duty cycle
00_1100	12/63 or 18.732 % duty cycle
00_1101	13/63 or 20.295 % duty cycle
00_1110	14/63 or 21.864 % duty cycle
00_1111	15/63 or 23.414 % duty cycle
01_0000	16/63 or 24.987 % duty cycle
01_0001	17/63 or 26.553 % duty cycle
01_0010	18/63 or 28.121 % duty cycle
01_0011	19/63 or 29.678 % duty cycle
01_0100	20/63 or 31.234 % duty cycle
01_0101	21/63 or 32.795 % duty cycle
01_0110	22/63 or 34.375 % duty cycle
01_0111	23/63 or 35.923 % duty cycle
01_1000	24/63 or 37.482 % duty cycle

01_1001	25/63 or 39.048 % duty cycle
01_1010	26/63 or 40.617 % duty cycle
01_1011	27/63 or 42.177 % duty cycle
01_1100	28/63 or 43.732 % duty cycle
01_1101	29/63 or 45.303 % duty cycle
01_1110	30/63 or 46.863 % duty cycle
01_1111	31/63 or 49.900 % duty cycle
10_0000	32/63 or 51.546 % duty cycle
10_0001	33/63 or 53.109 % duty cycle
10_0010	34/63 or 54.669 % duty cycle
10_0011	35/63 or 56.234 % duty cycle
10_0100	36/63 or 57.789 % duty cycle
10_0101	37/63 or 59.369 % duty cycle
10_0110	38/63 or 60.932 % duty cycle
10_0111	39/63 or 62.495 % duty cycle
10_1000	40/63 or 64.041 % duty cycle
10_1001	41/63 or 65.613 % duty cycle
10_1010	42/63 or 67.177 % duty cycle
10_1011	43/63 or 68.745 % duty cycle
10_1100	44/63 or 70.295 % duty cycle
10_1101	45/63 or 71.863 % duty cycle
10_1110	46/63 or 73.419 % duty cycle
10_1111	47/63 or 74.975 % duty cycle

11_0000	48/63 or 76.553 % duty cycle
11_0001	49/63 or 78.106 % duty cycle
11_0010	50/63 or 79.671 % duty cycle
11_0011	51/63 or 81.234 % duty cycle
11_0100	52/63 or 82.796 % duty cycle
11_0101	53/63 or 84.349 % duty cycle
11_0110	54/63 or 85.925 % duty cycle
11_0111	55/63 or 87.482 % duty cycle
11_1000	56/63 or 89.039 % duty cycle
11_1001	57/63 or 90.606 % duty cycle
11_1010	58/63 or 92.169 % duty cycle
11_1011	59/63 or 93.736 % duty cycle
11_1100	60/63 or 95.297 % duty cycle
11_1101	61/63 or 96.861 % duty cycle
11_1110	62/63 or 98.424 % duty cycle
11_1111	63/63 or 100.00 % duty cycle

Table 9: Fan PWM Control

In order to reduce the inrush current after the fan-tray is present, CPLD will automatically control the fan PWM settings after the fan present signal is active. By default the fan PWM target value will be set to 50%. CPLD will take 8S to increase the PWM duty cycle from 0% to 50%. Every 500mS increases a duty cycle level.

Below figure shows the fan present status and the PWM duty cycle control signal.

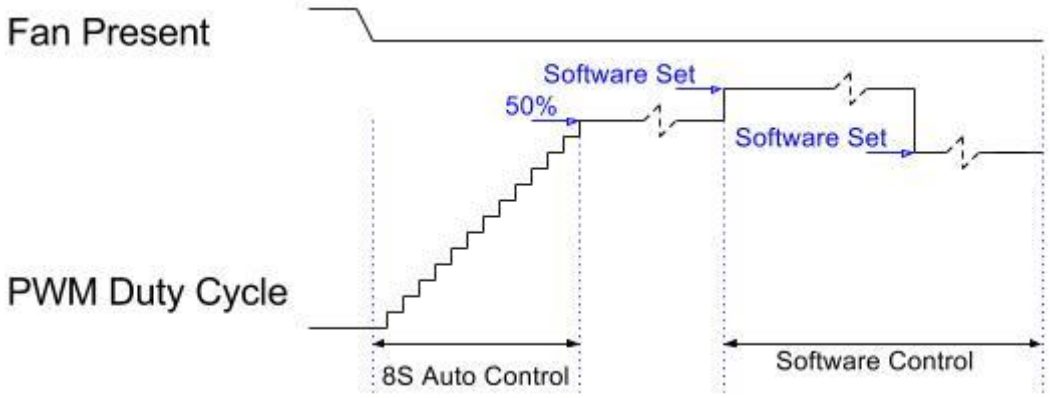


Figure 8-22: Fan PWM and Inrush Current Control

8.6.2 I2C Architecture of FCM

There is one I2C Mux PCA9548 on FCB, 8 sub-ports behind this I2C Mux. The following table shows the sub-bus and devices behind the buses.

PCA9548	PCA9548 I2C Mux for FCM	PCA9548 I2C Addr: 0x70	
Sub-bus and devices behind I2C Mux PCA9548			
Sub-Bus Bus	Sub-Bus function	Level 2 Slave Device	Note
I2C #0	FAN Tray #1 I2C Bus	EEPROM Addr : 0x52	Access fan-tray FRU EEPROM content
I2C #1	FAN Tray #2 I2C Bus	EEPROM Addr : 0x52	
I2C #2	FAN Tray #3 I2C Bus	EEPROM Addr : 0x52	
I2C #3	FCM_CPLD_I2C	CPLD I2C Addr: 0x3E	
I2C #4	FAN Tray #4 I2C Bus	EEPROM Addr : 0x52	
I2C #5	EEPROM I2C	I2C Addr: 0x51	
I2C #6	TMP75 Temperature sensor I2C	TMP75 #1: 0x48	
	TMP75 Temperature sensor I2C	TMP75 #2: 0x49	
I2C #7	ADM1278 hotswap Controller	I2C Addr: 0x10	

Table 10: FCM I2C Devices

The FCM I2C bus is connected to BMC I2c Bus 9.

PDB-L I2C Access			
PCA9548	PCA9548 I2C Mux for PDB	I2C Addr: 0x71	
Sub-bus and devices behind I2C Mux PCA9548 of PDB			
Sub-Bus	Sub-Bus function	Level 2 Slave Device	Note

I2C #0	PSU #1 I2C Bus	EEPROM I2C Addr : 0x50/0x10	
I2C #1	PSU #2 I2C Bus	EEPROM I2C Addr : 0x50/0x10	
I2C #2	PCA9535	I2C Addr : 0x21	
I2C #3	LM75	I2C addr : 0x48	Temp sensor close to PSU-#1
	LM75	I2C Addr: 0x49	Temp sensor close to PSU-#2
I2C #4	Unused		
I2C #5	Unused		
I2C #6	Unused		
I2C #7	Unused		

Table 11: I2C Devices of PDB-L

PDB-R I2C Access			
PCA9548	PCA9548 I2C Mux for PDB	PCA9548 I2C Addr: 0x76	
Sub-bus and devices behind I2C Mux PCA9548 of PDB			
Sub-Bus	Sub-Bus function	Level 2 Slave Device	Note
I2C #0	PSU #3 I2C Bus	EEPROM I2C Addr : 0x50/0x10	
I2C #1	PSU #4 I2C Bus	EEPROM I2C Addr : 0x50/0x10	
I2C #2	PCA9535	I2C Addr : 0x21	
I2C #3	LM75	I2C addr : 0x48	Temp sensor close to PSU-#1
	LM75	I2C Addr: 0x49	Temp sensor close to PSU-#2
I2C #4	Unused		
I2C #5	Unused		
I2C #6	Unused		
I2C #7	Unused		

Table 12: I2C Devices of PDB-R

8.7 Power Distribution Boards (PDB)

Minipack has two power distribution boards (PDB-L and PDB-R) that connect the 4 AC/DC PSUs to the chassis bus bar and SMB. One key feature of the PDB is to support chassis power shutdown, which powers off everything in the Minipack chassis other than the PDB itself.

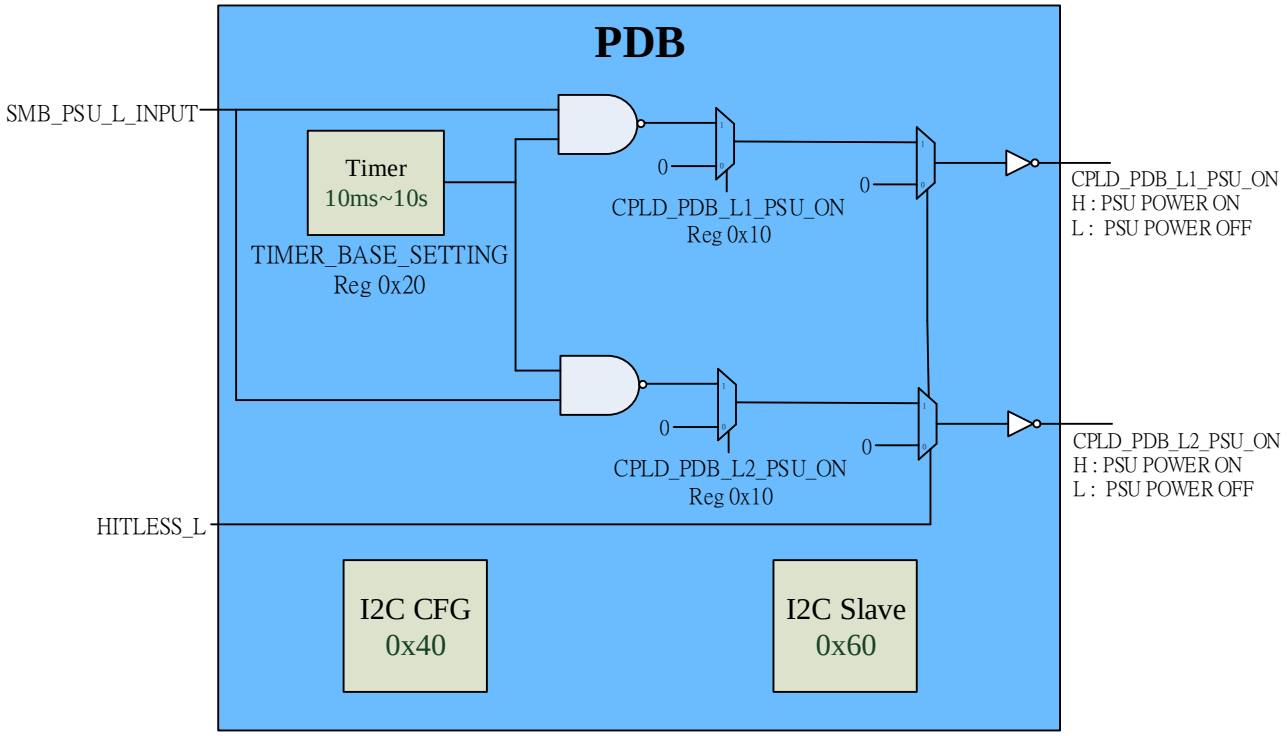


Figure 8-23: Chassis Shutdown by PDB

9 Functional Descriptions

9.1 Orthogonal Direct Architecture

Minipack uses orthogonal direct architecture for chassis design. It does not have a midplane or backplane, and PIM highspeed connector directly mates to the highspeed connector of SMB, providing more air channel for air flow inside chassis. Orthogonal direct architecture can also minimize the high speed PCB trace length to provide much better signal integrity performance than traditional backplane architecture.

Figure 9-1: Front ISO View of Minipack Orthogonal Architecture

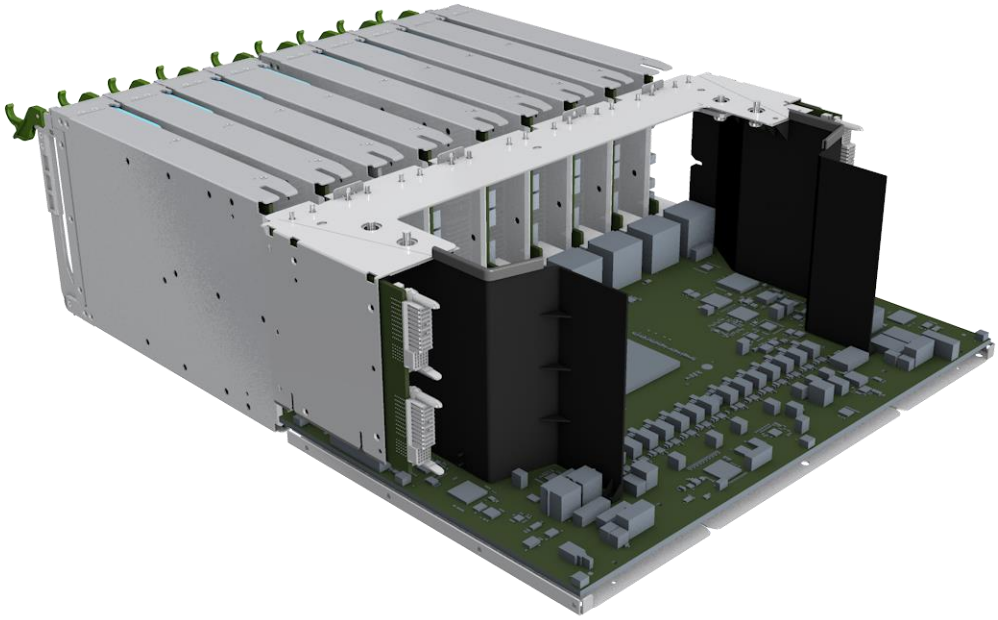


Figure 9-2: Rear ISO View of Minipack Orthogonal Architecture

9.1.1 Direct Mated Orthogonal Connector

Minipack uses FCI EXAMAX+ DMO(Direct Mated Orthogonal) connector for both data plane and control plane interconnect. The following picture shows the typical direct mating diagram of EXAMAX orthogonal direct connector, more information can be downloaded from Amphenol FCI website.

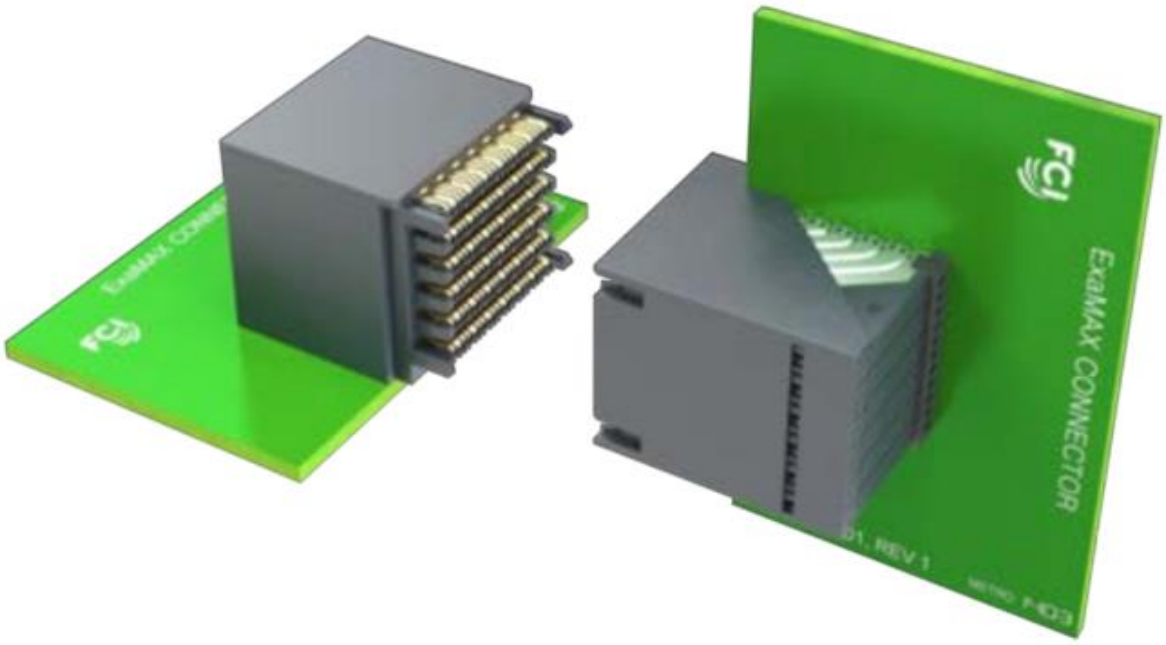


Figure 9-3 : Amphenol FCI EXAMAX DMO Connectors

For highspeed data plane signals, PIM uses four 6x12 Daughter Card RAR (Right Angle Receptacle) to mate RAOH (Right Angle Orthogonal Header) connector of SMB card, only 64 pairs are used among 72 pairs in the 6x12 DMO pair. The rest of 8 differential pairs are used for control plane signals, 6x12 EXAMAX+ connector also has extra 12 single ended signals, which can be used as control signals from SMB.

9.2 Data Plane

Minipack uses Broadcom BCM56980 Tomahakw3 12.8T switch ASIC as the main data plane chip. The Tomahakw3 switch ASIC supports 32 x 400G, or 64 x 200G, or 128 x 100G, or 128 x 40G port configurations.

9.2.1 Switch Element

Facebook OCP switches are always built with the concept of switch element. Each switch element has one BMC, one CPU module (a.k.a micro-server) and one switch ASIC. This unique switch element architecture makes Facebook data center networks disaggregated, easily managed and easy to scale.

Minipack is one switch element which supports 128 x 100G. It can be used in multiple layers of data center networks.

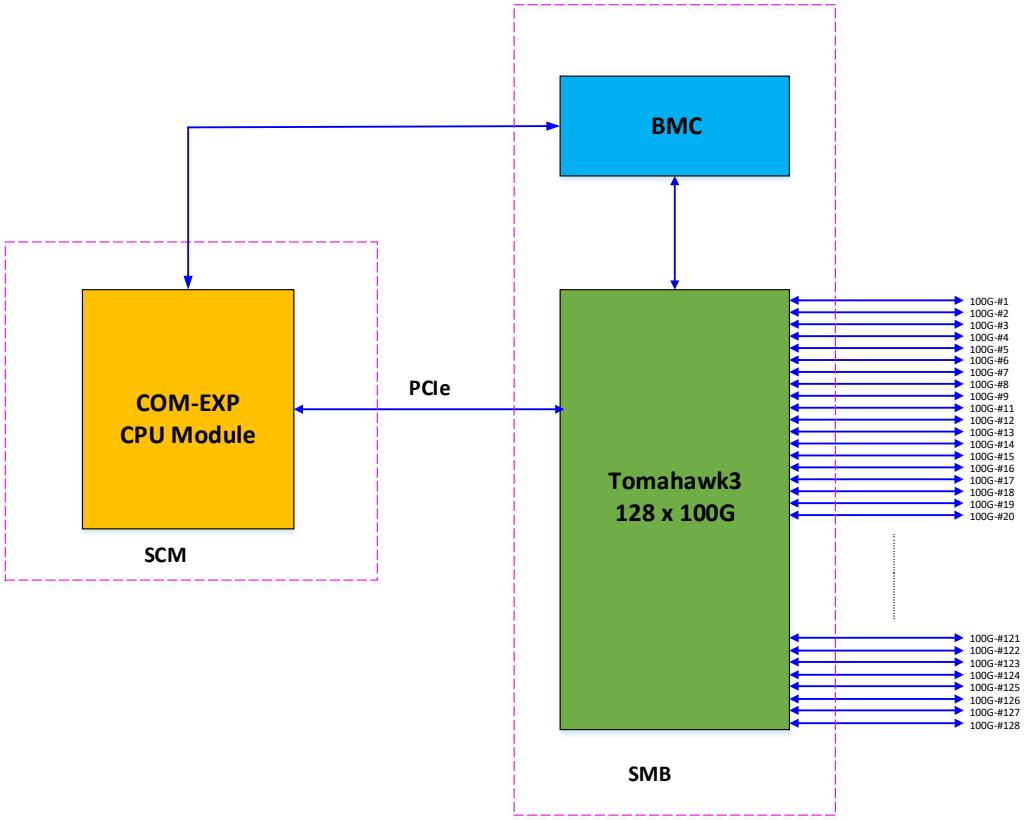


Figure 9-4: Switch Element

9.2.2 Port Mapping between SMB and PIM

In Minipack system, eight PIM and SMB are connected orthogonally. Each PIM connects to four Blackhawk SERDES ports of Tomahawk3.

9.2.2.1 General PIM Card Port Assignment

Eight PIM card and one SCM use orthogonal direct connector EXAMAX connecting to SMB. There is no backplane in Minipack design, SMB and PIM/SCM mate directly in order to minimize the length of PAM4 signal traces from SMB TH3 to PIM gearbox/retimer chip.

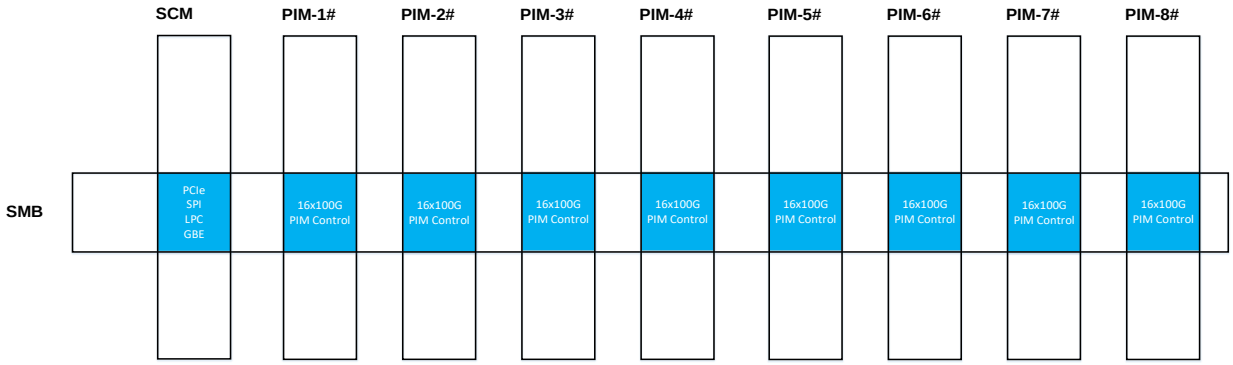


Figure 9-5: PIM Orthogonal Connection to SMB

The port assignment should improve the usage of packet buffer memory and balance the traffic to each pipeline of the switch chip. It is also recommended to distribute the pipelines to different PIM slots.

9.2.2.2 PIM-16Q Port Mapping to SMB

The following table shows the port mapping of Tomahawk3 ASIC SERDES and gearbox port.

		TH3 TX	PIM-16Q RX		TH3 RX	PIM-16Q TX					
SDK Port No.	BC	TX Ln	RX Ln	P/N Swap	RX Ln	TX Ln	P/N Swap	PIM	PIM-16Q	Location	MDIO Address (4:0)
4	BC0	3	7	Y	0	7	N		Q2		

		2	6	Y	1	6	N	PIM-#1		U19-4A	00000 00001 00010 00011
3		0	5	Y	2	5	Y		Q1		
		4	4	N	3	4	N				
2		6	3	N	7	3	Y		Q4		
		7	2	Y	6	2	N				
1		5	1	Y	4	1	N		Q3		
		1	0	Y	5	0	Y				
23	BC4	6	7	Y	5	7	Y		Q6	U25-4B	00100 00101 00110 00111
		5	6	Y	6	6	N				
22		1	5	Y	3	5	Y		Q5		
		0	4	Y	2	4	N				
21		3	3	N	7	3	Y		Q8		
		2	2	Y	4	2	N				
20		4	1	Y	1	1	N		Q7		
		7	0	N	0	0	Y				
43	BC8	4	7	N	7	7	Y		Q10	U30-4C	01000 01001 01010 01011
		2	6	Y	3	6	Y				
42		5	5	N	6	5	Y		Q9		
		1	4	Y	2	4	N				
41		3	3	Y	5	3	N		Q12		
		0	2	N	1	2	Y				
40		7	1	Y	0	1	N		Q11		
		6	0	N	4	0	Y				
63	BC12	5	7	N	3	7	Y		Q14	U22-4D	10000 10001 10010 10011
		7	6	N	2	6	Y				
62		4	5	N	5	5	Y		Q13		
		6	4	N	1	4	N				
61		2	3	N	0	3	Y		Q16		
		1	2	N	4	2	N				
60		0	1	N	6	1	N		Q15		
		3	0	Y	7	0	Y				
8	BC1	1	7	Y	4	7	Y	PIM-#2	Q18	U19-4A	00000 00001
		3	6	N	5	6	N				
7		2	5	N	6	5	Y		Q17		

		4	4	N	7	4	N				00010 00011
6		0	3	N	2	3	N		Q20		
		7	2	Y	1	2	Y				
5		5	1	N	0	1	N		Q19		
		6	0	Y	3	0	Y				
27	BC5	0	7	Y	7	7	N		Q22	U25-4B	00100 00101 00110 00111
		3	6	N	6	6	Y				
26		5	5	N	5	5	N		Q21		
		1	4	Y	4	4	Y				
25		7	3	N	3	3	Y		Q24		
		4	2	N	2	2	N				
24		2	1	Y	0	1	N		Q23		
		6	0	N	1	0	Y				
47	BC9	3	7	N	6	7	Y		Q26	U30-4C	01000 01001 01010 01011
		2	6	N	4	6	N				
46		0	5	N	5	5	Y		Q25		
		1	4	Y	0	4	Y				
45		5	3	N	1	3	N		Q28		
		4	2	N	7	2	Y				
44		7	1	N	2	1	Y		Q27		
		6	0	N	3	0	N				
67	BC13	2	7	Y	3	7	N		Q30	U22-4D	10000 10001 10010 10011
		3	6	Y	2	6	N				
66		0	5	N	1	5	Y		Q29		
		1	4	Y	0	4	N				
65		5	3	Y	6	3	Y		Q32		
		7	2	N	7	2	N				
64		4	1	Y	4	1	Y		Q31		
		6	0	N	5	0	N				
12	BC2	6	7	Y	1	7	N	PIM-#3	Q34	U19-4A	00000 00001 00010 00011
		7	6	N	0	6	Y				
11		4	5	N	2	5	Y		Q33		
		5	4	Y	3	4	N				
10		1	3	N	7	3	Y		Q36		

		0	2	Y	4	2	N				
9		3	1	N	5	1	Y		Q35		
		2	0	N	6	0	N				
31	BC6	6	7	Y	6	7	N		Q38	U25-4B	00100 00101 00110 00111
		7	6	Y	3	6	Y				
30		4	5	N	7	5	N		Q37		
		5	4	N	2	4	N				
29		0	3	Y	4	3	Y		Q40		
		2	2	Y	5	2	N				
28		1	1	N	1	1	Y		Q39		
		3	0	N	0	0	N				
51	BC10	6	7	Y	2	7	Y		Q42	U30-4C	01000 01001 01010 01011
		7	6	N	0	6	N				
50		5	5	Y	1	5	Y		Q41		
		4	4	N	3	4	Y				
49		0	3	Y	4	3	Y		Q44		
		1	2	N	5	2	N				
48		2	1	Y	6	1	Y		Q43		
		3	0	N	7	0	N				
71	BC14	6	7	Y	3	7	Y		Q46	U22-4D	10000 10001 10010 10011
		5	6	Y	2	6	Y				
70		7	5	N	4	5	N		Q45		
		0	4	Y	5	4	Y				
69		4	3	Y	1	3	N		Q48		
		2	2	Y	6	2	Y				
68		3	1	Y	0	1	Y		Q47		
		1	0	Y	7	0	N				
16	BC3	3	7	N	7	7	Y	PIM-#4	Q50	U19-4A	00000 00001 00010 00011
		6	6	Y	6	6	N				
15		0	5	N	2	5	N		Q49		
		1	4	Y	3	4	Y				
14		2	3	Y	1	3	Y		Q52		
		4	2	Y	5	2	Y				
13		5	1	N	0	1	Y		Q51		

		7	0	Y	4	0	N				
35	BC7	6	7	N	7	7	N		Q54	U25-4B	00100 00101 00110 00111
		2	6	N	4	6	Y				
34		7	5	Y	5	5	N		Q53		
		3	4	Y	0	4	N				
33		1	3	Y	1	3	N		Q56		
		0	2	N	6	2	N				
32		4	1	Y	2	1	Y		Q55		
		5	0	N	3	0	N				
55	BC11	6	7	N	3	7	N		Q58	U30-4C	01000 01001 01010 01011
		2	6	N	6	6	N				
54		4	5	Y	2	5	N		Q57		
		1	4	Y	7	4	Y				
53		3	3	Y	1	3	Y		Q60		
		5	2	N	5	2	Y				
52		0	1	Y	0	1	N		Q59		
		7	0	Y	4	0	N				
75	BC15	1	7	Y	1	7	Y		Q62	U22-4D	10000 10001 10010 10011
		7	6	Y	2	6	Y				
74		5	5	Y	3	5	N		Q61		
		2	4	N	0	4	Y				
73		6	3	N	4	3	N		Q64		
		4	2	N	5	2	Y				
72		0	1	Y	6	1	N		Q63		
		3	0	N	7	0	Y				
83	BC16	3	7	Y	7	7	N	PIM-#5	Q66	U19-4A	00000 00001 00010 00011
		2	6	N	0	6	N				
82		1	5	Y	4	5	Y		Q65		
		0	4	Y	5	4	N				
81		4	3	N	3	3	Y		Q68		
		6	2	N	2	2	N				
80		7	1	N	6	1	Y		Q67		
		5	0	N	1	0	Y				
103	BC20	1	7	N	0	7	Y		Q70		

		4	6	Y	4	6	N			
102		2	5	N	1	5	Y	Q69	U25-4B	00100 00101 00110 00111
		0	4	N	5	4	Y			
101		7	3	Y	2	3	N	Q72		
		6	2	Y	7	2	Y			
100		5	1	Y	3	1	Y	Q71		
		3	0	N	6	0	N			
123	BC24	4	7	Y	3	7	N	Q74	U30-4C	01000 01001 01010 01011
		1	6	Y	6	6	Y			
122		2	5	Y	2	5	N	Q73		
		0	4	N	7	4	N			
121		3	3	Y	1	3	Y	Q76		
		6	2	N	5	2	N			
120		7	1	N	0	1	N	Q75		
		5	0	N	4	0	Y			
143	BC28	6	7	Y	3	7	Y	Q78	U22-4D	10000 10001 10010 10011
		5	6	N	2	6	Y			
142		7	5	Y	1	5	N	Q77		
		0	4	Y	0	4	Y			
141		2	3	N	6	3	Y	Q80		
		1	2	N	7	2	N			
140		3	1	Y	4	1	Y	Q79		
		4	0	N	5	0	N			
87	BC17	2	7	Y	7	7	N	PIM-#6	Q82	U19-4A	00000 00001 00010 00011
		3	6	Y	3	6	Y			
86		4	5	N	6	5	Y		Q81		
		0	4	N	2	4	N			
85		7	3	N	5	3	N		Q84		
		6	2	Y	4	2	Y			
84		1	1	Y	1	1	Y		Q83		
		5	0	N	0	0	Y			
107	BC21	3	7	N	3	7	N		Q86	U25-4B	00100 00101
		0	6	N	7	6	Y			
106		2	5	Y	2	5	Y		Q85		

		4	4	Y	6	4	N				00110
105		6	3	Y	1	3	Y		Q88		00111
		7	2	Y	5	2	N				
104		5	1	Y	0	1	N		Q87		
		1	0	Y	4	0	Y				
127	BC25	3	7	N	6	7	Y		Q90	U30-4C	01000
		2	6	Y	4	6	N				01001
126		0	5	N	5	5	Y		Q89		01010
		4	4	Y	7	4	Y				01011
125		6	3	Y	0	3	Y		Q92		
		5	2	Y	1	2	N				
124		7	1	Y	2	1	Y		Q91		
		1	0	Y	3	0	N				
147	BC29	5	7	Y	7	7	Y		Q94	U22-4D	10000
		2	6	N	6	6	Y				10001
146		3	5	Y	4	5	Y		Q93		10010
		0	4	N	5	4	N				10011
145		1	3	Y	0	3	N		Q96		
		4	2	N	3	2	Y				
144		6	1	Y	2	1	N		Q95		
		7	0	N	1	0	Y				
91	BC18	7	7	Y	3	7	N	PIM-#7	Q98	U19-4A	00000
		6	6	N	2	6	Y				00001
90		5	5	Y	0	5	Y		Q97		00010
		4	4	Y	1	4	N				00011
89		0	3	N	6	3	N		Q100		
		1	2	Y	4	2	N				
88		3	1	N	5	1	Y		Q99		
		2	0	Y	7	0	Y				
111	BC22	6	7	Y	7	7	Y		Q102	U25-4B	00100
		7	6	Y	2	6	N				00101
110		5	5	N	5	5	N		Q101		00110
		0	4	Y	4	4	Y				00111
109		4	3	N	1	3	Y		Q104		

		3	2	N	0	2	N				
108		1	1	Y	6	1	Y		Q103		
		2	0	Y	3	0	Y				
131		5	7	N	3	7	N		Q106		
		6	6	N	7	6	N				
130		7	5	Y	0	5	N		Q105		
	BC26	0	4	Y	1	4	Y			U30-4C	01000 01001 01010 01011
129		4	3	N	4	3	Y		Q108		
		2	2	Y	5	2	N				
128		1	1	N	2	1	N		Q107		
		3	0	Y	6	0	Y				
151		6	7	Y	0	7	N		Q110		
		7	6	N	1	6	N				
150		5	5	N	2	5	Y		Q109		
	BC30	4	4	N	7	4	Y			U22-4D	10000 10001 10010 10011
149		0	3	N	6	3	N		Q112		
		1	2	N	5	2	Y				
148		2	1	Y	3	1	N		Q111		
		3	0	Y	4	0	N				
95		1	7	N	3	7	Y		Q114		
		3	6	Y	2	6	Y				
94		2	5	Y	1	5	N		Q113		
	BC19	0	4	Y	0	4	Y			U19-4A	00000 00001 00010 00011
93		5	3	N	6	3	N		Q116		
		7	2	Y	4	2	N				
92		4	1	N	5	1	Y		Q115		
		6	0	Y	7	0	Y	PIM-#8			
115		1	7	N	6	7	Y		Q118		
		5	6	N	4	6	Y				
114		2	5	N	5	5	N		Q117		
	BC23	4	4	N	7	4	N			U25-4B	00100 00101 00110 00111
113		7	3	N	0	3	Y		Q120		
		3	2	Y	1	2	N				
112		6	1	N	2	1	Y		Q119		

		0	0	N	3	0	N				
135	BC27	5	7	Y	6	7	Y		Q122	U30-4C	01000 01001 01010 01011
		3	6	Y	5	6	Y				
134		1	5	Y	0	5	Y		Q121		
		7	4	N	4	4	N				
133		4	3	Y	1	3	N		Q124		
		6	2	N	2	2	Y				
132		2	1	N	7	1	Y		Q123		
		0	0	N	3	0	N				
155	BC31	6	7	N	0	7	N		Q126	U22-4D	10000 10001 10010 10011
		7	6	Y	6	6	N				
154		5	5	Y	1	5	N		Q125		
		0	4	Y	5	4	Y				
153		1	3	Y	2	3	Y		Q128		
		3	2	Y	3	2	N				
152		4	1	Y	4	1	N		Q127		
		2	0	N	7	0	Y				

Table 13: Minipack TH3 to Gearbox Port Mapping

The following table show the QSFP28 port mapping inside PIM-16Q:

U19 (BCM81724)		Net name	Conn9	PN swap
P1	MTX_0P	NRZP13_0_TX_N	QSFP2	Y
R1	MTX_0N	NRZP13_0_TX_P		
L1	MRX_0P	NRZP13_0_RX_N		Y
M1	MRX_0N	NRZP13_0_RX_P		
U1	MTX_1P	NRZP13_1_TX_P		N
V1	MTX_1N	NRZP13_1_TX_N		
M3	MRX_1P	NRZP13_1_RX_P		N
N3	MRX_1N	NRZP13_1_RX_N		
Y1	MTX_2P	NRZP13_2_TX_N		Y
AA1	MTX_2N	NRZP13_2_TX_P		

R3	MRX_2P	NRZP13_2_RX_P		N
T3	MRX_2N	NRZP13_2_RX_N		
AA3	MTX_3P	NRZP13_3_TX_N		Y
AB3	MTX_3N	NRZP13_3_TX_P		
V3	MRX_3P	NRZP13_3_RX_P		N
W3	MRX_3N	NRZP13_3_RX_N		
AA5	MTX_4P	NRZP14_0_TX_N	QSFP3	Y
AB5	MTX_4N	NRZP14_0_TX_P		
V5	MRX_4P	NRZP14_0_RX_P		N
W5	MRX_4N	NRZP14_0_RX_N		
AA7	MTX_5P	NRZP14_1_TX_P		N
AB7	MTX_5N	NRZP14_1_TX_N		
V7	MRX_5P	NRZP14_1_RX_P		N
W7	MRX_5N	NRZP14_1_RX_N		
AA9	MTX_6P	NRZP14_2_TX_P		N
AB9	MTX_6N	NRZP14_2_TX_N		
V9	MRX_6P	NRZP14_2_RX_P		N
W9	MRX_6N	NRZP14_2_RX_N		
AA11	MTX_7P	NRZP14_3_TX_P		N
AB11	MTX_7N	NRZP14_3_TX_N		
V11	MRX_7P	NRZP14_3_RX_P		N
W11	MRX_7N	NRZP14_3_RX_N		
AA13	MTX_8P	NRZP15_0_TX_N	QSFP0	Y
AB13	MTX_8N	NRZP15_0_TX_P		
V13	MRX_8P	NRZP15_0_RX_P		N
W13	MRX_8N	NRZP15_0_RX_N		
AA15	MTX_9P	NRZP15_1_TX_N		Y
AB15	MTX_9N	NRZP15_1_TX_P		
V15	MRX_9P	NRZP15_1_RX_N		Y
W15	MRX_9N	NRZP15_1_RX_P		
AA17	MTX_10P	NRZP15_2_TX_N		Y
AB17	MTX_10N	NRZP15_2_TX_P		
V17	MRX_10P	NRZP15_2_RX_N		Y
W17	MRX_10N	NRZP15_2_RX_P		
AA19	MTX_11P	NRZP15_3_TX_N		Y
AB19	MTX_11N	NRZP15_3_TX_P		

W19	MRX_11P	NRZP15_3_RX_N		Y
W20	MRX_11N	NRZP15_3_RX_P		
AA21	MTX_12P	NRZP16_0_TX_P	QSFP1	N
AB21	MTX_12N	NRZP16_0_TX_N		
U19	MRX_12P	NRZP16_0_RX_N		Y
U20	MRX_12N	NRZP16_0_RX_P		
V22	MTX_13P	NRZP16_1_TX_P		N
W22	MTX_13N	NRZP16_1_TX_N		
R19	MRX_13P	NRZP16_1_RX_P		N
R20	MRX_13N	NRZP16_1_RX_N		
R22	MTX_14P	NRZP16_2_TX_P		N
T22	MTX_14N	NRZP16_2_TX_N		
M19	MRX_14P	NRZP16_2_RX_N		Y
N19	MRX_14N	NRZP16_2_RX_P		
N21	MTX_15P	NRZP16_3_TX_P		N
N22	MTX_15N	NRZP16_3_TX_N		
L21	MRX_15P	NRZP16_3_RX_P		N
L22	MRX_15N	NRZP16_3_RX_N		
U25 (BCM81724)		**Net name**	**Conn 7 & 9**	**PN swap**
P1	MTX_0P	NRZP9_0_TX_N	QSFP6	Y
R1	MTX_0N	NRZP9_0_TX_P		
L1	MRX_0P	NRZP9_0_RX_N		Y
M1	MRX_0N	NRZP9_0_RX_P		
U1	MTX_1P	NRZP9_1_TX_N		Y
V1	MTX_1N	NRZP9_1_TX_P		
M3	MRX_1P	NRZP9_1_RX_P		N
N3	MRX_1N	NRZP9_1_RX_N		
Y1	MTX_2P	NRZP9_2_TX_N		Y
AA1	MTX_2N	NRZP9_2_TX_P		
R3	MRX_2P	NRZP9_2_RX_P		N
T3	MRX_2N	NRZP9_2_RX_N		
AA3	MTX_3P	NRZP9_3_TX_N		Y
AB3	MTX_3N	NRZP9_3_TX_P		
V3	MRX_3P	NRZP9_3_RX_P		N
W3	MRX_3N	NRZP9_3_RX_N		
AA5	MTX_4P	NRZP10_0_TX_N	QSFP7	Y

AB5	MTX_4N	NRZP10_0_TX_P		
V5	MRX_4P	NRZP10_0_RX_P		N
W5	MRX_4N	NRZP10_0_RX_N		
AA7	MTX_5P	NRZP10_1_TX_P		N
AB7	MTX_5N	NRZP10_1_TX_N		
V7	MRX_5P	NRZP10_1_RX_P		N
W7	MRX_5N	NRZP10_1_RX_N		
AA9	MTX_6P	NRZP10_2_TX_P		N
AB9	MTX_6N	NRZP10_2_TX_N		
V9	MRX_6P	NRZP10_2_RX_P		N
W9	MRX_6N	NRZP10_2_RX_N		
AA11	MTX_7P	NRZP10_3_TX_P		N
AB11	MTX_7N	NRZP10_3_TX_N		
V11	MRX_7P	NRZP10_3_RX_P		N
W11	MRX_7N	NRZP10_3_RX_N		
AA13	MTX_8P	NRZP11_0_TX_N	QSFP4	Y
AB13	MTX_8N	NRZP11_0_TX_P		
V13	MRX_8P	NRZP11_0_RX_N		Y
W13	MRX_8N	NRZP11_0_RX_P		
AA15	MTX_9P	NRZP11_1_TX_P		N
AB15	MTX_9N	NRZP11_1_TX_N		
V15	MRX_9P	NRZP11_1_RX_N		Y
W15	MRX_9N	NRZP11_1_RX_P		
AA17	MTX_10P	NRZP11_2_TX_N		Y
AB17	MTX_10N	NRZP11_2_TX_P		
V17	MRX_10P	NRZP11_2_RX_N		Y
W17	MRX_10N	NRZP11_2_RX_P		
AA19	MTX_11P	NRZP11_3_TX_N		Y
AB19	MTX_11N	NRZP11_3_TX_P		
W19	MRX_11P	NRZP11_3_RX_N		Y
W20	MRX_11N	NRZP11_3_RX_P		
AA21	MTX_12P	NRZP12_0_TX_P	QSFP5	N
AB21	MTX_12N	NRZP12_0_TX_N		
U19	MRX_12P	NRZP12_0_RX_N		Y
U20	MRX_12N	NRZP12_0_RX_P		
V22	MTX_13P	NRZP12_1_TX_P		N

W22	MTX_13N	NRZP12_1_TX_N		
R19	MRX_13P	NRZP12_1_RX_N		Y
R20	MRX_13N	NRZP12_1_RX_P		
R22	MTX_14P	NRZP12_2_TX_P		N
T22	MTX_14N	NRZP12_2_TX_N		
M19	MRX_14P	NRZP12_2_RX_N		Y
N19	MRX_14N	NRZP12_2_RX_P		
N21	MTX_15P	NRZP12_3_TX_P		N
N22	MTX_15N	NRZP12_3_TX_N		
L21	MRX_15P	NRZP12_3_RX_N		Y
L22	MRX_15N	NRZP12_3_RX_P		
U30 (BCM81724)		**Net name**	**Conn 8 & 7**	**PN swap**
P1	MTX_0P	NRZP5_0_TX_N	QSFP10	Y
R1	MTX_0N	NRZP5_0_TX_P		
L1	MRX_0P	NRZP5_0_RX_N		Y
M1	MRX_0N	NRZP5_0_RX_P		
U1	MTX_1P	NRZP5_1_TX_N		Y
V1	MTX_1N	NRZP5_1_TX_P		
M3	MRX_1P	NRZP5_1_RX_P		N
N3	MRX_1N	NRZP5_1_RX_N		
Y1	MTX_2P	NRZP5_2_TX_N		Y
AA1	MTX_2N	NRZP5_2_TX_P		
R3	MRX_2P	NRZP5_2_RX_P		N
T3	MRX_2N	NRZP5_2_RX_N		
AA3	MTX_3P	NRZP5_3_TX_N		Y
AB3	MTX_3N	NRZP5_3_TX_P		
V3	MRX_3P	NRZP5_3_RX_N		Y
W3	MRX_3N	NRZP5_3_RX_P		
AA5	MTX_4P	NRZP6_0_TX_N	QSFP11	Y
AB5	MTX_4N	NRZP6_0_TX_P		
V5	MRX_4P	NRZP6_0_RX_P		N
W5	MRX_4N	NRZP6_0_RX_N		
AA7	MTX_5P	NRZP6_1_TX_P		N
AB7	MTX_5N	NRZP6_1_TX_N		
V7	MRX_5P	NRZP6_1_RX_P		N
W7	MRX_5N	NRZP6_1_RX_N		

AA9	MTX_6P	NRZP6_2_TX_P		N
AB9	MTX_6N	NRZP6_2_TX_N		
V9	MRX_6P	NRZP6_2_RX_P		N
W9	MRX_6N	NRZP6_2_RX_N		
AA11	MTX_7P	NRZP6_3_TX_P		N
AB11	MTX_7N	NRZP6_3_TX_N		
V11	MRX_7P	NRZP6_3_RX_P		N
W11	MRX_7N	NRZP6_3_RX_N		
AA13	MTX_8P	NRZP7_0_TX_N	QSFP8	Y
AB13	MTX_8N	NRZP7_0_TX_P		
V13	MRX_8P	NRZP7_0_RX_N		Y
W13	MRX_8N	NRZP7_0_RX_P		
AA15	MTX_9P	NRZP7_1_TX_P		N
AB15	MTX_9N	NRZP7_1_TX_N		
V15	MRX_9P	NRZP7_1_RX_N		Y
W15	MRX_9N	NRZP7_1_RX_P		
AA17	MTX_10P	NRZP7_2_TX_N		Y
AB17	MTX_10N	NRZP7_2_TX_P		
V17	MRX_10P	NRZP7_2_RX_N		Y
W17	MRX_10N	NRZP7_2_RX_P		
AA19	MTX_11P	NRZP7_3_TX_N		Y
AB19	MTX_11N	NRZP7_3_TX_P		
W19	MRX_11P	NRZP7_3_RX_N		Y
W20	MRX_11N	NRZP7_3_RX_P		
AA21	MTX_12P	NRZP8_0_TX_P	QSFP9	N
AB21	MTX_12N	NRZP8_0_TX_N		
U19	MRX_12P	NRZP8_0_RX_N		Y
U20	MRX_12N	NRZP8_0_RX_P		
V22	MTX_13P	NRZP8_1_TX_P		N
W22	MTX_13N	NRZP8_1_TX_N		
R19	MRX_13P	NRZP8_1_RX_P		N
R20	MRX_13N	NRZP8_1_RX_N		
R22	MTX_14P	NRZP8_2_TX_P		N
T22	MTX_14N	NRZP8_2_TX_N		
M19	MRX_14P	NRZP8_2_RX_N		Y
N19	MRX_14N	NRZP8_2_RX_P		

N21	MTX_15P	NRZP8_3_TX_P		N
N22	MTX_15N	NRZP8_3_TX_N		
L21	MRX_15P	NRZP8_3_RX_P		N
L22	MRX_15N	NRZP8_3_RX_N		
U22 (BCM81724)		**Net name**	**Conn8**	**PN swap**
P1	MTX_0P	NRZP1_0_TX_N	QSFP14	Y
R1	MTX_0N	NRZP1_0_TX_P		
L1	MRX_0P	NRZP1_0_RX_N		Y
M1	MRX_0N	NRZP1_0_RX_P		
U1	MTX_1P	NRZP1_1_TX_N		Y
V1	MTX_1N	NRZP1_1_TX_P		
M3	MRX_1P	NRZP1_1_RX_P		N
N3	MRX_1N	NRZP1_1_RX_N		
Y1	MTX_2P	NRZP1_2_TX_N		Y
AA1	MTX_2N	NRZP1_2_TX_P		
R3	MRX_2P	NRZP1_2_RX_P		N
T3	MRX_2N	NRZP1_2_RX_N		
AA3	MTX_3P	NRZP1_3_TX_N		Y
AB3	MTX_3N	NRZP1_3_TX_P		
V3	MRX_3P	NRZP1_3_RX_N		Y
W3	MRX_3N	NRZP1_3_RX_P		
AA5	MTX_4P	NRZP2_0_TX_N	QSFP15	Y
AB5	MTX_4N	NRZP2_0_TX_P		
V5	MRX_4P	NRZP2_0_RX_P		N
W5	MRX_4N	NRZP2_0_RX_N		
AA7	MTX_5P	NRZP2_1_TX_P		N
AB7	MTX_5N	NRZP2_1_TX_N		
V7	MRX_5P	NRZP2_1_RX_P		N
W7	MRX_5N	NRZP2_1_RX_N		
AA9	MTX_6P	NRZP2_2_TX_P		N
AB9	MTX_6N	NRZP2_2_TX_N		
V9	MRX_6P	NRZP2_2_RX_P		N
W9	MRX_6N	NRZP2_2_RX_N		
AA11	MTX_7P	NRZP2_3_TX_P		N
AB11	MTX_7N	NRZP2_3_TX_N		
V11	MRX_7P	NRZP2_3_RX_P		N

W11	MRX_7N	NRZP2_3_RX_N		
AA13	MTX_8P	NRZP3_0_TX_N	QSFP12	Y
AB13	MTX_8N	NRZP3_0_TX_P		
V13	MRX_8P	NRZP3_0_RX_N		Y
W13	MRX_8N	NRZP3_0_RX_P		
AA15	MTX_9P	NRZP3_1_TX_P		N
AB15	MTX_9N	NRZP3_1_TX_N		
V15	MRX_9P	NRZP3_1_RX_N		Y
W15	MRX_9N	NRZP3_1_RX_P		
AA17	MTX_10P	NRZP3_2_TX_N		Y
AB17	MTX_10N	NRZP3_2_TX_P		
V17	MRX_10P	NRZP3_2_RX_N		Y
W17	MRX_10N	NRZP3_2_RX_P		
AA19	MTX_11P	NRZP3_3_TX_N		Y
AB19	MTX_11N	NRZP3_3_TX_P		
W19	MRX_11P	NRZP3_3_RX_N		Y
W20	MRX_11N	NRZP3_3_RX_P		
AA21	MTX_12P	NRZP4_0_TX_P	QSFP13	N
AB21	MTX_12N	NRZP4_0_TX_N		
U19	MRX_12P	NRZP4_0_RX_N		Y
U20	MRX_12N	NRZP4_0_RX_P		
V22	MTX_13P	NRZP4_1_TX_P		N
W22	MTX_13N	NRZP4_1_TX_N		
R19	MRX_13P	NRZP4_1_RX_P		N
R20	MRX_13N	NRZP4_1_RX_N		
R22	MTX_14P	NRZP4_2_TX_P		N
T22	MTX_14N	NRZP4_2_TX_N		
M19	MRX_14P	NRZP4_2_RX_N		Y
N19	MRX_14N	NRZP4_2_RX_P		
N21	MTX_15P	NRZP4_3_TX_P		N
N22	MTX_15N	NRZP4_3_TX_N		
L21	MRX_15P	NRZP4_3_RX_P		N
L22	MRX_15N	NRZP4_3_RX_N		

Table 14: PIM-16Q Gearbox and QSFP28 Port Mapping

9.2.2.3 Port Mapping of PIM-4DD to SMB

The following table shows the port mapping of Tomahawk3 ASIC SERDES and retimer ports of PIM-4DD.

			TH3 TX			TH3 RX		
PIM	PIM Port	Loc	Net name (SMB)	Net name (4DD)	BCM81328 pin name	Net name (SMB)	Net name (4DD)	BCM81328 pin name
PIM-#1	Q1	U14-4A	OD1_BC0_TX3_N	PAM4A_0_RX_N	HRX_7P	OD1_BC0_RX3_N	PAM4A_0_TX_N	HTX_7P
			OD1_BC0_TX2_P	PAM4A_1_RX_N	HRX_6P	OD1_BC0_RX2_N	PAM4A_1_TX_N	HTX_6P
			OD1_BC0_TX0_P	PAM4A_2_RX_N	HRX_5P	OD1_BC0_RX1_P	PAM4A_2_TX_N	HTX_5P
			OD1_BC0_TX4_N	PAM4A_3_RX_N	HRX_4P	OD1_BC0_RX4_P	PAM4A_3_TX_N	HTX_4P
			OD1_BC0_TX6_N	PAM4A_4_RX_N	HRX_3P	OD1_BC0_RX5_N	PAM4A_4_TX_N	HTX_3P
			OD1_BC0_TX7_P	PAM4A_5_RX_N	HRX_2P	OD1_BC0_RX6_P	PAM4A_5_TX_N	HTX_2P
			OD1_BC0_TX5_P	PAM4A_6_RX_N	HRX_1P	OD1_BC0_RX7_N	PAM4A_6_TX_N	HTX_1P
			OD1_BC0_TX1_N	PAM4A_7_RX_N	HRX_0P	OD1_BC0_RX0_N	PAM4A_7_TX_N	HTX_0P
	Q2	U19-4B	OD1_BC4_TX5_P	PAM4B_0_RX_N	HRX_7P	OD1_BC4_RX5_N	PAM4B_0_TX_N	HTX_7P
			OD1_BC4_TX6_N	PAM4B_1_RX_N	HRX_6P	OD1_BC4_RX6_N	PAM4B_1_TX_N	HTX_6P
			OD1_BC4_TX1_N	PAM4B_2_RX_N	HRX_5P	OD1_BC4_RX3_N	PAM4B_2_TX_N	HTX_5P
			OD1_BC4_TX0_P	PAM4B_3_RX_N	HRX_4P	OD1_BC4_RX2_P	PAM4B_3_TX_N	HTX_4P
			OD1_BC4_TX3_N	PAM4B_4_RX_P	HRX_3N	OD1_BC4_RX1_N	PAM4B_4_TX_P	HTX_3N
			OD1_BC4_TX2_P	PAM4B_5_RX_P	HRX_2N	OD1_BC4_RX0_P	PAM4B_5_TX_P	HTX_2N
			OD1_BC4_TX4_N	PAM4B_6_RX_P	HRX_1N	OD1_BC4_RX7_P	PAM4B_6_TX_P	HTX_1N
			OD1_BC4_TX7_P	PAM4B_7_RX_P	HRX_0N	OD1_BC4_RX4_N	PAM4B_7_TX_P	HTX_0N
	Q3	U21-4C	OD1_BC8_TX4_P	PAM4C_0_RX_P	HRX_7N	OD1_BC8_RX7_N	PAM4C_0_TX_P	HTX_7N
			OD1_BC8_TX5_N	PAM4C_1_RX_P	HRX_6N	OD1_BC8_RX3_P	PAM4C_1_TX_P	HTX_6N
			OD1_BC8_TX2_N	PAM4C_2_RX_P	HRX_5N	OD1_BC8_RX2_N	PAM4C_2_TX_P	HTX_5N
			OD1_BC8_TX1_P	PAM4C_3_RX_P	HRX_4N	OD1_BC8_RX1_P	PAM4C_3_TX_P	HTX_4N
			OD1_BC8_TX3_N	PAM4C_4_RX_P	HRX_3N	OD1_BC8_RX0_N	PAM4C_4_TX_P	HTX_3N
			OD1_BC8_TX0_N	PAM4C_5_RX_P	HRX_2N	OD1_BC8_RX6_P	PAM4C_5_TX_P	HTX_2N
			OD1_BC8_TX7_P	PAM4C_6_RX_P	HRX_1N	OD1_BC8_RX4_P	PAM4C_6_TX_P	HTX_1N
			OD1_BC8_TX6_N	PAM4C_7_RX_P	HRX_0N	OD1_BC8_RX5_P	PAM4C_7_TX_P	HTX_0N
	Q4		OD1_BC12_TX7_N	PAM4D_0_RX_N	HRX_7P	OD1_BC12_RX1_P	PAM4D_0_TX_P	HTX_7N

		U17-4D	OD1_BC12_TX5_P	PAM4D_1_RX_P	HRX_6N	OD1_BC12_RX0_N	PAM4D_1_TX_P	HTX_6N
			OD1_BC12_TX4_N	PAM4D_2_RX_P	HRX_5N	OD1_BC12_RX2_P	PAM4D_2_TX_P	HTX_5N
			OD1_BC12_TX6_P	PAM4D_3_RX_P	HRX_4N	OD1_BC12_RX3_N	PAM4D_3_TX_P	HTX_4N
			OD1_BC12_TX2_P	PAM4D_4_RX_P	HRX_3N	OD1_BC12_RX4_N	PAM4D_4_TX_P	HTX_3N
			OD1_BC12_TX1_P	PAM4D_5_RX_P	HRX_2N	OD1_BC12_RX5_P	PAM4D_5_TX_P	HTX_2N
			OD1_BC12_TX0_N	PAM4D_6_RX_P	HRX_1N	OD1_BC12_RX6_N	PAM4D_6_TX_P	HTX_1N
			OD1_BC12_TX3_P	PAM4D_7_RX_N	HRX_0P	OD1_BC12_RX7_P	PAM4D_7_TX_P	HTX_0N
PIM-#2	Q5	U14-4A	OD2_BC1_TX1_P	PAM4A_0_RX_N	HRX_7P	OD2_BC1_RX4_P	PAM4A_0_TX_N	HTX_7P
			OD2_BC1_TX3_P	PAM4A_1_RX_N	HRX_6P	OD2_BC1_RX5_P	PAM4A_1_TX_N	HTX_6P
			OD2_BC1_TX2_P	PAM4A_2_RX_N	HRX_5P	OD2_BC1_RX6_N	PAM4A_2_TX_N	HTX_5P
			OD2_BC1_TX4_P	PAM4A_3_RX_N	HRX_4P	OD2_BC1_RX7_N	PAM4A_3_TX_N	HTX_4P
			OD2_BC1_TX0_P	PAM4A_4_RX_N	HRX_3P	OD2_BC1_RX3_N	PAM4A_4_TX_N	HTX_3P
			OD2_BC1_TX7_N	PAM4A_5_RX_N	HRX_2P	OD2_BC1_RX0_N	PAM4A_5_TX_N	HTX_2P
			OD2_BC1_TX5_P	PAM4A_6_RX_N	HRX_1P	OD2_BC1_RX2_N	PAM4A_6_TX_N	HTX_1P
			OD2_BC1_TX6_N	PAM4A_7_RX_N	HRX_0P	OD2_BC1_RX1_P	PAM4A_7_TX_N	HTX_0P
	Q6	U19-4B	OD2_BC5_TX3_P	PAM4B_0_RX_N	HRX_7P	OD2_BC5_RX7_P	PAM4B_0_TX_N	HTX_7P
			OD2_BC5_TX0_P	PAM4B_1_RX_N	HRX_6P	OD2_BC5_RX6_P	PAM4B_1_TX_N	HTX_6P
			OD2_BC5_TX1_P	PAM4B_2_RX_N	HRX_5P	OD2_BC5_RX5_N	PAM4B_2_TX_N	HTX_5P
			OD2_BC5_TX2_N	PAM4B_3_RX_N	HRX_4P	OD2_BC5_RX4_P	PAM4B_3_TX_N	HTX_4P
			OD2_BC5_TX5_N	PAM4B_4_RX_P	HRX_3N	OD2_BC5_RX3_P	PAM4B_4_TX_P	HTX_3N
			OD2_BC5_TX4_P	PAM4B_5_RX_P	HRX_2N	OD2_BC5_RX2_N	PAM4B_5_TX_P	HTX_2N
			OD2_BC5_TX7_N	PAM4B_6_RX_P	HRX_1N	OD2_BC5_RX1_P	PAM4B_6_TX_P	HTX_1N
			OD2_BC5_TX6_P	PAM4B_7_RX_P	HRX_0N	OD2_BC5_RX0_N	PAM4B_7_TX_P	HTX_0N
	Q7	U21-4C	OD2_BC9_TX3_N	PAM4C_0_RX_P	HRX_7N	OD2_BC9_RX6_P	PAM4C_0_TX_P	HTX_7N
			OD2_BC9_TX1_P	PAM4C_1_RX_P	HRX_6N	OD2_BC9_RX7_N	PAM4C_1_TX_P	HTX_6N
			OD2_BC9_TX0_P	PAM4C_2_RX_P	HRX_5N	OD2_BC9_RX5_N	PAM4C_2_TX_P	HTX_5N
			OD2_BC9_TX2_P	PAM4C_3_RX_P	HRX_4N	OD2_BC9_RX4_P	PAM4C_3_TX_P	HTX_4N
			OD2_BC9_TX5_P	PAM4C_4_RX_P	HRX_3N	OD2_BC9_RX3_P	PAM4C_4_TX_P	HTX_3N
			OD2_BC9_TX4_N	PAM4C_5_RX_P	HRX_2N	OD2_BC9_RX2_N	PAM4C_5_TX_P	HTX_2N
			OD2_BC9_TX7_P	PAM4C_6_RX_P	HRX_1N	OD2_BC9_RX0_P	PAM4C_6_TX_P	HTX_1N
			OD2_BC9_TX6_N	PAM4C_7_RX_P	HRX_0N	OD2_BC9_RX1_N	PAM4C_7_TX_P	HTX_0N
	Q8	U17-4D	OD2_BC13_TX2_N	PAM4D_0_RX_N	HRX_7P	OD2_BC13_RX3_N	PAM4D_0_TX_P	HTX_7N
			OD2_BC13_TX3_P	PAM4D_1_RX_P	HRX_6N	OD2_BC13_RX2_P	PAM4D_1_TX_P	HTX_6N
			OD2_BC13_TX0_N	PAM4D_2_RX_P	HRX_5N	OD2_BC13_RX1_N	PAM4D_2_TX_P	HTX_5N
			OD2_BC13_TX1_P	PAM4D_3_RX_P	HRX_4N	OD2_BC13_RX0_P	PAM4D_3_TX_P	HTX_4N

			OD2_BC13_TX5_P	PAM4D_4_RX_P	HRX_3N	OD2_BC13_RX6_P	PAM4D_4_TX_P	HTX_3N
			OD2_BC13_TX7_P	PAM4D_5_RX_P	HRX_2N	OD2_BC13_RX7_N	PAM4D_5_TX_P	HTX_2N
			OD2_BC13_TX4_N	PAM4D_6_RX_P	HRX_1N	OD2_BC13_RX4_P	PAM4D_6_TX_P	HTX_1N
			OD2_BC13_TX6_N	PAM4D_7_RX_N	HRX_0P	OD2_BC13_RX5_P	PAM4D_7_TX_P	HTX_0N
PIM-#3	**Q9**	U14-4A	OD3_BC2_TX6_N	PAM4A_0_RX_N	HRX_7P	OD3_BC2_RX0_P	PAM4A_0_TX_N	HTX_7P
			OD3_BC2_TX7_P	PAM4A_1_RX_N	HRX_6P	OD3_BC2_RX1_N	PAM4A_1_TX_N	HTX_6P
			OD3_BC2_TX4_N	PAM4A_2_RX_N	HRX_5P	OD3_BC2_RX2_P	PAM4A_2_TX_N	HTX_5P
			OD3_BC2_TX5_P	PAM4A_3_RX_N	HRX_4P	OD3_BC2_RX3_N	PAM4A_3_TX_N	HTX_4P
			OD3_BC2_TX1_N	PAM4A_4_RX_N	HRX_3P	OD3_BC2_RX4_P	PAM4A_4_TX_N	HTX_3P
			OD3_BC2_TX0_P	PAM4A_5_RX_N	HRX_2P	OD3_BC2_RX5_P	PAM4A_5_TX_N	HTX_2P
			OD3_BC2_TX3_N	PAM4A_6_RX_N	HRX_1P	OD3_BC2_RX7_P	PAM4A_6_TX_N	HTX_1P
			OD3_BC2_TX2_P	PAM4A_7_RX_N	HRX_0P	OD3_BC2_RX6_N	PAM4A_7_TX_N	HTX_0P
	Q10	U19-4B	OD3_BC6_TX0_N	PAM4B_0_RX_N	HRX_7P	OD3_BC6_RX6_P	PAM4B_0_TX_N	HTX_7P
			OD3_BC6_TX7_N	PAM4B_1_RX_N	HRX_6P	OD3_BC6_RX1_P	PAM4B_1_TX_N	HTX_6P
			OD3_BC6_TX5_N	PAM4B_2_RX_N	HRX_5P	OD3_BC6_RX0_N	PAM4B_2_TX_N	HTX_5P
			OD3_BC6_TX4_P	PAM4B_3_RX_N	HRX_4P	OD3_BC6_RX2_N	PAM4B_3_TX_N	HTX_4P
			OD3_BC6_TX1_P	PAM4B_4_RX_P	HRX_3N	OD3_BC6_RX3_N	PAM4B_4_TX_P	HTX_3N
			OD3_BC6_TX2_N	PAM4B_5_RX_P	HRX_2N	OD3_BC6_RX5_N	PAM4B_5_TX_P	HTX_2N
			OD3_BC6_TX6_N	PAM4B_6_RX_P	HRX_1N	OD3_BC6_RX4_N	PAM4B_6_TX_P	HTX_1N
			OD3_BC6_TX3_P	PAM4B_7_RX_P	HRX_0N	OD3_BC6_RX7_P	PAM4B_7_TX_P	HTX_0N
	Q11	U21-4C	OD3_BC10_TX6_N	PAM4C_0_RX_P	HRX_7N	OD3_BC10_RX7_P	PAM4C_0_TX_P	HTX_7N
			OD3_BC10_TX7_P	PAM4C_1_RX_P	HRX_6N	OD3_BC10_RX0_P	PAM4C_1_TX_P	HTX_6N
			OD3_BC10_TX5_P	PAM4C_2_RX_P	HRX_5N	OD3_BC10_RX1_P	PAM4C_2_TX_P	HTX_5N
			OD3_BC10_TX4_N	PAM4C_3_RX_P	HRX_4N	OD3_BC10_RX2_N	PAM4C_3_TX_P	HTX_4N
			OD3_BC10_TX1_N	PAM4C_4_RX_P	HRX_3N	OD3_BC10_RX4_P	PAM4C_4_TX_P	HTX_3N
			OD3_BC10_TX2_P	PAM4C_5_RX_P	HRX_2N	OD3_BC10_RX3_P	PAM4C_5_TX_P	HTX_2N
			OD3_BC10_TX0_N	PAM4C_6_RX_P	HRX_1N	OD3_BC10_RX5_N	PAM4C_6_TX_P	HTX_1N
			OD3_BC10_TX3_N	PAM4C_7_RX_P	HRX_0N	OD3_BC10_RX6_P	PAM4C_7_TX_P	HTX_0N
	Q12	U17-4D	OD3_BC14_TX6_P	PAM4D_0_RX_N	HRX_7P	OD3_BC14_RX2_P	PAM4D_0_TX_P	HTX_7N
			OD3_BC14_TX5_N	PAM4D_1_RX_P	HRX_6N	OD3_BC14_RX3_N	PAM4D_1_TX_P	HTX_6N
			OD3_BC14_TX7_P	PAM4D_2_RX_P	HRX_5N	OD3_BC14_RX1_P	PAM4D_2_TX_P	HTX_5N
			OD3_BC14_TX0_N	PAM4D_3_RX_P	HRX_4N	OD3_BC14_RX0_N	PAM4D_3_TX_P	HTX_4N
			OD3_BC14_TX4_N	PAM4D_4_RX_P	HRX_3N	OD3_BC14_RX4_N	PAM4D_4_TX_P	HTX_3N
			OD3_BC14_TX2_N	PAM4D_5_RX_P	HRX_2N	OD3_BC14_RX5_N	PAM4D_5_TX_P	HTX_2N
			OD3_BC14_TX3_N	PAM4D_6_RX_P	HRX_1N	OD3_BC14_RX6_P	PAM4D_6_TX_P	HTX_1N

			OD3_BC14_TX1_N	PAM4D_7_RX_N	HRX_0P	OD3_BC14_RX7_N	PAM4D_7_TX_P	HTX_0N
PIM-#4	Q13	U14-4A	OD4_BC3_TX3_P	PAM4A_0_RX_N	HRX_7P	OD4_BC3_RX4_N	PAM4A_0_TX_N	HTX_7P
			OD4_BC3_TX0_P	PAM4A_1_RX_N	HRX_6P	OD4_BC3_RX5_N	PAM4A_1_TX_N	HTX_6P
			OD4_BC3_TX1_N	PAM4A_2_RX_N	HRX_5P	OD4_BC3_RX0_N	PAM4A_2_TX_N	HTX_5P
			OD4_BC3_TX2_P	PAM4A_3_RX_N	HRX_4P	OD4_BC3_RX1_P	PAM4A_3_TX_N	HTX_4P
			OD4_BC3_TX6_N	PAM4A_4_RX_N	HRX_3P	OD4_BC3_RX7_N	PAM4A_4_TX_N	HTX_3P
			OD4_BC3_TX5_P	PAM4A_5_RX_N	HRX_2P	OD4_BC3_RX2_N	PAM4A_5_TX_N	HTX_2P
			OD4_BC3_TX4_P	PAM4A_6_RX_N	HRX_1P	OD4_BC3_RX6_N	PAM4A_6_TX_N	HTX_1P
			OD4_BC3_TX7_P	PAM4A_7_RX_N	HRX_0P	OD4_BC3_RX3_P	PAM4A_7_TX_N	HTX_0P
	Q14	U19-4B	OD4_BC7_TX7_P	PAM4B_0_RX_N	HRX_7P	OD4_BC7_RX4_P	PAM4B_0_TX_N	HTX_7P
			OD4_BC7_TX6_N	PAM4B_1_RX_N	HRX_6P	OD4_BC7_RX5_P	PAM4B_1_TX_N	HTX_6P
			OD4_BC7_TX2_P	PAM4B_2_RX_N	HRX_5P	OD4_BC7_RX6_N	PAM4B_2_TX_N	HTX_5P
			OD4_BC7_TX3_N	PAM4B_3_RX_N	HRX_4P	OD4_BC7_RX0_N	PAM4B_3_TX_N	HTX_4P
			OD4_BC7_TX1_N	PAM4B_4_RX_P	HRX_3N	OD4_BC7_RX1_P	PAM4B_4_TX_P	HTX_3N
			OD4_BC7_TX0_P	PAM4B_5_RX_P	HRX_2N	OD4_BC7_RX2_N	PAM4B_5_TX_P	HTX_2N
			OD4_BC7_TX4_N	PAM4B_6_RX_P	HRX_1N	OD4_BC7_RX7_N	PAM4B_6_TX_P	HTX_1N
			OD4_BC7_TX5_P	PAM4B_7_RX_P	HRX_0N	OD4_BC7_RX3_P	PAM4B_7_TX_P	HTX_0N
	Q15	U21-4C	OD4_BC11_TX6_P	PAM4C_0_RX_P	HRX_7N	OD4_BC11_RX4_N	PAM4C_0_TX_P	HTX_7N
			OD4_BC11_TX2_N	PAM4C_1_RX_P	HRX_6N	OD4_BC11_RX5_P	PAM4C_1_TX_P	HTX_6N
			OD4_BC11_TX3_P	PAM4C_2_RX_P	HRX_5N	OD4_BC11_RX0_P	PAM4C_2_TX_P	HTX_5N
			OD4_BC11_TX1_P	PAM4C_3_RX_P	HRX_4N	OD4_BC11_RX1_N	PAM4C_3_TX_P	HTX_4N
			OD4_BC11_TX0_N	PAM4C_4_RX_P	HRX_3N	OD4_BC11_RX7_P	PAM4C_4_TX_P	HTX_3N
			OD4_BC11_TX4_P	PAM4C_5_RX_P	HRX_2N	OD4_BC11_RX2_P	PAM4C_5_TX_P	HTX_2N
			OD4_BC11_TX5_N	PAM4C_6_RX_P	HRX_1N	OD4_BC11_RX6_N	PAM4C_6_TX_P	HTX_1N
			OD4_BC11_TX7_P	PAM4C_7_RX_P	HRX_0N	OD4_BC11_RX3_N	PAM4C_7_TX_P	HTX_0N
	Q16	U17-4D	OD4_BC15_TX1_P	PAM4D_0_RX_N	HRX_7P	OD4_BC15_RX3_N	PAM4D_0_TX_P	HTX_7N
			OD4_BC15_TX5_N	PAM4D_1_RX_P	HRX_6N	OD4_BC15_RX2_N	PAM4D_1_TX_P	HTX_6N
			OD4_BC15_TX7_N	PAM4D_2_RX_P	HRX_5N	OD4_BC15_RX1_P	PAM4D_2_TX_P	HTX_5N
			OD4_BC15_TX6_P	PAM4D_3_RX_P	HRX_4N	OD4_BC15_RX4_P	PAM4D_3_TX_P	HTX_4N
			OD4_BC15_TX4_P	PAM4D_4_RX_P	HRX_3N	OD4_BC15_RX5_N	PAM4D_4_TX_P	HTX_3N
			OD4_BC15_TX0_N	PAM4D_5_RX_P	HRX_2N	OD4_BC15_RX6_P	PAM4D_5_TX_P	HTX_2N
			OD4_BC15_TX2_N	PAM4D_6_RX_P	HRX_1N	OD4_BC15_RX7_N	PAM4D_6_TX_P	HTX_1N
			OD4_BC15_TX3_P	PAM4D_7_RX_N	HRX_0P	OD4_BC15_RX0_N	PAM4D_7_TX_P	HTX_0N
PIM-#5	Q17	U14-4A	OD5_BC16_TX3_P	PAM4A_0_RX_N	HRX_7P	OD5_BC16_RX0_N	PAM4A_0_TX_N	HTX_7P
			OD5_BC16_TX1_P	PAM4A_1_RX_N	HRX_6P	OD5_BC16_RX7_P	PAM4A_1_TX_N	HTX_6P

			OD5_BC16_TX2_P	PAM4A_2_RX_N	HRX_5P	OD5_BC16_RX6_N	PAM4A_2_TX_N	HTX_5P
			OD5_BC16_TX0_N	PAM4A_3_RX_N	HRX_4P	OD5_BC16_RX5_P	PAM4A_3_TX_N	HTX_4P
			OD5_BC16_TX4_N	PAM4A_4_RX_N	HRX_3P	OD5_BC16_RX4_P	PAM4A_4_TX_N	HTX_3P
			OD5_BC16_TX6_P	PAM4A_5_RX_N	HRX_2P	OD5_BC16_RX1_N	PAM4A_5_TX_N	HTX_2P
			OD5_BC16_TX7_P	PAM4A_6_RX_N	HRX_1P	OD5_BC16_RX2_P	PAM4A_6_TX_N	HTX_1P
			OD5_BC16_TX5_P	PAM4A_7_RX_N	HRX_0P	OD5_BC16_RX3_N	PAM4A_7_TX_N	HTX_0P
	Q18	U19-4B	OD5_BC20_TX4_N	PAM4B_0_RX_N	HRX_7P	OD5_BC20_RX5_P	PAM4B_0_TX_N	HTX_7P
			OD5_BC20_TX0_P	PAM4B_1_RX_N	HRX_6P	OD5_BC20_RX4_N	PAM4B_1_TX_N	HTX_6P
			OD5_BC20_TX1_N	PAM4B_2_RX_N	HRX_5P	OD5_BC20_RX3_N	PAM4B_2_TX_N	HTX_5P
			OD5_BC20_TX2_P	PAM4B_3_RX_N	HRX_4P	OD5_BC20_RX2_P	PAM4B_3_TX_N	HTX_4P
			OD5_BC20_TX3_N	PAM4B_4_RX_P	HRX_3N	OD5_BC20_RX1_P	PAM4B_4_TX_P	HTX_3N
			OD5_BC20_TX7_P	PAM4B_5_RX_P	HRX_2N	OD5_BC20_RX0_N	PAM4B_5_TX_P	HTX_2N
			OD5_BC20_TX6_N	PAM4B_6_RX_P	HRX_1N	OD5_BC20_RX6_P	PAM4B_6_TX_P	HTX_1N
			OD5_BC20_TX5_P	PAM4B_7_RX_P	HRX_0N	OD5_BC20_RX7_P	PAM4B_7_TX_P	HTX_0N
	Q19	U21-4C	OD5_BC24_TX4_P	PAM4C_0_RX_P	HRX_7N	OD5_BC24_RX5_N	PAM4C_0_TX_P	HTX_7N
			OD5_BC24_TX1_N	PAM4C_1_RX_P	HRX_6N	OD5_BC24_RX4_P	PAM4C_1_TX_P	HTX_6N
			OD5_BC24_TX0_N	PAM4C_2_RX_P	HRX_5N	OD5_BC24_RX6_N	PAM4C_2_TX_P	HTX_5N
			OD5_BC24_TX2_P	PAM4C_3_RX_P	HRX_4N	OD5_BC24_RX3_P	PAM4C_3_TX_P	HTX_4N
			OD5_BC24_TX3_P	PAM4C_4_RX_P	HRX_3N	OD5_BC24_RX2_N	PAM4C_4_TX_P	HTX_3N
			OD5_BC24_TX5_P	PAM4C_5_RX_P	HRX_2N	OD5_BC24_RX1_P	PAM4C_5_TX_P	HTX_2N
			OD5_BC24_TX6_N	PAM4C_6_RX_P	HRX_1N	OD5_BC24_RX0_N	PAM4C_6_TX_P	HTX_1N
			OD5_BC24_TX7_N	PAM4C_7_RX_P	HRX_0N	OD5_BC24_RX7_P	PAM4C_7_TX_P	HTX_0N
	Q20	U17-4D	OD5_BC28_TX5_P	PAM4D_0_RX_N	HRX_7P	OD5_BC28_RX2_N	PAM4D_0_TX_P	HTX_7N
			OD5_BC28_TX6_P	PAM4D_1_RX_P	HRX_6N	OD5_BC28_RX1_P	PAM4D_1_TX_P	HTX_6N
			OD5_BC28_TX7_N	PAM4D_2_RX_P	HRX_5N	OD5_BC28_RX0_P	PAM4D_2_TX_P	HTX_5N
			OD5_BC28_TX0_N	PAM4D_3_RX_P	HRX_4N	OD5_BC28_RX3_N	PAM4D_3_TX_P	HTX_4N
			OD5_BC28_TX1_P	PAM4D_4_RX_P	HRX_3N	OD5_BC28_RX6_N	PAM4D_4_TX_P	HTX_3N
			OD5_BC28_TX2_N	PAM4D_5_RX_P	HRX_2N	OD5_BC28_RX7_P	PAM4D_5_TX_P	HTX_2N
			OD5_BC28_TX3_P	PAM4D_6_RX_P	HRX_1N	OD5_BC28_RX4_N	PAM4D_6_TX_P	HTX_1N
			OD5_BC28_TX4_N	PAM4D_7_RX_N	HRX_0P	OD5_BC28_RX5_P	PAM4D_7_TX_P	HTX_0N
PIM-#6	**Q21**	U14-4A	OD6_BC17_TX3_P	PAM4A_0_RX_N	HRX_7P	OD6_BC17_RX6_P	PAM4A_0_TX_N	HTX_7P
			OD6_BC17_TX2_N	PAM4A_1_RX_N	HRX_6P	OD6_BC17_RX5_P	PAM4A_1_TX_N	HTX_6P
			OD6_BC17_TX1_P	PAM4A_2_RX_N	HRX_5P	OD6_BC17_RX4_P	PAM4A_2_TX_N	HTX_5P
			OD6_BC17_TX4_N	PAM4A_3_RX_N	HRX_4P	OD6_BC17_RX3_N	PAM4A_3_TX_N	HTX_4P
			OD6_BC17_TX0_P	PAM4A_4_RX_N	HRX_3P	OD6_BC17_RX2_P	PAM4A_4_TX_N	HTX_3P

			OD6_BC17_TX7_P	PAM4A_5_RX_N	HRX_2P	OD6_BC17_RX1_N	PAM4A_5_TX_N	HTX_2P
			OD6_BC17_TX5_N	PAM4A_6_RX_N	HRX_1P	OD6_BC17_RX0_N	PAM4A_6_TX_N	HTX_1P
			OD6_BC17_TX6_N	PAM4A_7_RX_N	HRX_0P	OD6_BC17_RX7_N	PAM4A_7_TX_N	HTX_0P
	Q22	U19-4B	OD6_BC21_TX3_P	PAM4B_0_RX_N	HRX_7P	OD6_BC21_RX7_P	PAM4B_0_TX_N	HTX_7P
			OD6_BC21_TX2_N	PAM4B_1_RX_N	HRX_6P	OD6_BC21_RX6_P	PAM4B_1_TX_N	HTX_6P
			OD6_BC21_TX0_N	PAM4B_2_RX_N	HRX_5P	OD6_BC21_RX5_N	PAM4B_2_TX_N	HTX_5P
			OD6_BC21_TX4_P	PAM4B_3_RX_N	HRX_4P	OD6_BC21_RX4_P	PAM4B_3_TX_N	HTX_4P
			OD6_BC21_TX6_P	PAM4B_4_RX_P	HRX_3N	OD6_BC21_RX3_N	PAM4B_4_TX_P	HTX_3N
			OD6_BC21_TX7_N	PAM4B_5_RX_P	HRX_2N	OD6_BC21_RX2_N	PAM4B_5_TX_P	HTX_2N
			OD6_BC21_TX5_N	PAM4B_6_RX_P	HRX_1N	OD6_BC21_RX1_P	PAM4B_6_TX_P	HTX_1N
			OD6_BC21_TX1_P	PAM4B_7_RX_P	HRX_0N	OD6_BC21_RX0_P	PAM4B_7_TX_P	HTX_0N
	Q23	U21-4C	OD6_BC25_TX3_N	PAM4C_0_RX_P	HRX_7N	OD6_BC25_RX7_N	PAM4C_0_TX_P	HTX_7N
			OD6_BC25_TX2_P	PAM4C_1_RX_P	HRX_6N	OD6_BC25_RX6_P	PAM4C_1_TX_P	HTX_6N
			OD6_BC25_TX0_P	PAM4C_2_RX_P	HRX_5N	OD6_BC25_RX5_N	PAM4C_2_TX_P	HTX_5N
			OD6_BC25_TX4_N	PAM4C_3_RX_P	HRX_4N	OD6_BC25_RX4_P	PAM4C_3_TX_P	HTX_4N
			OD6_BC25_TX6_N	PAM4C_4_RX_P	HRX_3N	OD6_BC25_RX3_P	PAM4C_4_TX_P	HTX_3N
			OD6_BC25_TX7_P	PAM4C_5_RX_P	HRX_2N	OD6_BC25_RX2_N	PAM4C_5_TX_P	HTX_2N
			OD6_BC25_TX5_P	PAM4C_6_RX_P	HRX_1N	OD6_BC25_RX0_P	PAM4C_6_TX_P	HTX_1N
			OD6_BC25_TX1_N	PAM4C_7_RX_P	HRX_0N	OD6_BC25_RX1_N	PAM4C_7_TX_P	HTX_0N
	Q24	U17-4D	OD6_BC29_TX2_N	PAM4D_0_RX_N	HRX_7P	OD6_BC29_RX7_N	PAM4D_0_TX_P	HTX_7N
			OD6_BC29_TX0_N	PAM4D_1_RX_P	HRX_6N	OD6_BC29_RX6_P	PAM4D_1_TX_P	HTX_6N
			OD6_BC29_TX3_P	PAM4D_2_RX_P	HRX_5N	OD6_BC29_RX5_N	PAM4D_2_TX_P	HTX_5N
			OD6_BC29_TX1_P	PAM4D_3_RX_P	HRX_4N	OD6_BC29_RX4_N	PAM4D_3_TX_P	HTX_4N
			OD6_BC29_TX4_P	PAM4D_4_RX_P	HRX_3N	OD6_BC29_RX1_P	PAM4D_4_TX_P	HTX_3N
			OD6_BC29_TX6_P	PAM4D_5_RX_P	HRX_2N	OD6_BC29_RX2_N	PAM4D_5_TX_P	HTX_2N
			OD6_BC29_TX7_N	PAM4D_6_RX_P	HRX_1N	OD6_BC29_RX3_N	PAM4D_6_TX_P	HTX_1N
			OD6_BC29_TX5_P	PAM4D_7_RX_N	HRX_0P	OD6_BC29_RX0_P	PAM4D_7_TX_P	HTX_0N
PIM-#7	Q25	U14-4A	OD7_BC18_TX1_N	PAM4A_0_RX_N	HRX_7P	OD7_BC18_RX0_N	PAM4A_0_TX_N	HTX_7P
			OD7_BC18_TX7_P	PAM4A_1_RX_N	HRX_6P	OD7_BC18_RX2_N	PAM4A_1_TX_N	HTX_6P
			OD7_BC18_TX6_N	PAM4A_2_RX_N	HRX_5P	OD7_BC18_RX1_N	PAM4A_2_TX_N	HTX_5P
			OD7_BC18_TX5_P	PAM4A_3_RX_N	HRX_4P	OD7_BC18_RX4_P	PAM4A_3_TX_N	HTX_4P
			OD7_BC18_TX4_N	PAM4A_4_RX_N	HRX_3P	OD7_BC18_RX5_P	PAM4A_4_TX_N	HTX_3P
			OD7_BC18_TX0_P	PAM4A_5_RX_N	HRX_2P	OD7_BC18_RX6_N	PAM4A_5_TX_N	HTX_2P
			OD7_BC18_TX2_P	PAM4A_6_RX_N	HRX_1P	OD7_BC18_RX7_P	PAM4A_6_TX_N	HTX_1P
			OD7_BC18_TX3_N	PAM4A_7_RX_N	HRX_0P	OD7_BC18_RX3_N	PAM4A_7_TX_N	HTX_0P

	Q26	U19-4B	OD7_BC22_TX6_P	PAM4B_0_RX_N	HRX_7P	OD7_BC22_RX3_P	PAM4B_0_TX_N	HTX_7P
			OD7_BC22_TX7_N	PAM4B_1_RX_N	HRX_6P	OD7_BC22_RX0_P	PAM4B_1_TX_N	HTX_6P
			OD7_BC22_TX5_P	PAM4B_2_RX_N	HRX_5P	OD7_BC22_RX1_P	PAM4B_2_TX_N	HTX_5P
			OD7_BC22_TX0_N	PAM4B_3_RX_N	HRX_4P	OD7_BC22_RX2_N	PAM4B_3_TX_N	HTX_4P
			OD7_BC22_TX4_N	PAM4B_4_RX_P	HRX_3N	OD7_BC22_RX6_P	PAM4B_4_TX_P	HTX_3N
			OD7_BC22_TX1_P	PAM4B_5_RX_P	HRX_2N	OD7_BC22_RX4_P	PAM4B_5_TX_P	HTX_2N
			OD7_BC22_TX2_P	PAM4B_6_RX_P	HRX_1N	OD7_BC22_RX5_P	PAM4B_6_TX_P	HTX_1N
			OD7_BC22_TX3_N	PAM4B_7_RX_P	HRX_0N	OD7_BC22_RX7_P	PAM4B_7_TX_P	HTX_0N
	Q27	U21-4C	OD7_BC26_TX6_N	PAM4C_0_RX_P	HRX_7N	OD7_BC26_RX3_N	PAM4C_0_TX_P	HTX_7N
			OD7_BC26_TX7_P	PAM4C_1_RX_P	HRX_6N	OD7_BC26_RX0_P	PAM4C_1_TX_P	HTX_6N
			OD7_BC26_TX5_N	PAM4C_2_RX_P	HRX_5N	OD7_BC26_RX1_P	PAM4C_2_TX_P	HTX_5N
			OD7_BC26_TX0_P	PAM4C_3_RX_P	HRX_4N	OD7_BC26_RX2_N	PAM4C_3_TX_P	HTX_4N
			OD7_BC26_TX4_P	PAM4C_4_RX_P	HRX_3N	OD7_BC26_RX4_P	PAM4C_4_TX_P	HTX_3N
			OD7_BC26_TX2_P	PAM4C_5_RX_P	HRX_2N	OD7_BC26_RX7_P	PAM4C_5_TX_P	HTX_2N
			OD7_BC26_TX1_P	PAM4C_6_RX_P	HRX_1N	OD7_BC26_RX5_N	PAM4C_6_TX_P	HTX_1N
			OD7_BC26_TX3_P	PAM4C_7_RX_P	HRX_0N	OD7_BC26_RX6_P	PAM4C_7_TX_P	HTX_0N
	Q28	U17-4D	OD7_BC30_TX5_N	PAM4D_0_RX_N	HRX_7P	OD7_BC30_RX2_P	PAM4D_0_TX_P	HTX_7N
			OD7_BC30_TX6_P	PAM4D_1_RX_P	HRX_6N	OD7_BC30_RX1_N	PAM4D_1_TX_P	HTX_6N
			OD7_BC30_TX7_P	PAM4D_2_RX_P	HRX_5N	OD7_BC30_RX0_N	PAM4D_2_TX_P	HTX_5N
			OD7_BC30_TX4_N	PAM4D_3_RX_P	HRX_4N	OD7_BC30_RX3_P	PAM4D_3_TX_P	HTX_4N
			OD7_BC30_TX0_P	PAM4D_4_RX_P	HRX_3N	OD7_BC30_RX6_N	PAM4D_4_TX_P	HTX_3N
			OD7_BC30_TX1_N	PAM4D_5_RX_P	HRX_2N	OD7_BC30_RX7_P	PAM4D_5_TX_P	HTX_2N
			OD7_BC30_TX2_P	PAM4D_6_RX_P	HRX_1N	OD7_BC30_RX5_N	PAM4D_6_TX_P	HTX_1N
			OD7_BC30_TX3_N	PAM4D_7_RX_N	HRX_0P	OD7_BC30_RX4_P	PAM4D_7_TX_P	HTX_0N
PIM-#8	Q29	U14-4A	OD8_BC19_TX1_N	PAM4A_0_RX_N	HRX_7P	OD8_BC19_RX6_N	PAM4A_0_TX_N	HTX_7P
			OD8_BC19_TX3_P	PAM4A_1_RX_N	HRX_6P	OD8_BC19_RX7_P	PAM4A_1_TX_N	HTX_6P
			OD8_BC19_TX2_N	PAM4A_2_RX_N	HRX_5P	OD8_BC19_RX4_P	PAM4A_2_TX_N	HTX_5P
			OD8_BC19_TX0_N	PAM4A_3_RX_N	HRX_4P	OD8_BC19_RX5_N	PAM4A_3_TX_N	HTX_4P
			OD8_BC19_TX5_P	PAM4A_4_RX_N	HRX_3P	OD8_BC19_RX1_N	PAM4A_4_TX_N	HTX_3P
			OD8_BC19_TX7_P	PAM4A_5_RX_N	HRX_2P	OD8_BC19_RX0_P	PAM4A_5_TX_N	HTX_2P
			OD8_BC19_TX4_N	PAM4A_6_RX_N	HRX_1P	OD8_BC19_RX2_N	PAM4A_6_TX_N	HTX_1P
			OD8_BC19_TX6_N	PAM4A_7_RX_N	HRX_0P	OD8_BC19_RX3_N	PAM4A_7_TX_N	HTX_0P
	Q30	U19-4B	OD8_BC23_TX1_N	PAM4B_0_RX_N	HRX_7P	OD8_BC23_RX4_P	PAM4B_0_TX_N	HTX_7P
			OD8_BC23_TX5_P	PAM4B_1_RX_N	HRX_6P	OD8_BC23_RX5_P	PAM4B_1_TX_N	HTX_6P
			OD8_BC23_TX2_P	PAM4B_2_RX_N	HRX_5P	OD8_BC23_RX6_N	PAM4B_2_TX_N	HTX_5P

			OD8_BC23_TX3_N	PAM4B_3_RX_N	HRX_4P	OD8_BC23_RX0_N	PAM4B_3_TX_N	HTX_4P
			OD8_BC23_TX4_N	PAM4B_4_RX_P	HRX_3N	OD8_BC23_RX1_P	PAM4B_4_TX_P	HTX_3N
			OD8_BC23_TX0_P	PAM4B_5_RX_P	HRX_2N	OD8_BC23_RX2_N	PAM4B_5_TX_P	HTX_2N
			OD8_BC23_TX7_P	PAM4B_6_RX_P	HRX_1N	OD8_BC23_RX7_N	PAM4B_6_TX_P	HTX_1N
			OD8_BC23_TX6_N	PAM4B_7_RX_P	HRX_0N	OD8_BC23_RX3_P	PAM4B_7_TX_P	HTX_0N
	Q31	U21-4C	OD8_BC27_TX1_P	PAM4C_0_RX_P	HRX_7N	OD8_BC23_RX4_N	PAM4C_0_TX_P	HTX_7N
			OD8_BC27_TX3_P	PAM4C_1_RX_P	HRX_6N	OD8_BC27_RX6_N	PAM4C_1_TX_P	HTX_6N
			OD8_BC27_TX5_N	PAM4C_2_RX_P	HRX_5N	OD8_BC27_RX5_P	PAM4C_2_TX_P	HTX_5N
			OD8_BC27_TX2_N	PAM4C_3_RX_P	HRX_4N	OD8_BC27_RX4_N	PAM4C_3_TX_P	HTX_4N
			OD8_BC27_TX4_P	PAM4C_4_RX_P	HRX_3N	OD8_BC27_RX0_P	PAM4C_4_TX_P	HTX_3N
			OD8_BC27_TX0_N	PAM4C_5_RX_P	HRX_2N	OD8_BC27_RX1_N	PAM4C_5_TX_P	HTX_2N
			OD8_BC27_TX7_N	PAM4C_6_RX_P	HRX_1N	OD8_BC27_RX2_P	PAM4C_6_TX_P	HTX_1N
			OD8_BC27_TX6_P	PAM4C_7_RX_P	HRX_0N	OD8_BC27_RX7_P	PAM4C_7_TX_P	HTX_0N
	Q32	U17-4D	OD8_BC31_TX5_N	PAM4D_0_RX_N	HRX_7P	OD8_BC27_RX3_P	PAM4D_0_TX_P	HTX_7N
			OD8_BC31_TX7_P	PAM4D_1_RX_P	HRX_6N	OD8_BC31_RX0_P	PAM4D_1_TX_P	HTX_6N
			OD8_BC31_TX6_N	PAM4D_2_RX_P	HRX_5N	OD8_BC31_RX1_N	PAM4D_2_TX_P	HTX_5N
			OD8_BC31_TX0_P	PAM4D_3_RX_P	HRX_4N	OD8_BC31_RX2_P	PAM4D_3_TX_P	HTX_4N
			OD8_BC31_TX1_P	PAM4D_4_RX_P	HRX_3N	OD8_BC31_RX3_N	PAM4D_4_TX_P	HTX_3N
			OD8_BC31_TX4_P	PAM4D_5_RX_P	HRX_2N	OD8_BC31_RX7_P	PAM4D_5_TX_P	HTX_2N
			OD8_BC31_TX3_P	PAM4D_6_RX_P	HRX_1N	OD8_BC31_RX6_N	PAM4D_6_TX_P	HTX_1N
			OD8_BC31_TX2_N	PAM4D_7_RX_N	HRX_0P	OD8_BC31_RX5_P	PAM4D_7_TX_P	HTX_0N

Table 15: Minipack TH3 Port Mapping for PIM-4DD

The following table show the QSFP-DD port mapping in PIM-4DD card.

U14 (BCM81328)		Net name	CONN17	PN swap
P2	MTX_0P	QSFP1_DD_TX0_P	Q1	N
R2	MTX_0N	QSFP1_DD_TX0_N		
P4	MTX_1P	QSFP1_DD_TX1_P		N
R4	MTX_1N	QSFP1_DD_TX1_N		
P6	MTX_2P	QSFP1_DD_TX2_P		N
R6	MTX_2N	QSFP1_DD_TX2_N		
P8	MTX_3P	QSFP1_DD_TX3_P		N
R8	MTX_3N	QSFP1_DD_TX3_N		

P10	MTX_4P	QSFP1_DD_TX4_P		N
R10	MTX_4N	QSFP1_DD_TX4_N		
P12	MTX_5P	QSFP1_DD_TX5_P		N
R12	MTX_5N	QSFP1_DD_TX5_N		
P14	MTX_6P	QSFP1_DD_TX6_P		N
R14	MTX_6N	QSFP1_DD_TX6_N		
P16	MTX_7P	QSFP1_DD_TX7_P		N
R16	MTX_7N	QSFP1_DD_TX7_N		
U3	MRX_0P	QSFP1_DD_RX0_P	Q1	N
V3	MRX_0N	QSFP1_DD_RX0_N		
U5	MRX_1P	QSFP1_DD_RX1_P		N
V5	MRX_1N	QSFP1_DD_RX1_N		
U7	MRX_2P	QSFP1_DD_RX2_P		N
V7	MRX_2N	QSFP1_DD_RX2_N		
U9	MRX_3P	QSFP1_DD_RX3_P		N
V9	MRX_3N	QSFP1_DD_RX3_N		
U11	MRX_4P	QSFP1_DD_RX4_P		N
V11	MRX_4N	QSFP1_DD_RX4_N		
U13	MRX_5P	QSFP1_DD_RX5_P		N
V13	MRX_5N	QSFP1_DD_RX5_N		
U15	MRX_6P	QSFP1_DD_RX6_P		N
V15	MRX_6N	QSFP1_DD_RX6_N		
U17	MRX_7P	QSFP1_DD_RX7_P		N
V17	MRX_7N	QSFP1_DD_RX7_N		
U19 (BCM81328)		**Net name**	**CONN16**	**PN swap**
P2	MTX_0P	QSFP2_DD_TX0_P	Q2	N
R2	MTX_0N	QSFP2_DD_TX0_N		
P4	MTX_1P	QSFP2_DD_TX1_P		N
R4	MTX_1N	QSFP2_DD_TX1_N		
P6	MTX_2P	QSFP2_DD_TX2_P		N
R6	MTX_2N	QSFP2_DD_TX2_N		
P8	MTX_3P	QSFP2_DD_TX3_P		N
R8	MTX_3N	QSFP2_DD_TX3_N		
P10	MTX_4P	QSFP2_DD_TX4_P		N
R10	MTX_4N	QSFP2_DD_TX4_N		
P12	MTX_5P	QSFP2_DD_TX5_P		N

R12	MTX_5N	QSFP2_DD_TX5_N		
P14	MTX_6P	QSFP2_DD_TX6_P		N
R14	MTX_6N	QSFP2_DD_TX6_N		
P16	MTX_7P	QSFP2_DD_TX7_P		N
R16	MTX_7N	QSFP2_DD_TX7_N		
U3	MRX_0P	QSFP2_DD_RX0_P	Q2	N
V3	MRX_0N	QSFP2_DD_RX0_N		
U5	MRX_1P	QSFP2_DD_RX1_P		N
V5	MRX_1N	QSFP2_DD_RX1_N		
U7	MRX_2P	QSFP2_DD_RX2_P		N
V7	MRX_2N	QSFP2_DD_RX2_N		
U9	MRX_3P	QSFP2_DD_RX3_P		N
V9	MRX_3N	QSFP2_DD_RX3_N		
U11	MRX_4P	QSFP2_DD_RX4_P		N
V11	MRX_4N	QSFP2_DD_RX4_N		
U13	MRX_5P	QSFP2_DD_RX5_P		N
V13	MRX_5N	QSFP2_DD_RX5_N		
U15	MRX_6P	QSFP2_DD_RX6_P		N
V15	MRX_6N	QSFP2_DD_RX6_N		
U17	MRX_7P	QSFP2_DD_RX7_P		N
V17	MRX_7N	QSFP2_DD_RX7_N		
U21 (BCM81328)		**Net name**	**CONN15**	**PN swap**
P2	MTX_0P	QSFP3_DD_TX0_P	Q3	N
R2	MTX_0N	QSFP3_DD_TX0_N		
P4	MTX_1P	QSFP3_DD_TX1_P		N
R4	MTX_1N	QSFP3_DD_TX1_N		
P6	MTX_2P	QSFP3_DD_TX2_P		N
R6	MTX_2N	QSFP3_DD_TX2_N		
P8	MTX_3P	QSFP3_DD_TX3_P		N
R8	MTX_3N	QSFP3_DD_TX3_N		
P10	MTX_4P	QSFP3_DD_TX4_P		N
R10	MTX_4N	QSFP3_DD_TX4_N		
P12	MTX_5P	QSFP3_DD_TX5_P		N
R12	MTX_5N	QSFP3_DD_TX5_N		
P14	MTX_6P	QSFP3_DD_TX6_P		N
R14	MTX_6N	QSFP3_DD_TX6_N		

P16	MTX_7P	QSFP3_DD_TX7_P		N
R16	MTX_7N	QSFP3_DD_TX7_N		
U3	MRX_0P	QSFP3_DD_RX0_P	Q3	N
V3	MRX_0N	QSFP3_DD_RX0_N		
U5	MRX_1P	QSFP3_DD_RX1_P		N
V5	MRX_1N	QSFP3_DD_RX1_N		
U7	MRX_2P	QSFP3_DD_RX2_P		N
V7	MRX_2N	QSFP3_DD_RX2_N		
U9	MRX_3P	QSFP3_DD_RX3_P		N
V9	MRX_3N	QSFP3_DD_RX3_N		
U11	MRX_4P	QSFP3_DD_RX4_P		N
V11	MRX_4N	QSFP3_DD_RX4_N		
U13	MRX_5P	QSFP3_DD_RX5_P		N
V13	MRX_5N	QSFP3_DD_RX5_N		
U15	MRX_6P	QSFP3_DD_RX6_P		N
V15	MRX_6N	QSFP3_DD_RX6_N		
U17	MRX_7P	QSFP3_DD_RX7_P		N
V17	MRX_7N	QSFP3_DD_RX7_N		
U17 (BCM81328)		**Net name**	**CONN14**	**PN swap**
P2	MTX_0P	QSFP4_DD_TX0_P	Q4	N
R2	MTX_0N	QSFP4_DD_TX0_N		
P4	MTX_1P	QSFP4_DD_TX1_P		N
R4	MTX_1N	QSFP4_DD_TX1_N		
P6	MTX_2P	QSFP4_DD_TX2_P		N
R6	MTX_2N	QSFP4_DD_TX2_N		
P8	MTX_3P	QSFP4_DD_TX3_P		N
R8	MTX_3N	QSFP4_DD_TX3_N		
P10	MTX_4P	QSFP4_DD_TX4_P		N
R10	MTX_4N	QSFP4_DD_TX4_N		
P12	MTX_5P	QSFP4_DD_TX5_P		N
R12	MTX_5N	QSFP4_DD_TX5_N		
P14	MTX_6P	QSFP4_DD_TX6_P		N
R14	MTX_6N	QSFP4_DD_TX6_N		
P16	MTX_7P	QSFP4_DD_TX7_P		N
R16	MTX_7N	QSFP4_DD_TX7_N		
U3	MRX_0P	QSFP4_DD_RX0_P	Q4	N

V3	MRX_0N	QSFP4_DD_RX0_N		
U5	MRX_1P	QSFP4_DD_RX1_P		N
V5	MRX_1N	QSFP4_DD_RX1_N		
U7	MRX_2P	QSFP4_DD_RX2_P		N
V7	MRX_2N	QSFP4_DD_RX2_N		
U9	MRX_3P	QSFP4_DD_RX3_P		N
V9	MRX_3N	QSFP4_DD_RX3_N		
U11	MRX_4P	QSFP4_DD_RX4_P		N
V11	MRX_4N	QSFP4_DD_RX4_N		
U13	MRX_5P	QSFP4_DD_RX5_P		N
V13	MRX_5N	QSFP4_DD_RX5_N		
U15	MRX_6P	QSFP4_DD_RX6_P		N
V15	MRX_6N	QSFP4_DD_RX6_N		
U17	MRX_7P	QSFP4_DD_RX7_P		N
V17	MRX_7N	QSFP4_DD_RX7_N		

Table 16: PIM-4DD Retimer Port Mapping

9.3 Control Plane

Main control plane features are listed below:

- COM-Express BW-DE CPU module
  - 8mm mating distance.
  - Can upgrade to future COM-e module
  - Implemented on SCM
- BMC as management entity to control Switch ASIC and COM-e CPU module
  - Enable/disable power of switch ASIC or SCM
  - OOB ethernet to SCM
  - Console port to SCM
  - SMB bus and I2C bus to SCM COM-e CPU module
- Front panel management and debug interface
  - Facebook 2nd generation debug connector
- PCIe Interface
  - Primary Bus 0: PCIe x4 Gen-3 between SCM COM-e and Switch ASIC(Tomahawk3)
  - PCIe clock is from COM-e module to Switch ASIC
  - Secondary Bus 1: PCIe x 4 Gen-3 bus to SMB and to eight PIM via PCIe switch
- LPC bus
  - SCM COM-e LPC bus control the following devices
    - LPC TPM on SCM
    - BMC on SMB
    - SYSCPLD of SMB
  - SMB SYSCPLD implement LPC to I2C bridge function
- OOB Ethernet
  - 8-port OOB switch on SMB
    - BMC GBE ethernet interface
    - SCM COM-e ethernet interface
    - Switch ASIC management GBE port(SGMII)
    - System OOB ethernet interface(SCM front panel)
    - Reserved GbE interface for PIM
    - On-board debug RJ45 port

- Secondary 10GBE Ethernet interface
  - 10GBE interface of BW-DE COM-e connect to Tomahawk3 management 10GBE interface

- USB
  - COM-e is root-complex port
  - 3-port USB hub on SMB
    - BMC USB slave port
    - On-board debug USB type-A port
    - CP2112 USB port for QSFP28 I2C access

Minipack has Gigabit Ethernet out-of-band communication network and console inside the chassis. The following diagram show the architecture of the OOB Ethernet design:

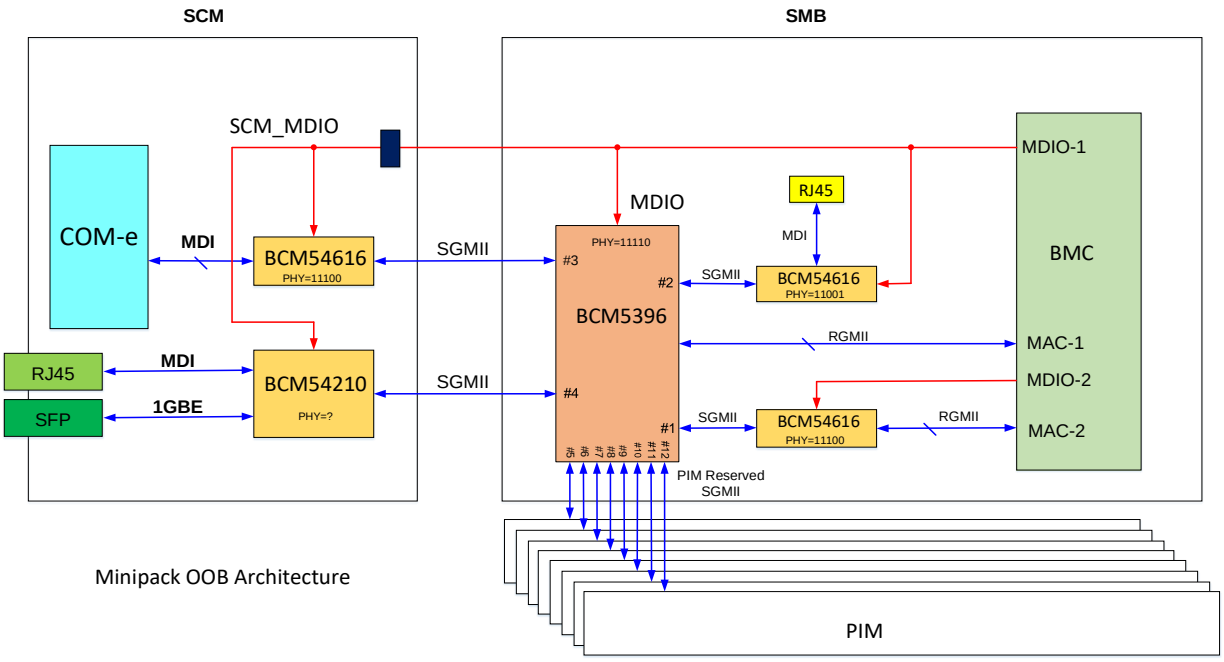


Figure 9-6: Minipack OOB Network Architecture

Minipack also has an internal UART network, and the following diagram shows the UART console network design inside the chassis.

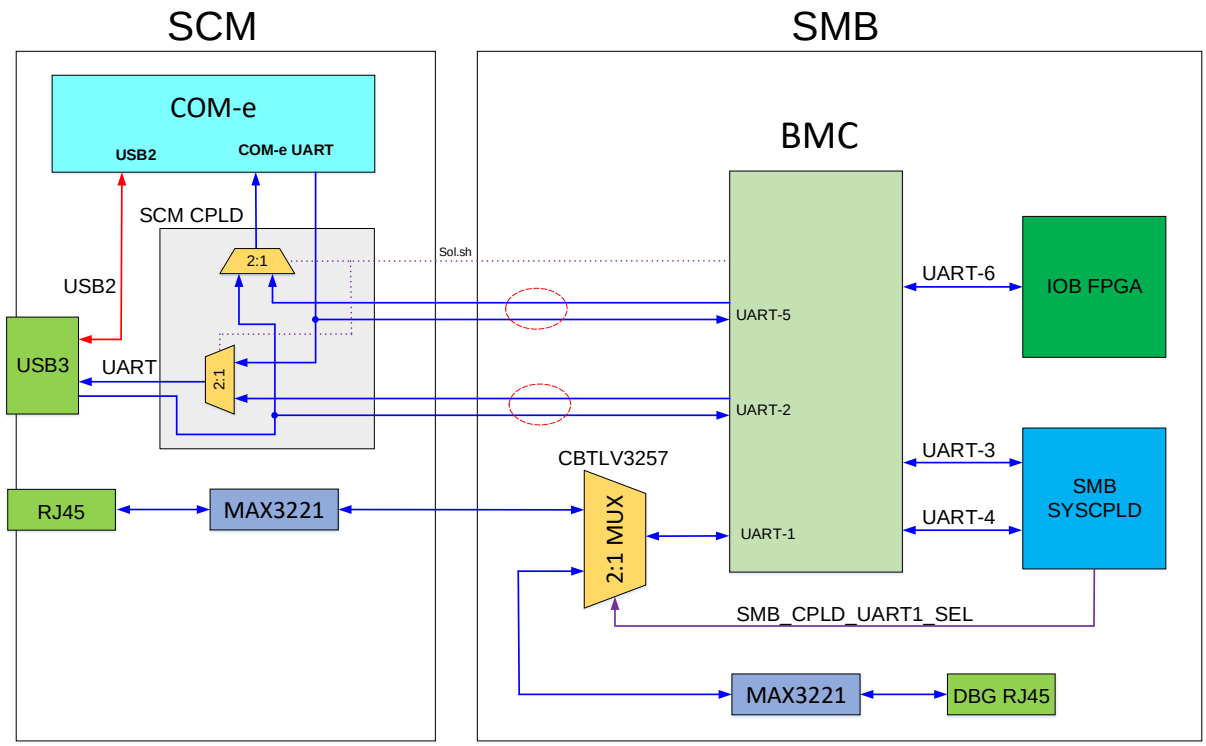


Figure 9-7: Minipack UART Architecture

9.4 Chassis Management Plane

BMC on SMB takes care of system hardware management, including

- System thermal management and fan control
- Sensor monitoring
- Serial over LAN (SoL) for the microserver console
- Firmware upgrade

The chassis management bus is I2C, and it provides access to the following modules:

- System Control Module(SCM)
- Port Interface Module(PIM)
  - PIM-16Q
  - PIM-4DD
- FCM (BMC I2C bus #9)
  - FCM-T
  - FCM-B
- PDB (BMC I2C bus #3)
  - PDB-L
  - PDB-R

9.5 Power Plane

Power of the chassis is provided by four power supply units. Each PSU is rated to supply up to 1500W at 12V. The following is estimated power consumption of Minipack.

Components	Max (W)	Practical Max (W)	Qty	Notes
Tomahawk3	365	300	1	Maximal power from the datasheet is 365W. Typical power at full line rate is 300W.
QSFP28 optics	448	358	128	Max: 3.5W, Typical: 2.8W
QSFP-DD 400G optics	0	0	0	Max: 12W, Typical: 9W
BCM81724 (gearbox)	384	288	32	Max: 12W w/ AVS Typical: 9W w/ AVS
BMC etc.	5	3	1	
COM-e	40	30	1	COM-e CPU module including DIMM
Misc components	30	20	1	FPGA, CPLD, LED, Flash, SSD, EEPROM, etc
Total Component power	1272	999		Total power consumption of discrete components excluding fans which directly uses 12V
Cooling fans	560	80	8	Directly powered by 12V
VR loss	95	75		93% eff. to step down from 12V
AC-PSU	123	73		94% efficiency from AC 208V to 12V
Total power of chassis	2050	1227		Input power of the chassis

Table 17: Minipack Power Consumption with 8 PIM-16Q

Components	Max (W)	Practical Max (W)	Qty	Notes
Tomahawk3	365	300	1	Maximal power from the datasheet is 365W. Typical power at full line rate is 300W.
QSFP28 100G	224	179	64	Max: 3.5W, Typical: 2.8W
QSFP-DD 400G	192	144	16	Max: 12W, Typical: 9W
BCM81724 (gearbox)	192	144	16	Max: 12W w/ AVS Typical: 9W w/ AVS
BCM81328 (retimer)	147	86	16	Max: 9.2 w/o AVS Typical: 5.4 w/ AVS
BMC etc.	5	3	1	
COM-e	40	30	1	COM-e CPU module including DIMM
Misc components	30	20	1	FPGA, CPLD, LED, Flash, SSD, EEPROM, etc
Total Component power	1195	906		Total power consumption of discrete components excluding fans which directly uses 12V
Cooling fans	560	80	8	Directly powered by 12V
VR loss	90	68		93% eff. to step down from 12V
AC-PSU	118	67		94% efficiency from AC 208V to 12V
total power of chassis	1963	1121		Input power of the chassis

Table 18: Minipack Power Consumption with 4 PIM-16Q and 4 PIM-4DD

9.5.1 Power Distribution System

Minipack Power distribution system consists of the following items:

- PSU: 1500W PSU from BelPower PFE1500-12-054NAC
- PDB: Power Distribution Board
    - PDB-R: Power Distribution Board Right
    - PDB-L: Power Distribution Board Left
    - PDB-H: Power Distribution Board Horizontal, BusBar

	Current (A)	Power (W)	Note
PDB-R	250A	3000W	Support two PSU 2x1500W max
PDB-L	250A	3000W	Support two PSU 2x1500W max
PDB-H	252A (28A x 9)	3024W	Provide power for 8 PIM and 1 SCM, busbar implementation

Table 19: Minipack Power Distribution Design Budget

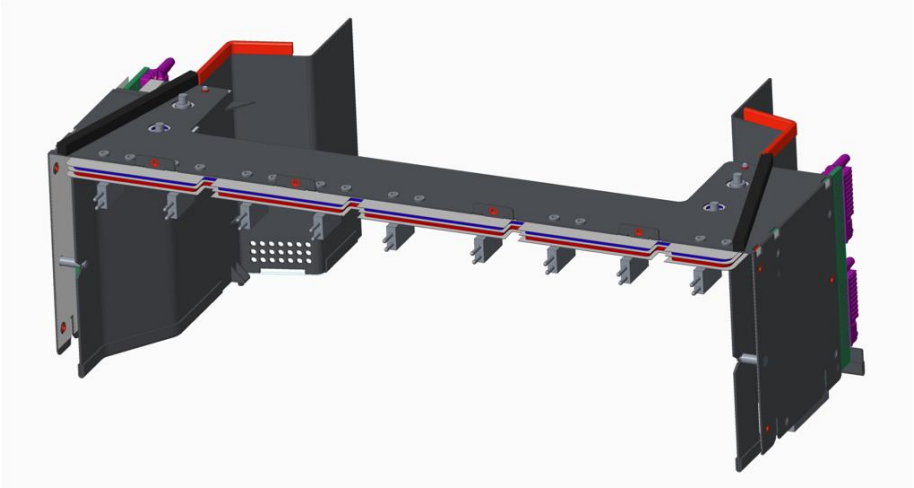


Figure 9-8: PDB-H

The following block diagram shows the I2C buses from the BMC to the PSUs and other components on PDB-L, PDB-R, and SIM.

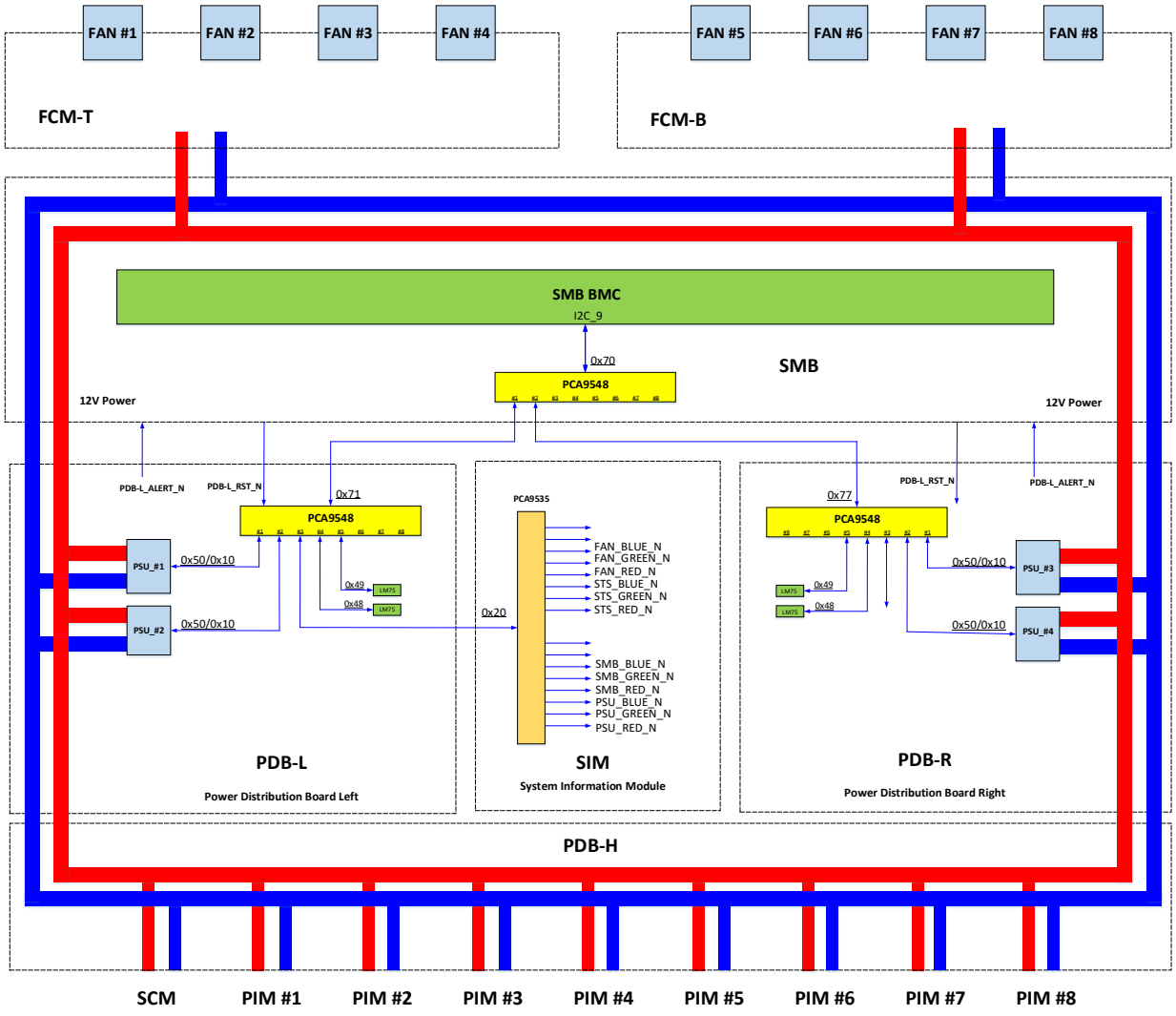


Figure 9-9: Minipack Power Distribution and Associated I2C Bus Topology

9.5.2 PSU

Minipack uses BelPower PFE1500-12-054NAC AC power supply unit (PSU) to provide power to the chassis. There are 4 PSU in the chassis. Each PSU is rated at 1500W with 12V output. The

power system of Minipack is load sharing of four PSU, usually it is used as 2+2 PSU redundancy, two PSU connect to one AC feed and two other PSU connect to redundant feed, providing feed redundancy, And two PSU in one feed can also provide PSU redundancy.

Second source PSU is also needed to provide better availability. The following new requirement need to be supported by second source PSU.

- AC power input range need to support FB 277VAC input
- PSU efficiency need to be improved from 94% to 96%.
- PSU need to support dual fuse to support Line to Line voltage input.

The following Figure shows the AC PSU from BelPower/PowerOne.

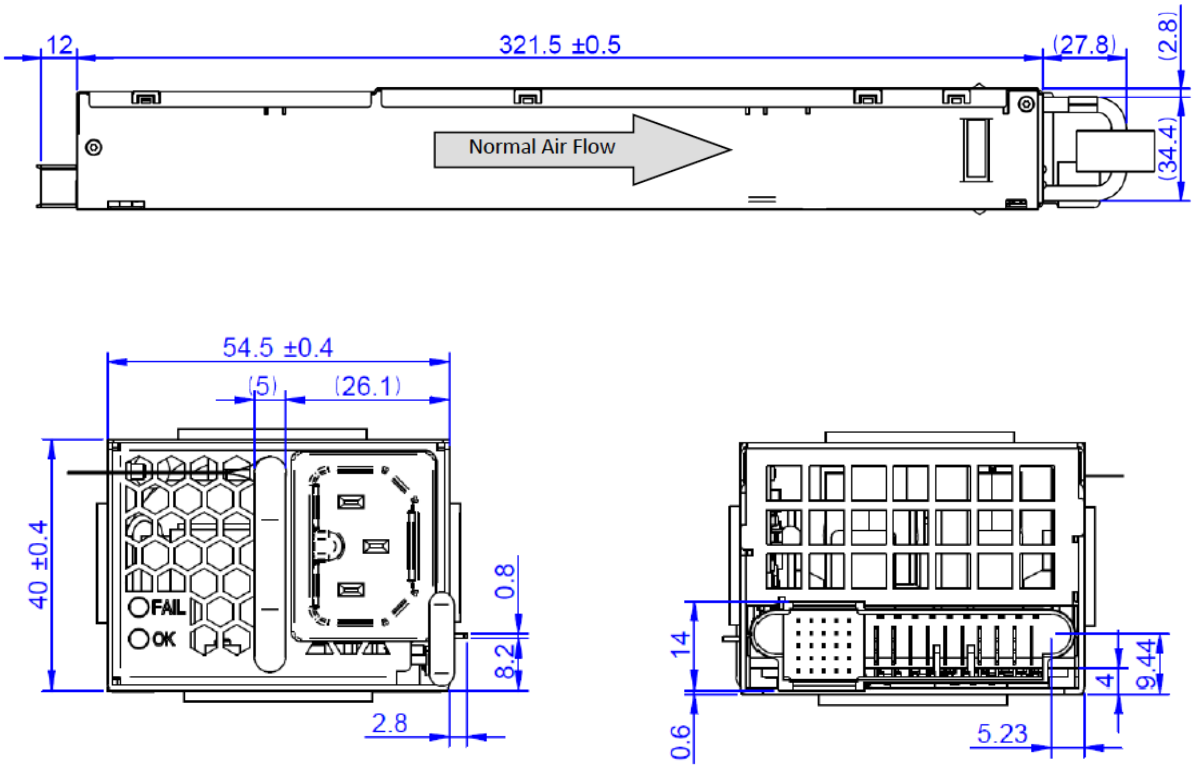


Figure 9-10: PFE1500-12-054NAC 1.5KW PSU

Power Supply Connector: Tyco Electronics P/N 2-1926736-3 (NOTE: Column 5 is recessed (short pins))

Mating Connector: Tyco Electronics P/N 2-1926739-5 or FCI 10108888-R10253SLF

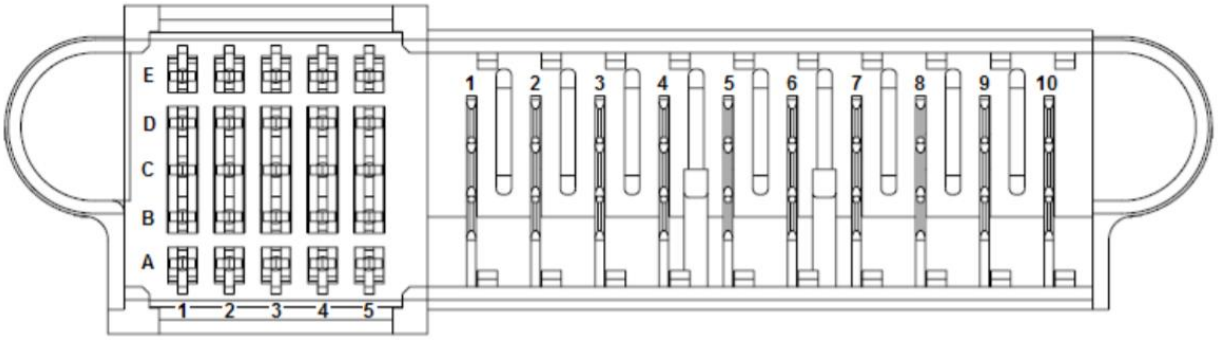


Figure 9-11: PSU Power Output Connector

Pin	Signal	Description
6, 7, 8, 9, 10	V12	12V output
1, 2, 3, 4, 5	PGND	Power ground
A1	VSB	Standby positive output (+3.3/5 V)
B1	VSB	Standby positive output (+3.3/5 V)
C1	VSB	Standby positive output (+3.3/5 V)
D1	VSB	Standby positive output (+3.3/5 V)
E1	VSB	Standby positive output (+3.3/5 V)
A2	SGND	Signal ground (return)
B2	SGND	Signal ground (return)
C2	HOTSTANDBYEN_H	Hot standby enable signal: active-high
D2	VSB_SENSE_R	Standby output negative sense
E2	VSB_SENSE	Standby output positive sense
A3	APS	I2C address and protocol selection (select by a pull down resistor)
B3	N/C	Reserved
C3	SDA	I2C data signal line
D3	V1_SENSE_R	Main output negative sense
E3	V1_SENSE	Main output positive sense
A4	SCL	I2C clock signal line

B4	PSON_L	Power supply on input (connect to A2/B2 to turn unit on): active-low
C4	SMB_ALERT_L	SMB Alert signal output: active-low
D4	N/C	Reserved
E4	ACOK_H	AC input OK signal: active-high
A5	PSKILL_H	Power supply kill (lagging pin): active-high
B5	ISHARE	Current share bus (lagging pin)
C5	PWOK_H	Power OK signal output (lagging pin): active-high
D5	VSB_SEL	Standby voltage selection (lagging pin)
E5	PRESENT_L	Power supply present (lagging pin): active-low

Table 20: PSU to PDB Connector Pin-out

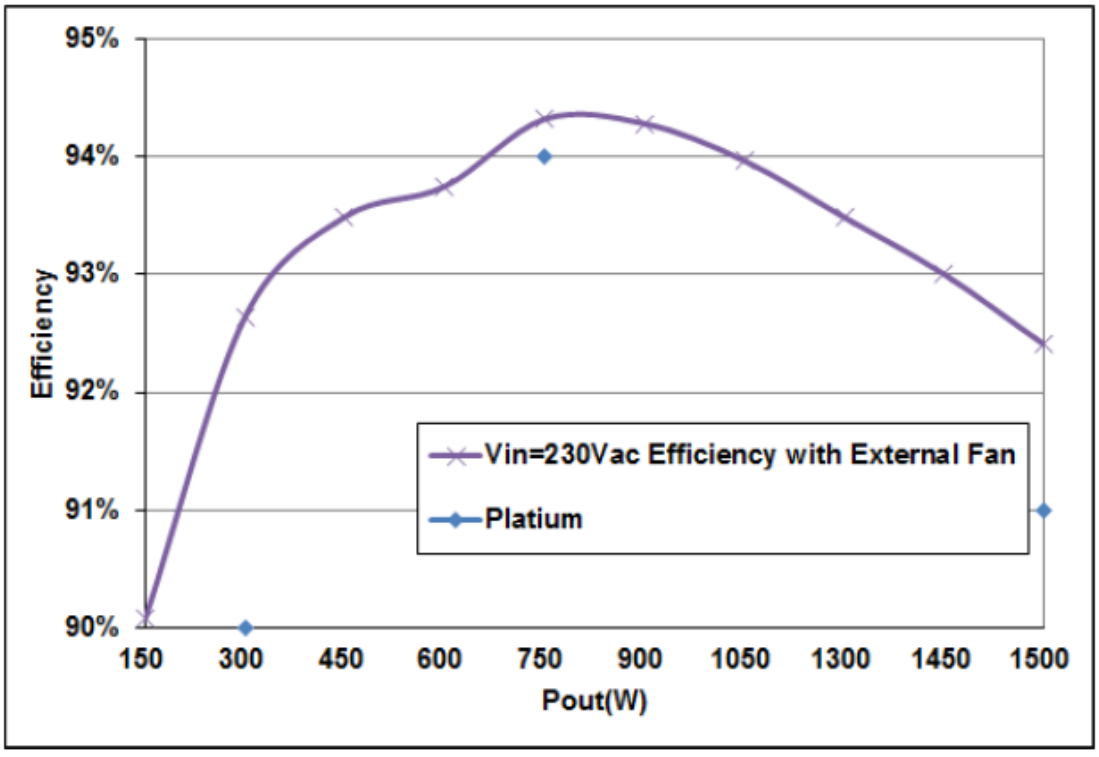


Figure 9-12: PFE1500 Efficiency Curve

9.6 Thermal Design

The thermal design of Minipack is optimized for better thermal performance to support CWDM4-OCP 100G optics (with 55°C case temperature limit) and future 200G and 400G optics. It is also targeting much better thermal performance than current 128 x 100G configuration, enabling Minipack platform to support future 128 x 200G design.

Totally there are 8 fan-trays in Minipack chassis, and each fan-tray has one 80mm x 80mm x 80mm CR fan. Each FCM (Fan Control Module) supports 4 fan-tray, and there are two FCM in the system: FCM-T and FCM-B.

9.6.1 Fan Tray

Minipack chassis supports eight fan-trays with 7+1 redundancy.

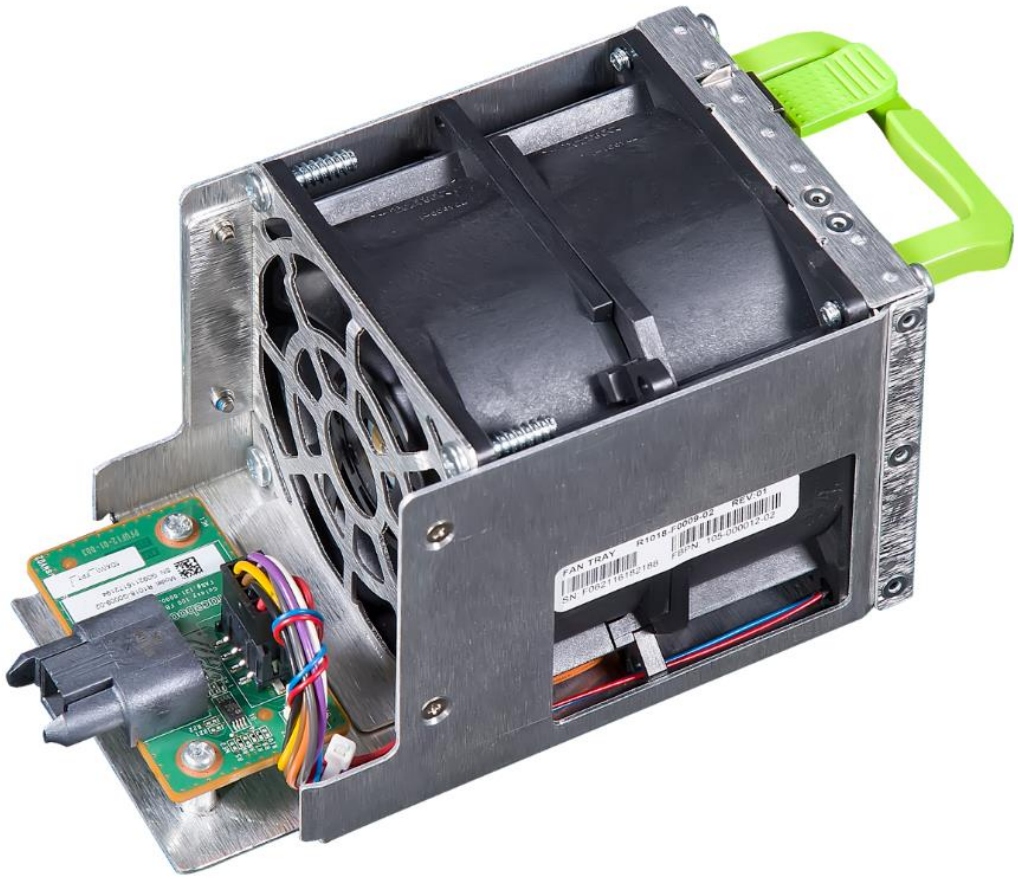


Figure 9-13: Minipack Fan-tray

The following Sanyo Denki CR fan is recommended.

- Sanyo Denki: 9CRA0812P8G001 (80mm x 80mm x 80mm)
  - 63.6W Max
  - Rated speed: 12000 inlet, 11300 outlet
  - Max Airflow: 4.5 M3/min, or 158.9CFM
  - Max Static Pressure: 4.62 inchH2O

Figure 9-14: Minipack Fan

80mm CR fan 9CRA0812P8G001 from Sanyo Denki has the following technical parameters

9CRA0812P8G001	
Item	Description
Rated voltage	12 VDC
Operating voltage	7.0 ~ 13.2 VDC
Input current	5.30A
Input power	63.6W
speed	Front 12000, Rear 11300 RPM +/-10%
Max Air flow at zero static	4.50m3/min, or 158.9CFM
Max Air Pressure	4.62 in-H2O
acoustic	76 dB-A
Lead Wire	

Table 21: Sanyo Denki Fan 9CRA0812P8G001

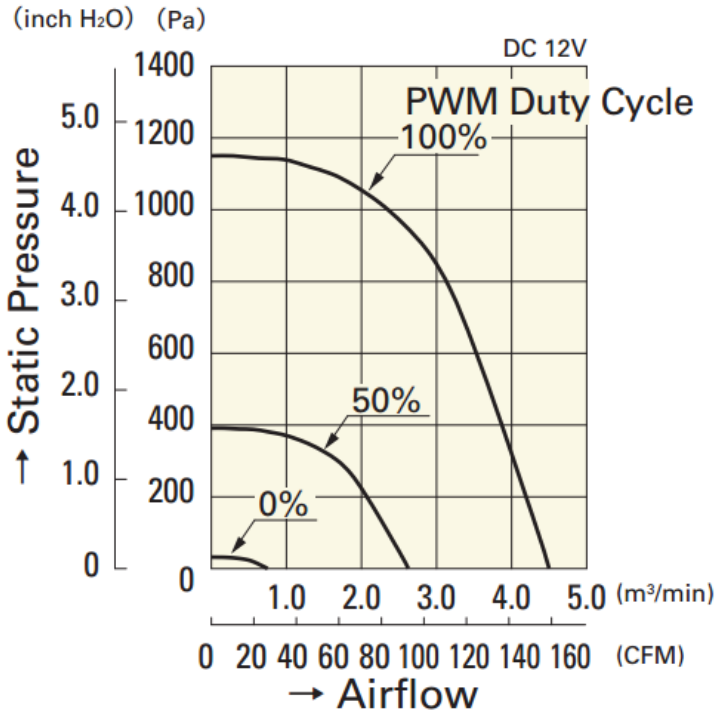


Figure 9-15: PQ Curve of CR Fan 9CRA0812P8G001

9.6.2 Temperature Sensing and Fan Speed Control

Each module card can have multiple temperature sensors to monitor local temperatures. Temperature information needs to be reported to the BMC via system management I2C buses.

Additionally, over-temperature thresholds are configurable and an alert mechanism is provided to enable thermal shutdown and / or an increase in airflow. The sensors are accurate at least to +/- 2C.

The ambient temperature sensor can be *TMP75* from Texas Instruments or equivalent parts from other vendors. Its I2C address can be set to 0x98 to 0x9F. 8x TMP75 temperature sensors can share one I2C bus.

OpenBMC fscd (fan speed control daemon) takes in the temperature readings from various sensors and controls the fan speed through the PWM signals generated by the FCM CPLD.

9.7 FRU and Module Numbering

9.7.1 FRU Name

Each module or FRU has an user identification number. The following table lists the FRU in Minipack system.

Minipack Chassis	Notes
PIM1 – PIM8	PIM #1 to #8
SCM	System Control Module
FAN1 – FAN8	Fan tray #1 to #8
PSU1, PSU2, PSU3, PSU4	PSU #1 to #4

Table 22: FRU Numbering

9.7.2 Slot ID for PIM and SCM

Every PIM and SCM has one unique slot ID.

On SCM and PIM, the following table show the slot ID definition. Software can read the slot ID information from CPLD SLOT_ID register of SCM and PIM.

SLOT_ID[3:0]	Indication
0000	Slot-1, SCM slot
0001	Slot-2, PIM1
0010	Slot-3, PIM2
0011	Slot-4, PIM3
0100	Slot-5, PIM4
0101	Slot-6, PIM5
0110	Slot-7, PIM6
0111	Slot-8, PIM7
1000	Slot-9, PIM8
1001	Unused ID
1010	Unused ID
1011	Unused ID
1100	Unused ID
1101	Unused ID
1110	Unused ID
1111	Unused ID

Table 23: Slot ID

9.7.3 PIM Board ID

Every type of Port Interface Module(PIM) has one unique board ID.

BRD_ID[7:0]	Indication
1111_0000	PIM Type-1: PIM-16Q
1111_0001	PIM Type-2: PIM-4DD
1111_0010	PIM Type-3: PIM-DWDM (TBD later)
1111_0011	PIM Type-4: PIM-MACSEC (TBD later)
1111_0100	PIM Type-5: TBD
1111_0101	PIM Type-6: TBD
1111_0110	PIM Type-7: TBD
1111_0111	PIM Type-8: TBD

Others	Reserved

Table 24: PIM Board ID

9.8 System LED

Minipack chassis and module cards have LED to display the operational status information.

9.8.1 System Information LED (SIM LED)

There are four tri-color LED on the top left corner of the Minipack chassis front panel to display information of the system:

- STS: System Status LED
- FAN: Fan Status LED
- PSU: PSU Status LED
- SMB: Switch Main Board Status LED

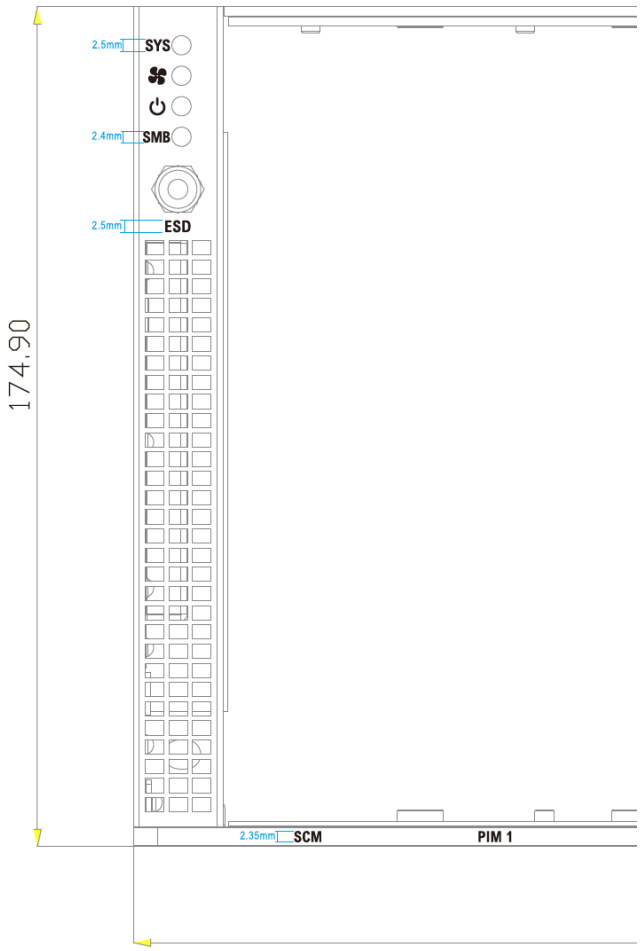


Figure 9-16: Minipack System LED

BMC controls the SIM LED through an I2C IO expander on SIM.

I2C Path for SIM LED Control			
BMC I2C Bus #8 (0-based)	SMB		I2C Bus #8 is used to access PDB, FCM, and fan-trays.
	PCA9548	I2C Addr: 0x70	
I2C Ch #0	PDB-L		
Sub-bus	PCA9548	I2C Addr: 0x71	
I2C Ch #2	PCA9535	I2C Addr: 0x20	

Table 25: I2C Path to Control SIM LED

SIM PCA9535 Bit Mapping

Bit	Name	R/W	Reset Value	Description
15:14	Reserve		1	NA
13	SMB_BLU_L	R/W	1	SMB LED Blue 0: SMB LED Blue is ON 1: SMB LED Blue is OFF
12	SMB_GRN_L	R/W	1	SMB LED Green 0: SMB LED Green is ON 1: SMB LED Green is OFF
11	SMB_RED_L	R/W	1	SMB LED Red 0: SMB LED Red is ON 1: SMB LED Red is OFF
10	PSU_BLU_L	R/W	1	PSU LED Blue 0: PSU LED Blue is ON 1: PSU LED Blue is OFF
9	PSU_GRN_L	R/W	1	PSU LED Green 0: PSU LED Green is ON 1: PSU LED Green is OFF
8	PSU_RED_L	R/W	1	PSU LED Red 0: PSU LED Red is ON 1: PSU LED Red is OFF
7:6	Reserve		1	NA
5	FAN_BLU_L	R/W	1	FAN LED Blue 0: FAN LED Blue is ON 1: FAN LED Blue is OFF
4	FAN_GRN_L	R/W	1	FAN LED Green 0: FAN LED Green is ON 1: FAN LED Green is OFF
3	FAN_RED_L	R/W	1	FAN LED Red 0: FAN LED Red is ON 1: FAN LED Red is OFF
2	SYS_BLU_L	R/W	1	SYS LED Blue 0: SYS LED Blue is ON 1: SYS LED Blue is OFF
1	SYS_GRN_L	R/W	1	SYS LED Green 0: SYS LED Green is ON 1: SYS LED Green is OFF
0	SYS_RED_L	R/W	1	SYS LED Red 0: SYS LED Red is ON 1: SYS LED Red is OFF

OpenBMC software controls the system information LED per Facebook Panel Indicator Specification (16 Appendix A: Facebook Panel Indicator Specification), and the following is the

specific behavior in Minipack. *Please note that Amber is generated by turning on both Red and Green.*

LED	Default Power-On State	Color	Condition
SYS LED	Off	Blue	All FRUs are present, and no FRU-level alarms
		Amber	One or more FRUs are not present; One or more FRUs have alarms
		Blue / Amber flashing (0.5s Blue and 0.5s Amber alternating)	Firmware upgrade in process (BIOS, EEPROM, CPLD, FPGA, etc.)
		Amber flashing	Attention from service technician required
Fan LED	Off	Blue	All fans are present, and are within the normal RPM range
		Amber	One or more fans are not present; One or more fans have out-of-range RPM
PSU LED	Off	Blue	All PSUs are present, and both INPUT OK and PWR OK are asserted for every PSU (accessible through SMB Sys CPLD by BMC)
		Amber	One or more PSUs are not present; One or more PSUs have INPUT OK or PWR OK de-asserted
SMB LED	Off	Blue	No out-of-range voltage and temperature sensors
		Amber	One or more sensors out-of-range

Table 26: System Information LED Definition

9.8.2 PIM LED

PIM has one tri-color status LED (PIM STS LED) to display the status of that PIM. DOM FPGA on PIM provides a control register for STS LED that is accessible by the BMC through its I2C bus #11.

There is one PCA9548 for the BMC to select which PIM to access, and there is one PCA9548 on each PIM for the BMC to select which slave devices on PIM.

I2C Path for PIM LED Control			
BMC I2C Bus #11 (0-based)	SMB		I2C Bus #11 is used to access PIM.
	PCA9548	I2C Addr: 0x70	
I2C Ch #0 ~ #7	PIM #1 ~ #8		
Sub-bus	PCA9548	I2C Addr: 0x73	
I2C Ch #0	DOM FPGA	I2C Addr: 0x31	

Table 27: I2C Path to Control PIM LED

9.8.2.1 DOM FPGA Offset 0x80: STS_LED (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserve		0	NA
3	SYS_LED_AUTOFLASH	R/W	0	LED_RBG 0: turn off Auto Flash 1: turn on Auto Flash
2	SYS_LED_R	R/W	0	LED_RED 0: LED RED is ON 1: LED RED is OFF
1	SYS_LED_G	R/W	0	LED_GREEN 0: LED GREEN is ON 1: LED GREEN is OFF
0	SYS_LED_B	R/W	1	LED_BLUE 0: LED BLUE is ON 1: LED BLUE is OFF

Here is the expected PIM STS LED behavior under OpenBMC control. *Please note that Amber is generated by turning on both Red and Green.*

LED	Default Power-On State	Color	Condition
PIM STS LED	Amber	Blue	No out-of-range voltage and temperature sensors
		Amber	One or more sensors out-of-range

		Amber flashing	Attention from service technician required

Table 28: PIM Status LED Behavior

9.8.3 SCM LED

SCM (System Control Module) CPLD drives the status LED on its front panel, and BMC can control the LED behavior through its I2C bus #2.

I2C Path for SCM LED Control			
BMC I2C Bus #2 (0-based)	SMB		I2C Bus #2 is used to access SCM.
	SCM CPLD	I2C Addr: 0x35	

Table 29: I2C Path to Control SCM LED

9.8.3.1 SCM CPLD Offset 0x08: SYS_LED (Read & Write)

Bit	Name	R/W	Default Value	Description
7:5	Reserved		Reserved	
4	LED_TST_EN	R/W	0	LED Control 0:LED controlled by Bit[3:0]. ***Set the bit to '1' for BMC to control the LED behavior.*** 1:LED controlled by HW Logic – 7 color
3	LED_BLINK	R/W	0	LED_BLINK_EN 0: LED No blink 1: LED Blink is ON
2	SYS_BLUE	R/W	1	LED_BLUE 0: LED BLUE is ON 1: LED BLUE is OFF
1	SYS_GREEN	R/W	0	LED_GREEN 0: LED GREEN is ON 1: LED GREEN is OFF
0	SYS_RED	R/W	0	LED_RED 0: LED RED is ON 1: LED RED is OFF

Here is the expected SCM LED behavior under OpenBMC control. *Please note that Amber is generated by turning on both Red and Green.*

LED	Default Power-On State	Color	Condition
SCM LED	Amber	Blue	No out-of-range voltage and temperature sensors, and the COMe / Mini-Lake is not in powered off or suspended states
		Amber	One or more sensors out-of-range, or the COMe / Mini-Lake is in suspended states (per SCM CPLD register at 0x11).
		Amber flashing	Attention from service technician required

Table 30: SCM Status LED Behavior

The OOB RJ45 port on SCM front panel has industry-standard LED (Link LED and Activity LED) to indicate the status of OOB Ethernet. BMC needs to write '1' to Bit 7 of SCM CPLD register 0x09 to enable the following LED behavior. BMC also has to configure the OOB PHY (Broadcom BCM54210S) registers for the LED.

RJ45 LED	Definition	Behavior
Left / Green	Link	Link up: Green
		Link down: Off
Right / Amber	Activity	TX or RX activity: Blinking Amber
		No activity: Off

Figure 9-17: OOB RJ-45 Port LED Behavior

9.8.3.2 SCM CPLD Offset 0x09 OOB_LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	RJ45_mode_SEL	R/W	1	LED_GREEN 0: Control by SW register 0x09[1:0] 1: Control by OOB PHY. ***Set the bit to '1' for the OOB PHY to control the LED behavior.***
6:4	Reserved	R/W	0	Reserved
3	SFP_LED3_P	R/W	0	LED_GREEN 0: LED GREEN is OFF 1: LED GREEN is ON
2	SFP_LED3_N	R/W	0	LED_ORANGE 0: LED ORANGE is OFF 1: LED ORANGE is ON
1	RJ45_LED2	R/W	0	LED_ORANGE 1: LED ORANGE is ON 0: LED ORANGE is OFF
0	RJ45_LED1	R/W	0	LED_GREEN 1: LED GREEN is ON 0: LED GREEN is OFF

9.8.4 Fan-Tray LED

Each fan-tray has one dual color status LED (FAN STS LED) to display the status of that fan tray. FCM CPLD provides a control register for the LED that is accessible by the BMC through its I2C bus #8. There is one PCA9548 for the BMC to select which FCM to access, and there is one PCA9548 on each FCM for the BMC to select which slave devices on FCM.

I2C Path for Fan-Tray LED Control			
BMC I2C Bus #8 (0-based)	SMB		I2C Bus #8 is used to access PDB, FCM, and fan-trays.
	PCA9548	I2C Addr: 0x70	
I2C Ch #2 I2C Ch #3 (0-based)	FCM-T FCM-B		
Sub-bus	PCA9548	I2C Addr: 0x76	
I2C Ch #0	FCM CPLD	I2C Addr: 0x33	

Table 31: I2C Path to Control Fan-Tray LED

9.8.4.1 FCM CPLD Offset 0x24, 0x34, 0x44, 0x54: FAN1/2/3/4_LED (Read & Write)

Bit	Name	R/W	Reset Value	Description
[7:3]	Reserved	R/W		Reserved
[2:0]	FAN1_LED	R/W	111	FAN1_LED_CTRL[2:0] 000: Under HW control 001: Red OFF, Blue ON 010: Red ON, Blue OFF 101: Blinking Blue 110: Blinking Red 111: OFF If LED is under HW control Present_n=0, Fan_alive_n=0, then Red OFF, Blue ON Present_n=1, Fan_alive_n=x, then Red OFF, Blue OFF Present_n=0, Fan_alive_n=1, then Red ON, Blue OFF

Here is the expected fan-tray LED behavior under OpenBMC control.

LED	Default Power-On State	Color	Condition
Fan-Tray LED	Off	Blue	Fan RPM within the normal range
		Red	Fan RPM out-of-range
		Red flashing	Attention from service technician required

Table 32: Fan-Tray LED Behavior

9.8.5 PSU LED

The BelPower 1500W PSU comes with two LEDs. The LED locations and behavior are shown below.

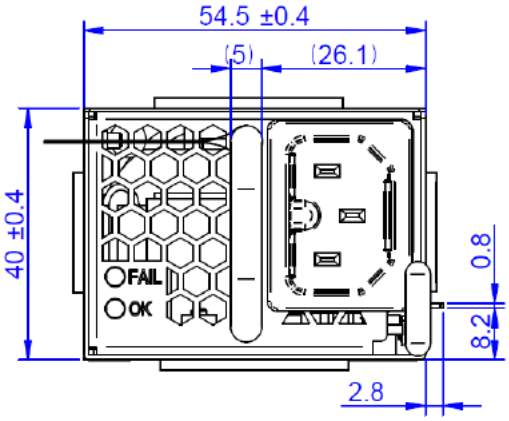


Figure 9-18: BelPower PSU LEDs

POWER SUPPLY CONDITION	GREEN (OK) LED STATUS	AMBER (FAIL) LED STATUS
No AC power to all power supplies	OFF	OFF
Power Supply Failure (includes over voltage, over current, over temperature and fan failure)	OFF	ON
Power Supply Warning events where the power supply continues to operate (high temperature, high power and slow fan)	OFF	Blinking
AC Present/ 12VSB on (PSU OFF)	Blinking	OFF
Power Supply ON and OK	ON	OFF

Table 33: PSU LED Behavior

9.9 Port LED

There is one LED per QSFP port on PIM-16Q. The microserver / CPU accesses the port LED control registers in DOM FPGA through IOB FPGA, and DOM FPGA lights up the port LEDs on PIM-16Q front panel.

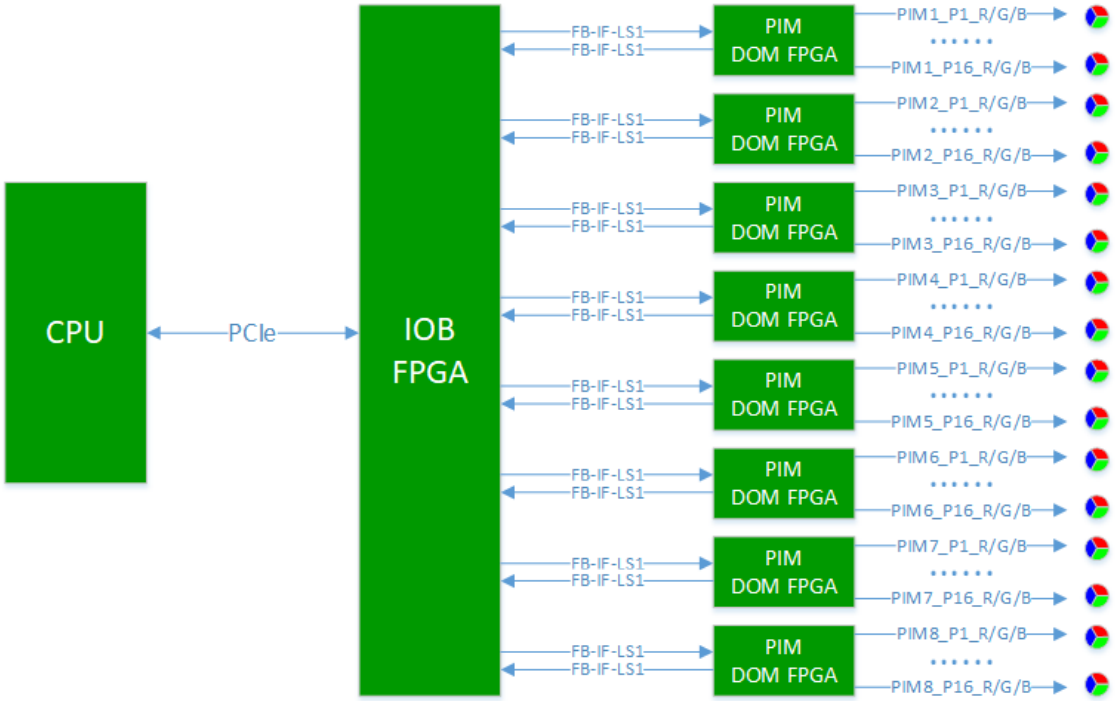


Figure 9-19: Port LED Control Path

The microserver software execute the following sequence to control the port LEDs:

(a) Write to the 8 groups of LED color profile registers to set up the available colors;
(b) Write 0x40 to the QSFP_LED control register;
(c) Choose 1 out of 8 color profile, and select whether the LED is off, constant on (link up) or blinking (twinkling) in the per LED register.

The following are the LED registers for PIM #1.

9.9.1.1 PIM#1 QSFP_LED Control Register

PIM#1 QSFP_LED Control Register				
Offset	Bit	Default	Type	Description
0x0_6084	[0]	0	WO	QSFP_LED_B LED_BLUE 0: LED_BLUE is ON 1: LED_ BLUE is OFF
	[1]	0	WO	QSFP_LED_G LED_GREEN 0: LED_GREEN is ON 1: LED_GREEN is OFF
	[2]	0	WO	QSFP_LED_R LED_RED 0: LED_RED is ON 1: LED_RED is OFF
	[3]	0	WO	QSFP_LED_Blinking 0: No Blinking 1: Blinking
	[6:4]	0	WO	QSFP_LED_Mode 000: AUTO Polling (Black => Red => Orange => Yellow => Green => Blue => Indigo => Violet) 011: LED_Test Mode (bit[2:0]) 100: CPU control LED mode
	[15:7]			Reserved

9.9.1.2 PIM#1 LED_COLOR_1_RG Color Profile Register

PIM#1 LED_COLOR_1_RG				
Offset	Bit	Default	Type	Description
0x0_6090	[7:0]	0	WO	LED_COLOR_1_R 0 : 0% duty cycle

				01: 1/255% duty cycle 02: 2/255% duty cycle …… FE: 254/255% duty cycle FF: 255/255% duty cycle
	[15:8]	0	WO	LED_COLOR_1_G 0 : 0% duty cycle 01: 1/255% duty cycle 02: 2/255% duty cycle …… FE: 254/255% duty cycle FF: 255/255% duty cycle

9.9.1.3 PIM#1 LED_COLOR_1_B Color Profile Register

PIM#1 LED_COLOR_1_B				
Offset	Bit	Default	Type	Description
0x0_6092	[7:0]	0	WO	LED_COLOR_1_B 0 : 0% duty cycle 01: 1/255% duty cycle 02: 2/255% duty cycle …… FE: 254/255% duty cycle FF: 255/255 % duty cycle
	[15:8]			Reserved

9.9.1.4 PIM#1 P1_P2_LED

PIM#1 P1_LED					
Offset	Bit	Default	Type	Name	Description
0x0_60B0	[0]	0	WO	P1-Link-UP	1: Link up 0: No link
	[1]	0	WO	P1-Blink	1: Blinking 0: No Blinking
	[4:2]	000	WO	P1-Color-Map	111 : LED_COLOR_8 110 : LED_COLOR_7 101 : LED_COLOR_6 … 001 : LED_COLOR_2 000 : LED_COLOR_1
	[15:5]			Reserved	

Here is the expected port LED behavior under microserver control.

LED	Default Power-On State	Color	Condition
Port LED	Rotating colors	Blue	Link up
		Amber	Optic transceiver present but link down
		Amber flashing	Attention from service technician required
		Off	Optic transceiver not present

Table 34: Port LED Behavior

9.10 IOB FPGA

9.10.1 Architecture

The main purpose of IOB FPGA on Minipack SMB is to provide a communication path between uServer and Minipack PIM cards.

There are eight PIM cards in Minipack. Each PIM card is allocated 32KB of memory. These PIM cards are directly mapped into PCIe memory through SLPC bus. IOB requests 512KB of memory at PCIe bus to support total 256KB of PIM card memory, with the remaining half used as general registers or other registers.

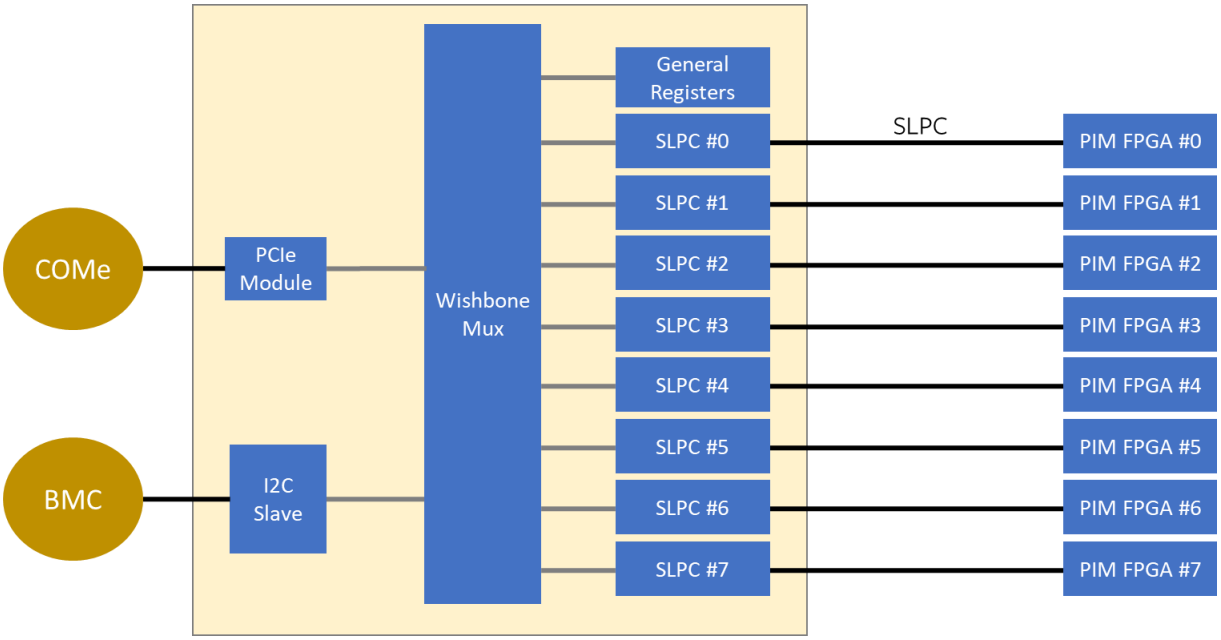


Figure 9-20 Minipack FPGA System Diagram

9.10.2 Major Modules

9.10.2.1 PCIe Core

PCIe core is an IP from the FPGA supplier. With some TLP layer logic and user interface logic, the PCIe module bridges the PCIe interface to Wishbone interface, which is the major bus of FPGA internal user logic.

The Lattice PCIe core provides TLP interface. TLP RX is sent to ur_gen, wb_tlc and rx_crpr. The TX TLP from ur_gen and wb_tlc are arbitrated at tx_arb before sending to PCIe core.

Ur_gen processes the unsupported TLP requests found by PCIe core, and generates Completion TLPs. Unsupported TLP requests in this module are defined as IO read/write, and memory access to the address not defined by BARs. IO read/write is non-posted TLP that requires Completion. Since this module doesn't support IO read/write, these IO read/write TLPs are terminated at ur_gen to generate Completion. Memory write is posted TLP that doesn't require Completion. However, memory write to incorrect address is terminated at ur_gen to generate Completion in the same ways as memory read to locked address.

Rx_crpr counts the TLP being processed and provides credit info to IP core. PCIe IP core will send Flow Control DLLP to free its credits at the peer. The PCIe core also provides peer's credit status to user interface, but user interface ignores these credit info, because this end-point implementation doesn't consume a lot of credits – it just responses to TLP request of 1DW data, no DMA is supported.

WB_TLC is responsible for adapting 1DW TLP memory requests into WISHBONE transactions. 1 DW TLPs are only supported since this is a low throughput control plane interface which reduces required logic. Whenever a valid memory read/write TLP is received, a corresponding Wishbone transaction is initiated. For each memory read, a Completion TLP is generated by this module and waiting to be sent to PCIe core through tx_arb. Note that a FIFO structure in this module allows user logic to run at a different clock freq. All the TLP layer circuit runs at 125MHz. FPGA user logic circuits runs at 50MHz.

WB_16:32 is to convert the DW of 16bit data to 32bit data on the Wishbone bus at user logic interface. All the user registers are defined as 32bit. These user registers support Byte selection. Software can write/read 8bit of the register at each access.

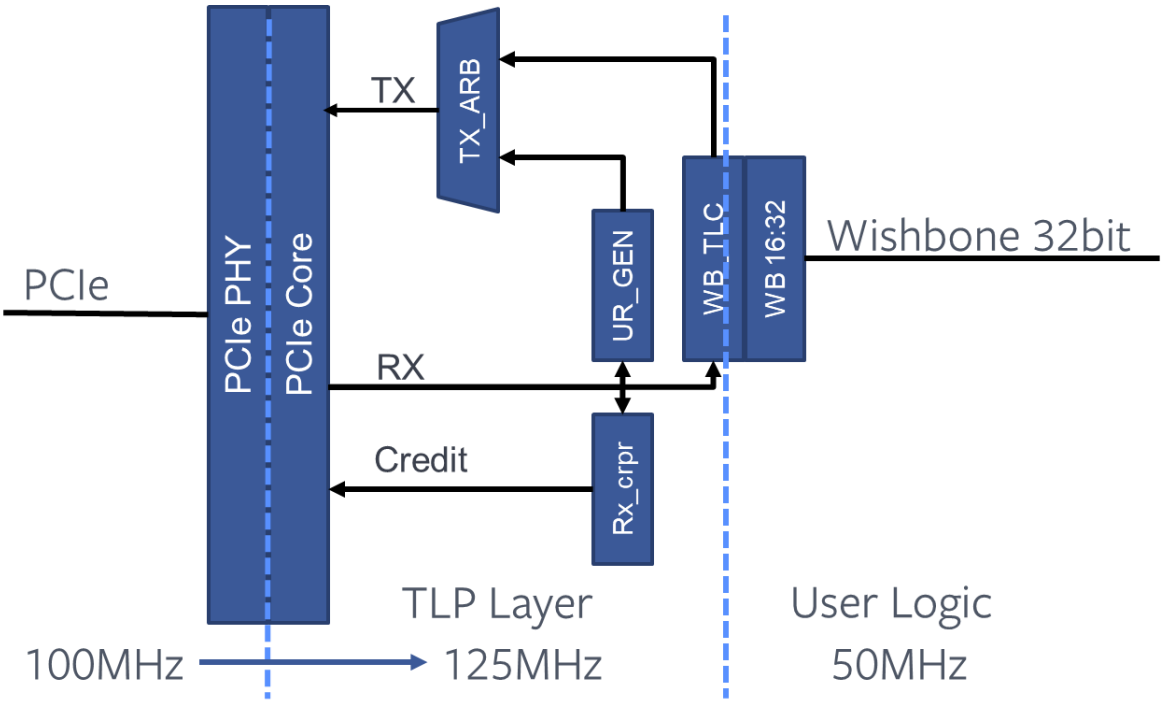


Figure 9-21 IOB FPGA Clock domain

9.10.2.2 I2C Slave

i2c_to_wb_top is leveraged from an i2c slave core downloaded from opencores.org. Some changes have been made to better serve our application. The major changes are inside i2c_to_wb_if.v, especially on i2c_offset_r. Please see the comments in the module for details.

i2c_reg_indirect_if.v is designed to convert the I2C slave register access Wishbone bus into indirect register access Wishbone bus.

Alternatively, i2c_reg_direct_8b_if.v is designed to support 256x8bit direct register access. This direct register option is preferred for small sized design.

The I2C slave 7bit device ID is configurable. Current setting is 0x50.

Following is a typical i2c write transaction and read transaction to these registers. The DATA sessions in these transactions have be consecutive.

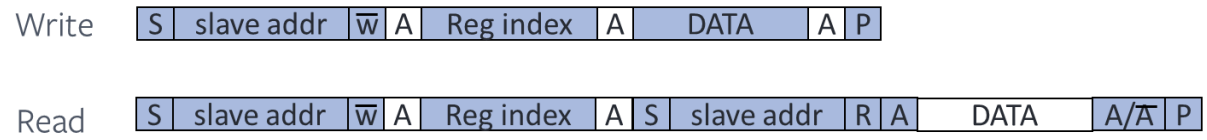


Figure 9-22 I2C Read and Write Transactions

9.10.2.3 Wishbone Mux

The Mux supports 2 master interfaces and total of 16 slave interfaces. PCIe and BMC I2C are the two masters that are hooked up on mux two master interfaces. PCIe module is on mux master port 0; BMC I2C module is on mux master port 1. The slave devices on the bus can be found in later chapter where memory mapping is defined. The Wishbone bus of these slaves has 32bit data bus.

This mux in Minipack design assigned PCIe path higher priority over BMC if both requests arrive simultaneously. Otherwise this mux serves the request in a first-come-first-serve manner. In real test, consecutive transactions on PCIe path always has enough gap to avoid BMC path starvation.

In order to make the memory space compact, there is a secondary mux on the Wishbone bus to interface some internal registers in IOB FPGA. This secondary mux is identical as the primary one in the module design.

9.10.2.4 SLPC

SLPC is a simplified Intel LPC protocol between IOB FPGA on SMB and DOM FPGA on PIM. SLPC has 8 signals – one reference clock signa, one bit of #FRAME, five bits of LAD[4:0] and one bit of #IRQ. #IRQ handles interrupt request from PIM, while #FRAME and LAD are the major signals for data transfer. #FRAME is the frame signal to identify the start of a transaction; LAD[3:0] is the four bit nibble that carries the data; LAD[4] is parity bit for LAD[3:0].

In this SLPC protocol, only memory read/write is supported. The address supported in this protocol is 16bit wide for total of 64KB memory space. The data bus supported in this implementation is 16bit to be compatible with PCIe core. We can scale the data bus to 32bit for future design if needed.

Following table describes the memory read operation on SLPC.

Field	# of clocks	LAD Driver	#FRAME	LAD[3:0]	Description
Start	1	Master	0	0000	Start of a transaction.
TYPE	1	Master	1	0100	Cycle Type is memory read.
ADDR	4	Master	1	address	16bit of address. Most significant nibble comes first.

TAR	2	Master	1		Turn around. LAD=1111 at the first cycle; then tri-state at the second cycle.
SYNC	4	Slave	1	SYNC	Slave drives LAD = 0101, until the last cycle to drive LAD = 0000.
DATA	4	Slave	1	Data	16bit of data. Least significant nibble comes first.
TAR	2	Slave	1		Turn around. LAD=1111 at the first cycle; then tri-state at the second cycle.
Total	18				Up to 18cycles to read 16bit of data.

Table 35 SLPC16 memory read cycles

Following table describes the memory write operation on SLPC.

Field	**# of clocks**	**LAD Driver**	**#FRAME**	**LAD[3:0]**	**Description**
Start	1	Master	0	0000	Start of a transaction.
TYPE	1	Master	1	0110	Cycle Type is memory write.
ADDR	4	Master	1	address	16bit of address. Most significant nibble comes first.
DATA	4	Master	1	Data	16bit of data. Least significant nibble comes first.
TAR	2	Master	1		Turn around. LAD=1111 at the first cycle; then tri-state at the second cycle.
SYNC	4	Slave	1	SYNC	Slave drives LAD = 0101, until the last cycle to drive LAD = 0000.
TAR	2	Slave	1		Turn around. LAD=1111 at the first cycle; then tri-state at the second cycle.
Total	18				Up to 18cycles to write 16bit of data.

Table 36 SLPC16 memory write cycles

Note that although there is such SLPC bus between IOB FPGA and PIM FPGA, memory access to PIM FPGA is transparent to software. Software can do normal 32bit register access to PIM memory space without the awareness of the SLPC bus, except that the latency of IO expander access over SLPC takes longer.

9.10.3 Interrupt

IOB FPGA collects all the interrupt sources and saves them in reg0x2C. Following diagrams show these interrupt trees.

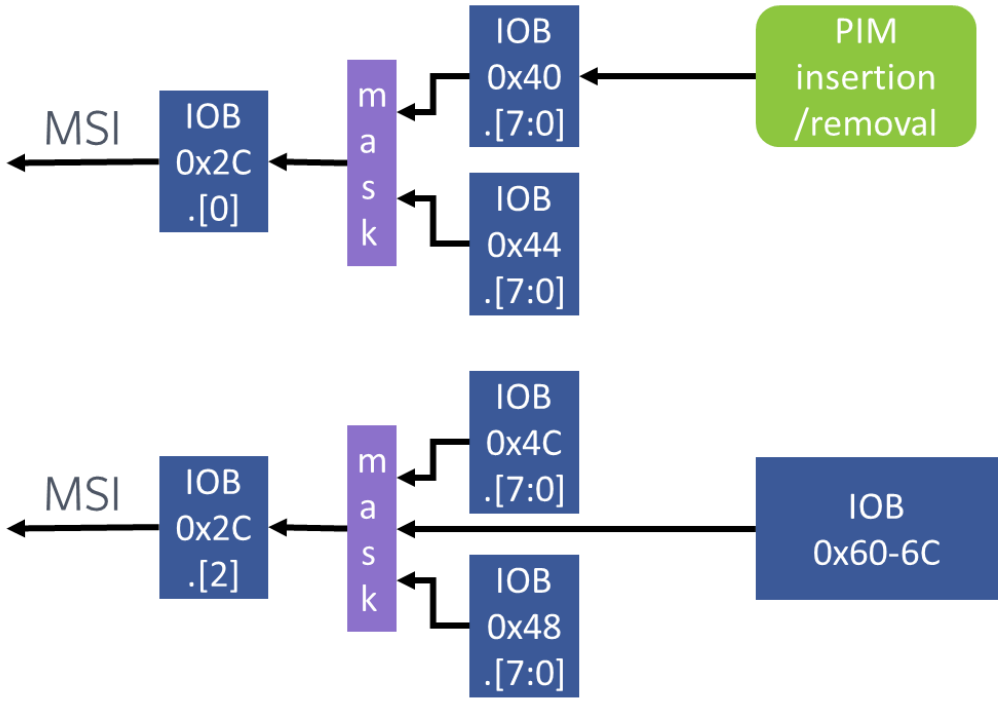


Figure 9-23 MSI[0] and MSI[2]

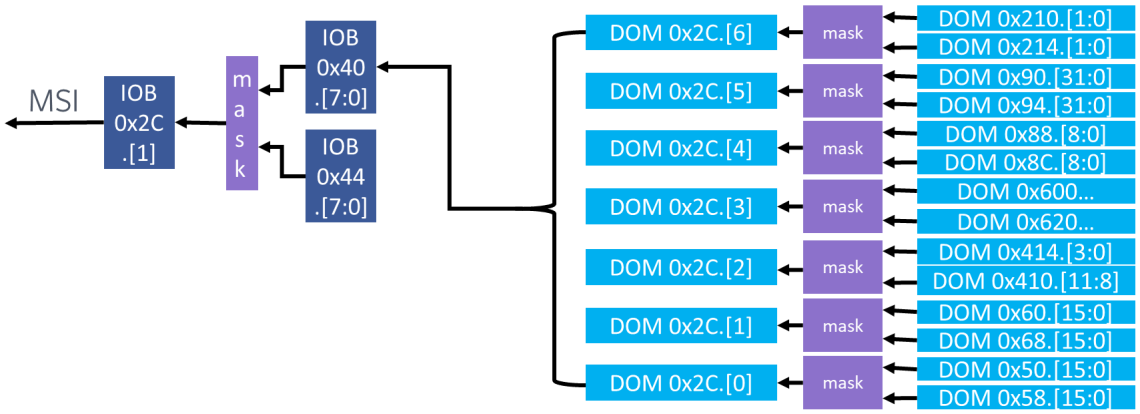


Figure 9-24 MSI[1]

9.11 DOM FPGA

9.11.1 Architecture

The FPGA in this design is used on the network switch unit control plane to handle the communication between CPU and the peripheral devices, and between BMC and the peripherals.

The key function of the FPGA is the DOM engine in it. This DOM engine is to support SFF-8636, Luxtera OBO and future ACMIS requirement. The DOM engine to be enabled on Minipack PIM card will be named as DOM1.

The major functions of the FPGA functions are

- To provide PCIe 32bit data access to CPU;
- To provide I2C connection for BMC access;
- To allow CPU and BMC to access QSFP devices through QSFP I2C bus;
- To collect QSFP DOM data either automatically or manually through software control;
- To provide max QSFP temperature reading;
- To allow CPU and BMC to access/control QSFP low speed IO signals;
- To generate the LED data streams for port LEDs;

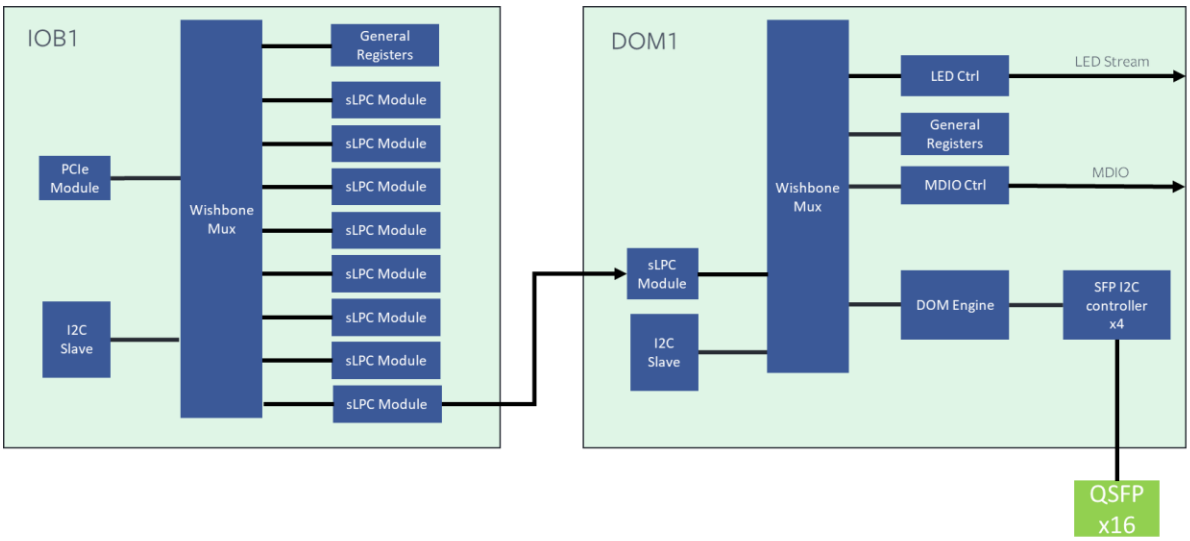


Figure 9-25 FPGA Architecture

9.11.2 Major Modules

9.11.2.1 SLPC

SLPC is a simplified Intel LPC protocol between FPGA and its IO-expander. SLPC has 8 signals -- one reference clock signal, one bit of #FRAME, five bits of LAD[4:0] and one bit of #IRQ. #IRQ handles interrupt request from IO expander, while #FRAME and LAD are the major signals for data transfer. #FRAME is the frame signal to identify the start of a transaction; LAD[3:0] is the four bit nibble that carries the data; LAD[4] is parity bit for LAD[3:0].

In this SLPC protocol, only memory read/write is supported. The address supported in this protocol is 16bit wide for total of 64KB memory space. The data bus supported in this implementation is 16bit to be compatible with PCIe core. We can scale the data bus to 32bit for future design if needed.

Following table describes the memory read operation on SLPC.

Field	# of clocks	LAD Driver	#FRAME	LAD[3:0]	Description
Start	1	Master	0	0000	Start of a transaction.
TYPE	1	Master	1	0100	Cycle Type is memory read.
ADDR	4	Master	1	address	16bit of address. Most significant nibble comes first.
TAR	2	Master	1		Turn around. LAD=1111 at the first cycle; then tri-state at the second cycle.
SYNC	4	Slave	1	SYNC	Slave drives LAD = 0101, until the last cycle to drive LAD = 0000.
DATA	4	Slave	1	Data	16bit of data. Least significant nibble comes first.
TAR	2	Slave	1		Turn around. LAD=1111 at the first cycle; then tri-state at the second cycle.
Total	18				Up to 18cycles to read 16bit of data.

Table 37 SLPC16 memory read cycles

Following table describes the memory write operation on SLPC.

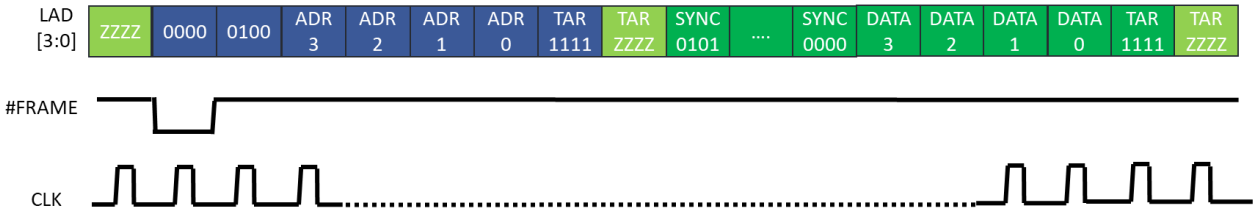
Field	# of clocks	LAD Driver	#FRAME	LAD[3:0]	Description
Start	1	Master	0	0000	Start of a transaction.
TYPE	1	Master	1	0110	Cycle Type is memory write.

ADDR	4	Master	1	address	16bit of address. Most significant nibble comes first.
DATA	4	Master	1	Data	16bit of data. Least significant nibble comes first.
TAR	2	Master	1		Turn around. LAD=1111 at the first cycle; then tri-state at the second cycle.
SYNC	4	Slave	1	SYNC	Slave drives LAD = 0101, until the last cycle to drive LAD = 0000.
TAR	2	Slave	1		Turn around. LAD=1111 at the first cycle; then tri-state at the second cycle.
Total	18				Up to 18cycles to write 16bit of data.

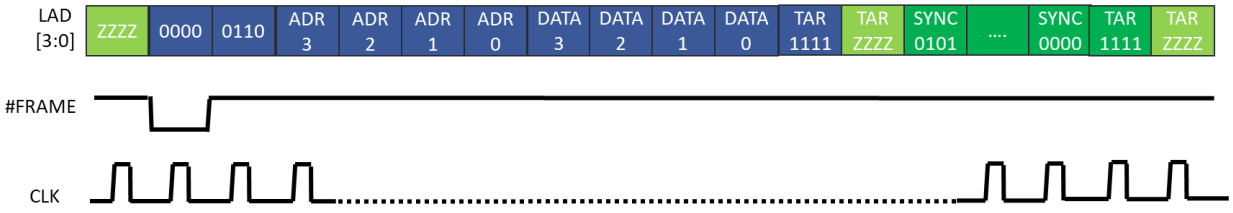
Table 38 SLPC16 memory write cycles

Note that although there is such SLPC bus between FPGA and its IO expander, memory access to FPGA IO expander is transparent to software. Software can do normal 32bit register access to IO expander memory space without the awareness of the SLPC bus, except that the latency of IO expander access over SLPC takes longer.

Following waveform illustrates a SLPC 16bit read transaction. Two such transactions make up one 32bit register access. The blue cycles are driven by the IOB master; the dark green cycles are driven by the DOM slave; the other cycles are tri-state pulled high.



Following waveform illustrates a SLPC 16bit write transaction. Two such transactions make up one 32bit register access. The blue cycles are driven by the IOB master; the dark green cycles are driven by the DOM slave; the other cycles are tri-state pulled high.



9.11.2.2 I2C Slave

i2c_to_wb_top is leveraged from an i2c slave core downloaded from opencores.org. Some changes have been made to better serve our application. The major changes are inside i2c_to_wb_if.v, especially on i2c_offset_r. Please see the comments in the module for details.

i2c_reg_indirect_if.v is designed to convert the I2C slave register access Wishbone bus into indirect register access Wishbone bus.

Alternatively, i2c_reg_direct_8b_if.v is designed to support 256x8bit direct register access. This direct register option is preferred for small sized design (not used in Minipack design).

The I2C slave 7bit device ID is configurable. (IOB I2C SLAVE DEV ID IS 0X35; PIM DOM SLAVE DEV ID IS 0X60)

Following is a typical i2c write transaction and read transaction to these registers. The DATA sessions in these transactions have be consecutive.

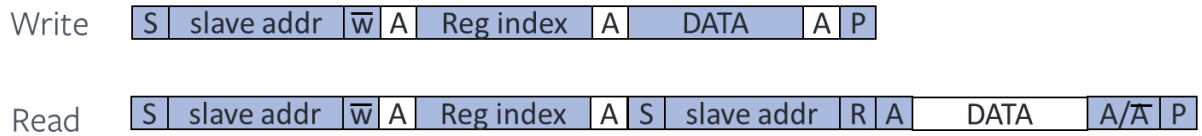


Figure 9-26 I2C Read and Write Transactions

9.11.2.3 Wishbone Mux

The Mux supports 2 master interfaces and total of 16 slave interfaces. PCIe and BMC I2C are the two masters that are hooked up on mux two master interfaces. PCIe module is on mux master port 0; BMC I2C module is on mux master port 1. The slave devices on the bus can be found in later chapter where memory mapping is defined. The Wishbone bus of these slaves has 32bit data bus.

This mux in Minipack design assigned PCIe path higher priority over BMC if both requests arrive simultaneously. Otherwise this mux serves the request in a first-come-first-serve manner. In real test, consecutive transactions on PCIe path always has enough gap to avoid BMC path starvation.

9.11.2.4 DOM Engine

Following is a list of major features supported in the DOM engine.

- Support both DOM data collection and real time I2C access.
- Support up to four pages of DOM data collection, with four global descriptors to specify page/bank/address/length of the target transceiver page.
- DOM function has auto mode and manual mode support.
- Real time I2C access supports up to four descriptors per quad channel; each descriptor supports up to 128B of data.

- Up to eight RTC controllers for total of 32 I2C channels. In minipack, only four RTC controllers are used.
- Transceiver max temperature extraction.
- Up to 32 point-to-point transceiver channels. In Minipack-16Q, only 16 are used. For PIM-4DD and PIM-16O only four are used.
- Up to eight I2C controllers. In Minipack, only four are used.
- Mix SCL freq (400KHz and 1MHz) support to be compatible with both SFF-8636 and ACMIS.
- OBO quad channel support

For DOM data collection, FPGA collects data from all the transceivers automatically or under software control. The target SFF I2C EEPROM should conform to MSA SFF-8636, with DOM data located at lower page 0. To support future ACMIS spec, the FPGA design has allocated 4 pages of 128B data for DOM function, which is defined by four global descriptors. Real time I2C access to QSFP is to access up to four pages of 128B of data to QSFP. Real time access has higher priority over DOM data collection.

These functions are achieved with an I2C core wrapped up as a generic I2C controller. This generic I2C controller supports

- 7bit slave address;
- 1B and 2B offset address; optionally 0B address for “i2c probe” type of access;
- Up to 128B write data; optionally 0B write for “i2c probe” type of access;
- multiple byte read up to 128B.

This I2C controller is integrated with DOM Qport controller and scheduler to support both DOM data collection and real time I2C access. To support OBO module, this DOM engine uses one I2C controller to handle the access of four transceiver channels, with 1:4 mux to split the I2C bus at FPGA pins to prevent the I2C quad from being locked up by one bad transceiver. Total of four controller groups are designed to support 16 channels of transceivers. The design can easily scale with six controller groups to support 24 channel transceivers, and eight controller groups to support 32 channel transceivers.

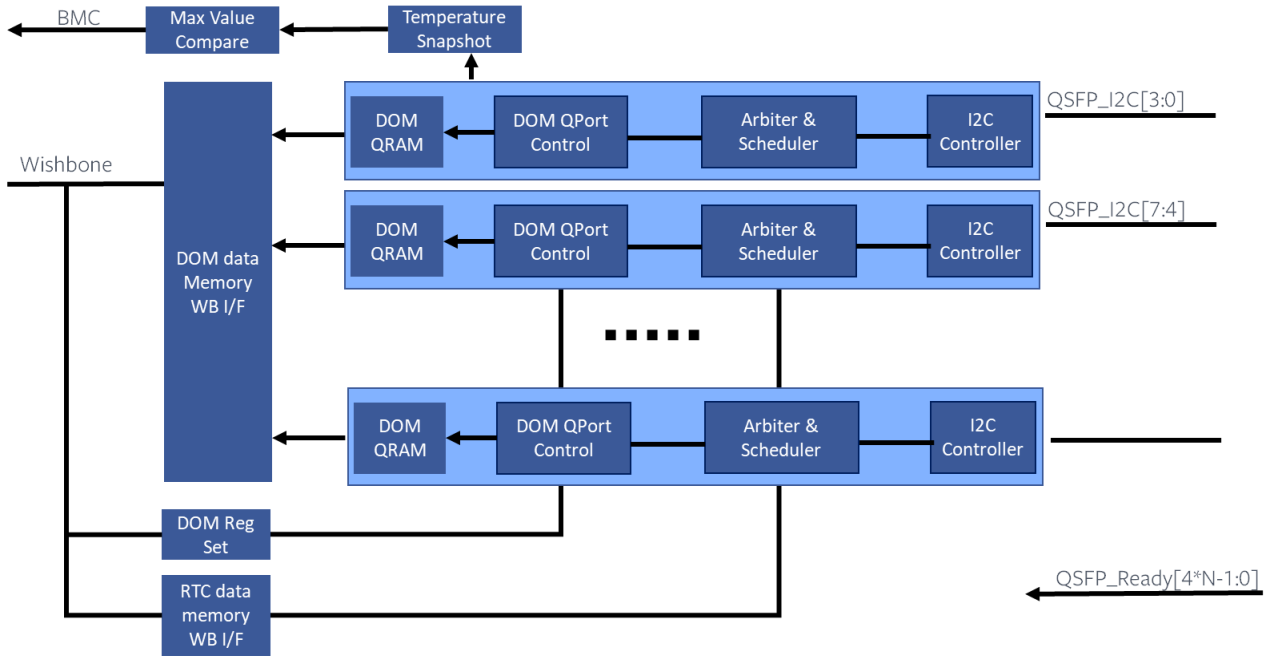


Figure 9-27 DOM Architecture

The memory address space of DOM I2C controller is split into four major categories. One is DOM global control/status memory space for DOM data collection; one is real time access control/status space for real time I2C access, the DOM data memory space, and the real time access data memory space.

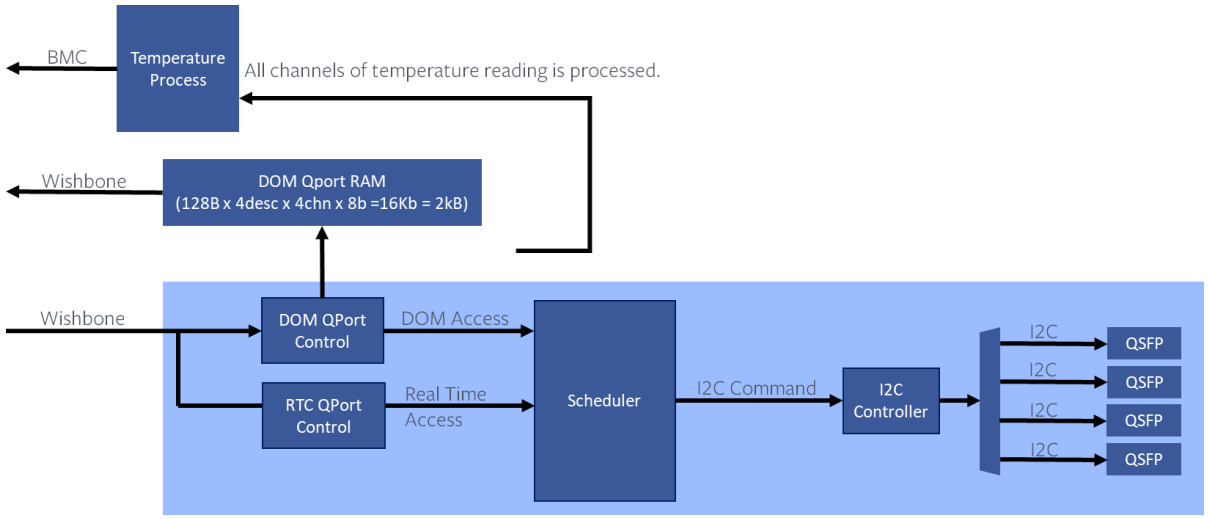


Figure 9-28 DOM engine

In DOM data collection, software instructs FPGA to collect up to 4x128B data from each of the eligible QSFPs – that is if QSFPs are present and out of reset. A set of DOM control and status registers are defined for software to interact with the FPGA DOM engine. There are four descriptors to instruct DOM engine to collect data from up to four desired page/banks of a transceiver. Descriptor #0 should be always set on lower page 0 to help FPGA to extract transceiver temperature data for software to monitor transceiver thermal status. DOM Qport controller will round-robin among the four transceiver channels in its domain, and on a specific channel it round-robins the four descriptors if they are valid. If a descriptor is invalid (not enabled), the corresponding descriptor memory page will be filled with zeros.

Following diagram illustrates DOM Qport controller behaviors.

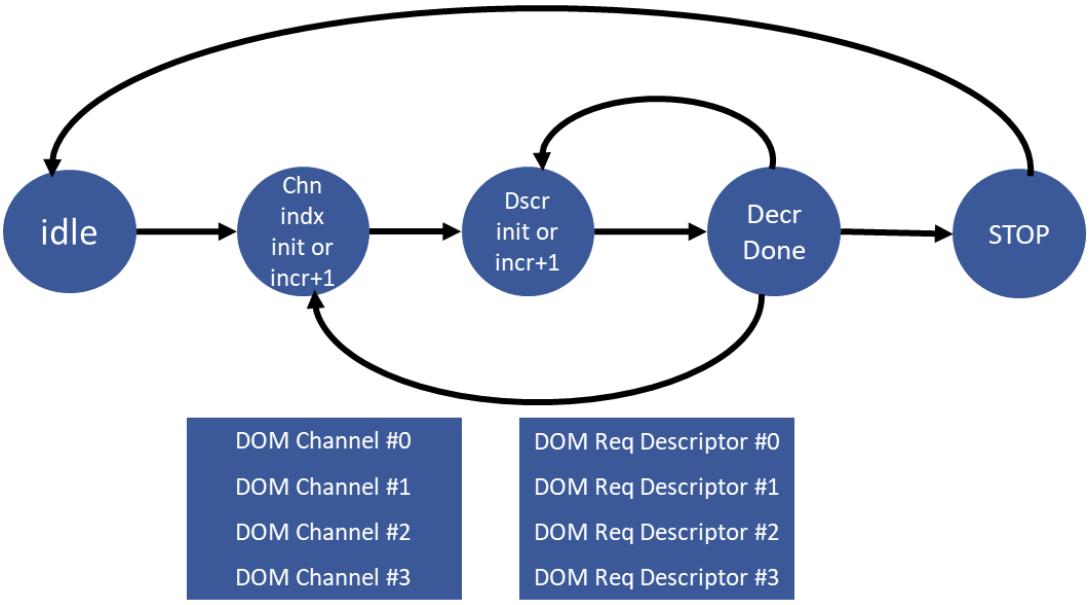


Figure 9-29 DOM engine state transfer

When QSFP I2C transaction is complete, the status is reported in the DOM status registers, so software can pick up the valid data. Once data is fetched by software, a new DOM data collection session can start again. This type of DOM data collection is called manual mode DOM collection.

If software doesn't fetch the collected DOM data, a watchdog timer can be enabled to expire eventually to restart the DOM engine. The watchdog timer expiration time is configurable by user. This type of DOM data collection is called auto mode DOM collection.

BMC is specifically interested in QSFP temperature reading, so a circuit to collect and process such temperature data is designed just to provide BMC the max QSFP temperature reading. This feature is available with auto mode DOM collection being enabled. If DOM manual mode is enabled, software needs to periodically restart the data collection to refresh temperature data.

I2C real time access is supported in the similar way as DOM function. There is one real time access controller per quad channel group. Each real time access controller can support up to 4 descriptors; each descriptor can be configured to transfer up to 128Byte of data. Following diagram illustrates the state transfer in the RTC controller.

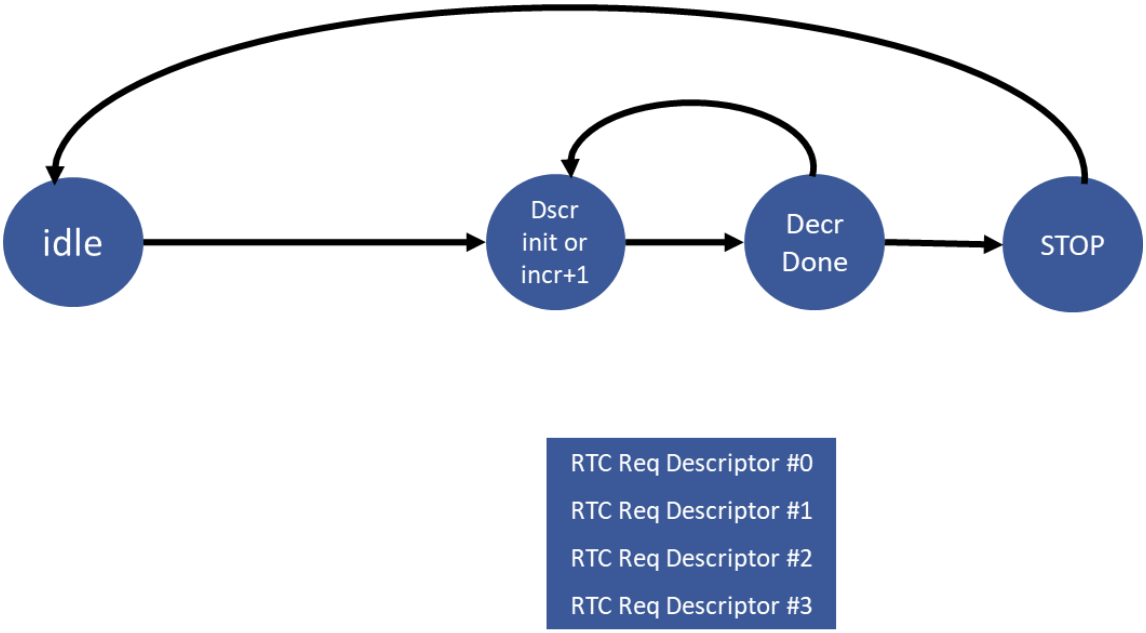


Figure 9-30 RTC state transfer

DOM data collection and real time access are scheduled by Qport scheduler. When real time QSFP access collides with DOM QSFP access, the real time access has higher priority. Real time access can interrupt DOM data collection in session whenever possible, so real time access can complete as soon as possible. DOM transaction can't interrupt real time access transaction. Until all the RTC descriptors have been serviced, the scheduler will not allow DOM collection to start. As shown in the next diagram, RTC (real time control) request has higher priority over DOM.

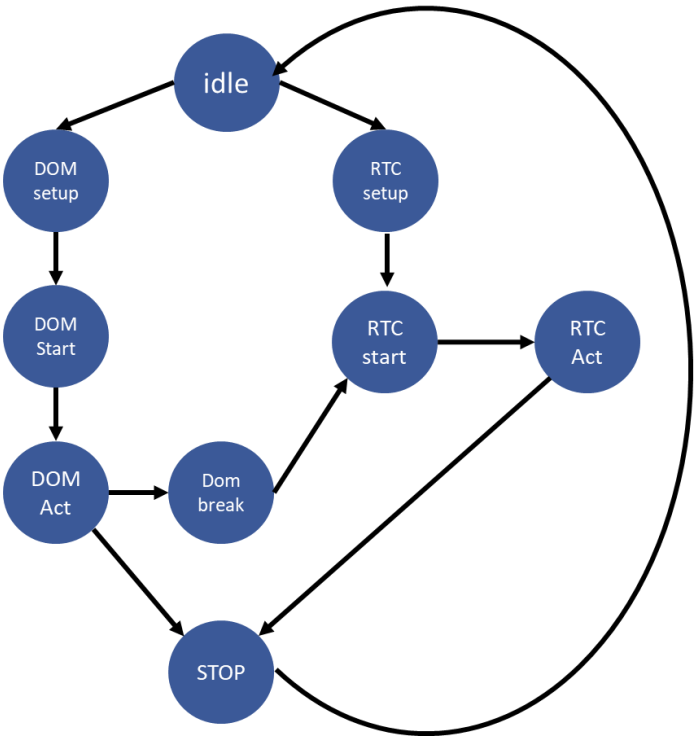


Figure 9-31 Schedulre state transfer

Qport scheduler keeps track of channel index it serves. If the incoming granted request has a different channel index than previous value, a channel setup state will be scheduled for OBO application if this feature is enabled.

Qport scheduler also tracks the previous page/bank index for each of the four channels in the scheduler's domain. If the incoming granted request has a different page/bank index than previous, a page/bank byte write operation will be scheduled by this scheduler.

Although DOM data collection can be interrupted by RTC request, DOM data collection can't be interrupted too frequently to waste I2C cycles. DOM data collection won't be interrupted at channel setup phase or page/bank byte write phase. DOM operation can only be interrupted when DOM is at data collection phase after at least one data byte has been collected, to make sure DOM operation won't be starved by frequent RTC interrupts. If a DOM function is interrupted by RTC, the current operation metadata is stored in the scheduler waiting for DOM re-entry.

These Qport controller and scheduler have many complex state transfers. To avoid deadlock, watchdog timers are designed to detect any deadlock event, so the deadlock can be reset if reset-on-deadlock feature is enabled and error can be flagged.

DOM data memory is 2KB for each quad transceiver group, which consumes one FPGA block RAM. Total of four block RAM for 16 transceivers, six block RAMfor 24 transceivers, and eight block RAM for 32 transceivers.

128B read memory and 128B write memory are needed for each RTC descriptor. There are four descriptors per RTC controller, so total of 128B*2*4=1KB memory is needed for each RTC controller, which consumes one FPGA block RAM. Total of four block RAM is needed for total of 16 transceivers, six block RAM for 24 transceivers, and eight block RAM for 32 transceivers.

RTC supports up to 128B of consecutive data access for each RTC descriptor. SFF-8636 only allows up to 4 byte of sequential write. ACMIS extends the sequential write support up to 8 Bytes for non-volatile memory. The number of sequential write to volatile memory is not limited in ACMIS, but the writing will roll over to the first byte of the same page when it hits the end of a 128byte page. These memory supports both CPU write and read without impacting I2C real time access.

9.11.2.5 I2C Master Core

I2C master core is downloaded from opencores.org. The i2c_master_top.v is stripped off and discarded. i2c_controller.v is designed to interact with i2c_master_byte_ctrl.v directly to support i2c function level transaction. i2c_controller.v doesn't have Wishbone interface. Instead, it has register interface exposed to user interface. A Wishbone register module is needed to hook up this module to Wishbone bus.

This master controller supports the typical i2c write and read transactions illustrated in above figures. Its registers are defined in "Register Definition" section.

9.11.2.6 Port LED Control

In legacy switch design, we usually use switch ASCI microcontroller to generate LED data stream. In this design, port LED data will be generated from FPGA.

A color profile is defined by three RGB profile registers (RGB). Each register defines up to 15 level of its brightness. There are eight of such RGB profiles defined to support up to 8 unique color profiles.

Each port LED is specified with 1 profile, plus on/off control and blink control. Eventually the LED data will be shifted out in serial in following pattern for external fanout.

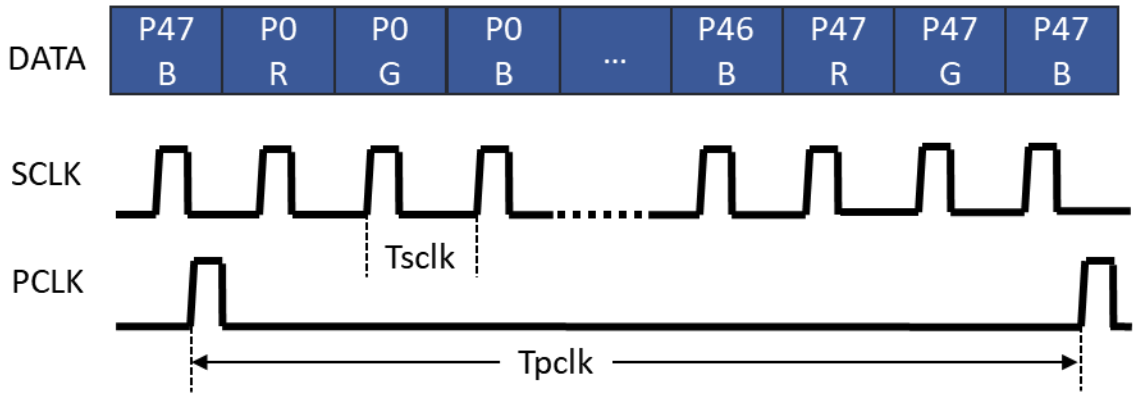


Figure 9-32 LED stream

We need to calculate Tsclk and Tpclk.

Tpclk = 144*Tsclk.

Since there are 15 PWM steps for each color, and let's allow n*Tpclk for one 15PWM step, the complete 15 PWM steps takes Tpwm_cyc = 15*n*144*Tsclk = 2160*n*Tsclk.

Let's use 100 f/s refresh cycle, so 2160*n*Tsclk = 10ms.

n*Tsclk = 10ms/2160 < 5us.

It is safe if we choose n =1, Tsclk = 1us; Tpclk = 144us; Tpwm_cyc = 2.16ms.

Here is how it works. SCLK will be active every 1us. One frame of LED data of 48ports will take 144us. Every frame will be one PWM step – one PWM pulse every 144us. 15 of PMW steps take 2.16ms.

Following is the port LED control design diagram. This design uses time-division-multiplex concept to drive external logic with a serial interface. The external logic could be discrete shifters, or external CPLD, or simply FPGA user logic.

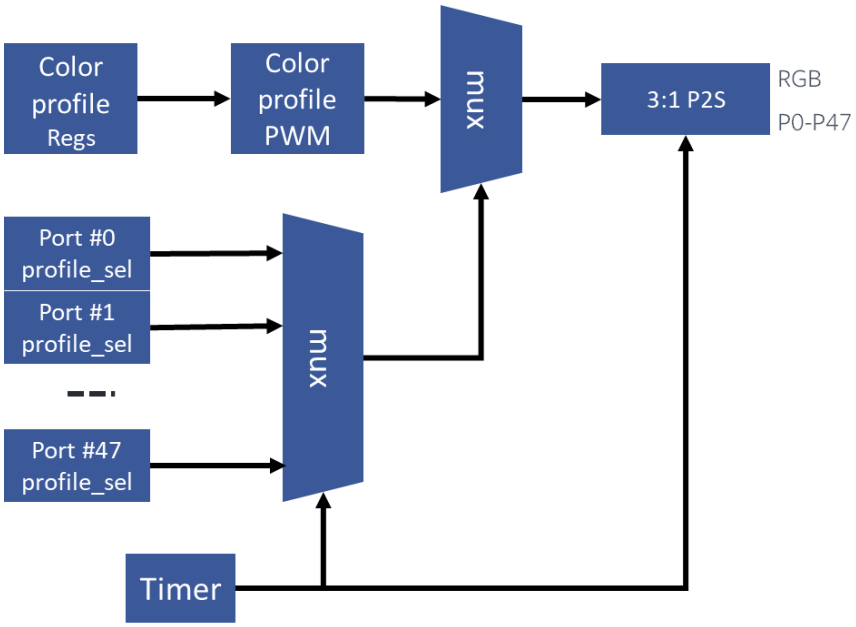
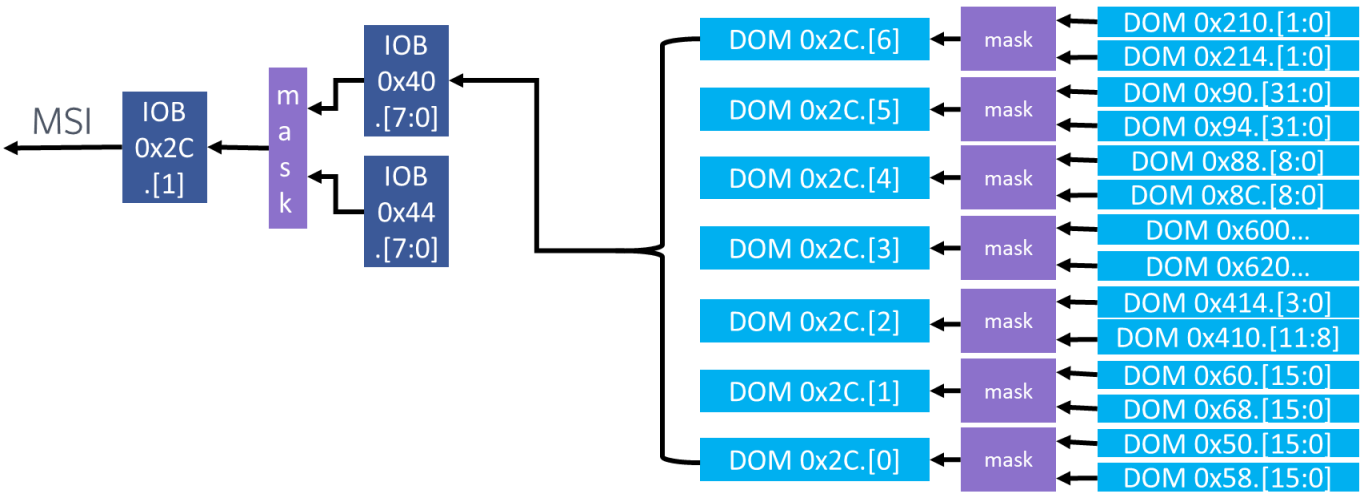


Figure 9-33 LED diagram

9.11.3 Interrupt

DOM FPGA collects interrupt in register 0x2C and asserts the interrupt to IOB FPGA through INT_N pin. Following diagram illustrate the interrupt tree on DOM FPGA and its upstream in IOB FPGA.



10 Programming Interfaces

10.1 SMB System CPLD Register Descriptions

10.1.1 Offset 0x00: Board Info (Read Only)

Bit	Name	R/W	Reset Value	Description
7	Reserve			NA
6:4	BRD_REV_ID[2:0]	R		
3:2	Reserved	NA	0	
1:0	PCB_Version[1:0]	R	00	00 for R0A 01 for R0B 10 for R0C 11 for R01

10.1.2 Offset 0x01: CPLD Version (Read Only)

Bit	Name	R/W	Reset Value	Description
7	Reserved	R	0	
6	RELEASE_STA	R	0	Released Bit 0= not released, 1= Released version after PVT
5:0	CPLD_VER	R		CPLD Revision[5:0]

10.1.3 Offset 0x02: CPLD Sub version (Read)

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_Sub_Version	R	1	Used for HW debug only

10.1.4 Offset 0x03: Power Module Status-L (Read Only)

Bit	Name	R/W	Reset Value	Description
7	PSU_L2_INPUT_OK	R	1	0: Fail 1: normal
6	PSU_L2_PRESENT_L	R	1	0: present 1:not present
5	PSU_L_PWR_OK	R	1	0: Fail 1: normal
4	PSU_L2_SMB_ALERT	R	1	0: Fail 1: normal
3	PSU_L1_INPUT_OK	R	1	0: Fail 1: normal
2	PSU_L1_PRESENT_L	R	1	0: present 1:not present
1	Reserved	R	1	
0	PSU_L1_SMB_ALERT	R	1	0: Fail 1: normal

10.1.5 Offset 0x04: Power Module Status-R (Read Only)

Bit	Name	R/W	Reset Value	Description
7	PSU_R2_INPUT_OK	R	1	0: Fail 1: normal
6	PSU_R2_PRESENT_L	R	1	0: present 1:not present
5	PSU_R_PWR_OK	R	1	0: Fail 1: normal
4	PSU_R2_SMB_ALERT	R	1	0: Fail 1: normal
3	PSU_R1_INPUT_OK	R	1	0: Fail 1: normal
2	PSU_R1_PRESENT_L	R	1	0: present 1:not present
1	Reserved	R	1	
0	PSU_R1_SMB_ALERT	R	1	0: Fail 1: normal

10.1.6 Offset 0x05: System Reset-1 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	BMC12_9548_2_RST	R		1: It is placed in normal operation state. 0: It is placed in reset state.
6	BMC10_9548_1_RST	R		1: It is placed in normal operation state. 0: It is placed in reset state.
5	BMC9_9548_0_RST	R		1: It is placed in normal operation state. 0: It is placed in reset state.
4	CPLD_BMC_RST_N	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
3	CPLD_BMC_PHY_RST_N	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
2	CPLD_BCM5396_RESETB_N	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
1	CPLD_MAC_PCIE_PERST_L	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.

0	CPLD_MAC_RESET_N	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.

Note: This register will return back to H after set to L automatically

10.1.7 Offset 0x06 System Reset-2: (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	CPLD_TPM_I2C_RST_N	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
6	CPLD_CLKGEN_RST	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
5	CPLD_CP2112_I2C_9548_RST	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
4	CPLD_USB2112A_BRDG_RST	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
3	CPLD_SMB_PHY_RST_N	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
2	CPLD_FPGA_FLASH_RST	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
1	BMC_EXTRST	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
0	BMC_SCM_LPC_RST_N	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.

Note: This register will return back to H after set to L automatically

10.1.8 Offset 0x07: System Reset-3 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	BMC_PIM1_9548_RST_N	R		1: It is placed in normal operation state.

				0: It is placed in reset state.
6	BMC_PIM2_9548_RST_N	R		1: It is placed in normal operation state. 0: It is placed in reset state.
5	BMC_PIM3_9548_RST_N	R		1: It is placed in normal operation state. 0: It is placed in reset state.
4	BMC_PIM4_9548_RST_N	R		1: It is placed in normal operation state. 0: It is placed in reset state.
3	BMC_PIM5_9548_RST_N	R		1: It is placed in normal operation state. 0: It is placed in reset state.
2	BMC_PIM6_9548_RST_N	R		1: It is placed in normal operation state. 0: It is placed in reset state.
1	BMC_PIM7_9548_RST_N	R		1: It is placed in normal operation state. 0: It is placed in reset state.
0	BMC_PIM8_9548_RST_N	R		1: It is placed in normal operation state. 0: It is placed in reset state.

10.1.9 Offset 0x08: System Reset-4 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	PSU_PDB9548_L_RST	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
6	PSU_PDB9548_R_RST	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
5	BMC_SPI_1_RST	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
4	BMC_SPI_2_RST	R/W	1	1: It is placed in normal operation state.

				0: It is placed in reset state.
3	SMB_CPLD_FCM_9548_RST_B	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
2	SMB_CPLD_FCM_9548_RST_T	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
1	SMB_CPLD_FCM_CPLD_RST_B	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
0	SMB_CPLD_FCM_CPLD_RST_T	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.

Note: This register will return back to H after set to L automatically

10.1.10 Offset 0x09: System Reset-5 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	CPLD_PIM_HW_RST_8	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
6	CPLD_PIM_HW_RST_7	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
5	CPLD_PIM_HW_RST_6	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
4	CPLD_PIM_HW_RST_5	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
3	CPLD_PIM_HW_RST_4	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
2	CPLD_PIM_HW_RST_3	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.

1	CPLD_PIM_HW_RST_2	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
0	CPLD_PIM_HW_RST_1	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.

Note: This register will return back to H after set to L automatically

10.1.11 Offset 0x0A: System Reset-6 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	CPLD_PIM8_9548_RST_N	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
6	CPLD_PIM7_9548_RST_N	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
5	CPLD_PIM6_9548_RST_N	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
4	CPLD_PIM5_9548_RST_N	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
3	CPLD_PIM4_9548_RST_N	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
2	CPLD_PIM3_9548_RST_N	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
1	CPLD_PIM2_9548_RST_N	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
0	CPLD_PIM1_9548_RST_N	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.

Note: This register will return back to H after set to L automatically

10.1.12 Offset 0x0B: System Reset-7 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:6	Reserve	NA	NA	NA
5	MAC_QSPI_RST	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
4	CPLD_RST_FPGA	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
3	CPLD_USBHUB_RST_N	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
2	CPLD_9548_2_RST	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
1	CPLD_9548_1_RST	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.
0	CPLD_9548_0_RST	R/W	1	1: It is placed in normal operation state. 0: It is placed in reset state.

Note: This register will return back to H after set to L automatically

10.1.13 Offset 0x0C: System Reset-8 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:2	Reserve	NA	NA	
1	SCM_RESET_CPLD_2	R	1	1: It is placed in normal operation state. 0: It is placed in reset state.
0	SCM_RESET_CPLD_1	R	1	1: It is placed in normal operation state. 0: It is placed in reset state.

10.1.14 Offset 0x0D: System Reset Lock / Unlock (Read & Write)(Reserved)

Bit	Name	R/W	Reset Value	Description

7:1	Reserve	NA	NA	
0	Reserve	R/W	0	1: Lock system reset signal to be high. 0: System reset signal to be normal.

10.1.15 Offset 0x10: Interrupt Status-1 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	PIM_FPGA_CPLD_8_INT	R	1	1:No interrupt 0: Interrupt
6	PIM_FPGA_CPLD_7_INT	R	1	1:No interrupt 0: Interrupt
5	PIM_FPGA_CPLD_6_INT	R	1	1:No interrupt 0: Interrupt
4	PIM_FPGA_CPLD_5_INT	R	1	1:No interrupt 0: Interrupt
3	PIM_FPGA_CPLD_4_INT	R	1	1:No interrupt 0: Interrupt
2	PIM_FPGA_CPLD_3_INT	R	1	1:No interrupt 0: Interrupt
1	PIM_FPGA_CPLD_2_INT	R	1	1:No interrupt 0: Interrupt
0	PIM_FPGA_CPLD_1_INT	R	1	1:No interrupt 0: Interrupt

10.1.16 Offset 0x11: Interrupt Status-2 (Read Only)

Bit	Name	R/W	Reset Value	Description

7	FCM_SMB_CPLD_FAN_ALT_T	R	1	1:No interrupt 0: Interrupt
6	FCM_SMB_CPLD_FAN_ALT_B	R	1	1:No interrupt 0: Interrupt
5	PDB_R_TEMP_ALERT	R	1	1:No interrupt 0: Interrupt
4	PDB_L_TEMP_ALERT	R	1	1:No interrupt 0: Interrupt
3	TEMP_SENSOR_CPLD_ALERT4	R	1	1:No interrupt 0: Interrupt
2	TEMP_SENSOR_CPLD_ALERT3	R	1	1:No interrupt 0: Interrupt
1	TEMP_SENSOR_CPLD_ALERT2	R	1	1:No interrupt 0: Interrupt
0	TEMP_SENSOR_CPLD_ALERT1	R	1	1:No interrupt 0: Interrupt

10.1.17 Offset 0x12: Interrupt Status-3 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	Reserve	NA	NA	NA
6	MAC_CPLD_PCIE_WAKE_L	R	1	1:No interrupt 0: Interrupt
5	TPM_CPLD_I2C_DAINT_N	R	1	1:No interrupt 0: Interrupt
4	MAC_CPLD_PCIE_INTR_L	R	1	1:No interrupt 0: Interrupt

3	VDD_CORE_FAULT_L	R	1	1:No interrupt 0: Interrupt
2	SCM_TPM_PP	R	1	1:No interrupt 0: Interrupt
1	SCM_M2_ALERT	R	1	1:No interrupt 0: Interrupt
0	SCM_ALERT	R	1	1:No interrupt 0: Interrupt

10.1.18 Offset 0x13: Interrupt Status-4 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:2	Reserve	NA	NA	NA
1	CPLD_INT_BMC	R	1	1:No interrupt 0: Interrupt
0	PCA9555_INT	R	1	1:No interrupt 0: Interrupt

10.1.19 Offset 0x20: Interrupt Mask-1 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	PIM_FPGA_CPLD_8_INT_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
6	PIM_FPGA_CPLD_7_INT_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
5	PIM_FPGA_CPLD_6_INT_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

4	PIM_FPGA_CPLD_5_INT_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	PIM_FPGA_CPLD_4_INT_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	PIM_FPGA_CPLD_3_INT_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	PIM_FPGA_CPLD_2_INT_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	PIM_FPGA_CPLD_1_INT_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

10.1.20 Offset 0x21: Interrupt Mask-2 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	FCM_SMB_CPLD_FAN_ALT_T_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
6	FCM_SMB_CPLD_FAN_ALT_B_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
5	PDB_R_TEMP_ALERT_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
4	PDB_L_TEMP_ALERT_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	TEMP_SENSOR_CPLD_ALERT4_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	TEMP_SENSOR_CPLD_ALERT3_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	TEMP_SENSOR_CPLD_ALERT2_MASK	R/W	0	1: CPLD blocks incoming the interrupt

				0: CPLD passes the interrupt to CPU
0	TEMP_SENSOR_CPLD_ALERT1_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

10.1.21 Offset 0x22: Interrupt Mask-3 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	Reserve	R/W	0	Reserve
6	MAC_CPLD_PCIE_WAKE_L_MASK		0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
5	TPM_CPLD_I2C_DAINT_N_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
4	MAC_CPLD_PCIE_INTR_L_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	VDD_CORE_FAULT_L_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	SCM_TPM_PP_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	SCM_M2_ALERT_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	SCM_ALERT_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

10.1.22 Offset 0x23: Interrupt Mask-4 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:2	Reserve	NA	NA	NA
1	CPLD_INT_BMC_MASK	R/W	0	1: CPLD blocks incoming the interrupt

				0: CPLD passes the interrupt to CPU
0	PCA9555_INT_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

10.1.23 Offset 0x30: PIM FPGA Present Interrupt Status (Read Only)

Bit	Name	R/W	Reset Value	Description
7	PIM_FPGA_CPLD_8_PRSNT_N	Rclr	1	1:No interrupt 0: Interrupt
6	PIM_FPGA_CPLD_7_PRSNT_N	Rclr	1	1:No interrupt 0: Interrupt
5	PIM_FPGA_CPLD_6_PRSNT_N	Rclr	1	1:No interrupt 0: Interrupt
4	PIM_FPGA_CPLD_5_PRSNT_N	Rclr	1	1:No interrupt 0: Interrupt
3	PIM_FPGA_CPLD_4_PRSNT_N	Rclr	1	1:No interrupt 0: Interrupt
2	PIM_FPGA_CPLD_3_PRSNT_N	Rclr	1	1:No interrupt 0: Interrupt
1	PIM_FPGA_CPLD_2_PRSNT_N	Rclr	1	1:No interrupt 0: Interrupt
0	PIM_FPGA_CPLD_1_PRSNT_N	Rclr	1	1:No interrupt 0: Interrupt

Note: This register will return to H automatically after read

10.1.24 Offset 0x31: PIM FPGA Present Interrupt Mask (Read& Write)

Bit	Name	R/W	Reset Value	Description

7	PIM_FPGA_CPLD_8_PRSNT_N	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
6	PIM_FPGA_CPLD_7_PRSNT_N	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
5	PIM_FPGA_CPLD_6_PRSNT_N	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
4	PIM_FPGA_CPLD_5_PRSNT_N	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	PIM_FPGA_CPLD_4_PRSNT_N	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	PIM_FPGA_CPLD_3_PRSNT_N	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	PIM_FPGA_CPLD_2_PRSNT_N	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	PIM_FPGA_CPLD_1_PRSNT_N	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

10.1.25 Offset 0x32: PIM FPGA Present Status (Read Only)

Bit	Name	R/W	Reset Value	Description
7	PIM_FPGA_CPLD_8_PRSNT_N	R	1	1:No PIM_FPGA 0: PIM_FPGA had plugged
6	PIM_FPGA_CPLD_7_PRSNT_N	R	1	1:No PIM_FPGA 0: PIM_FPGA had plugged
5	PIM_FPGA_CPLD_6_PRSNT_N	R	1	1:No PIM_FPGA 0: PIM_FPGA had plugged
4	PIM_FPGA_CPLD_5_PRSNT_N	R	1	1:No PIM_FPGA

				0: PIM_FPGA had plugged
3	PIM_FPGA_CPLD_4_PRSNT_N	R	1	1:No PIM_FPGA 0: PIM_FPGA had plugged
2	PIM_FPGA_CPLD_3_PRSNT_N	R	1	1:No PIM_FPGA 0: PIM_FPGA had plugged
1	PIM_FPGA_CPLD_2_PRSNT_N	R	1	1:No PIM_FPGA 0: PIM_FPGA had plugged
0	PIM_FPGA_CPLD_1_PRSNT_N	R	1	1:No PIM_FPGA 0: PIM_FPGA had plugged

10.1.26 Offset 0x33: SCM and FCM Present Interrupt Status (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	Reserve	NA	NA	NA
2	SCM_PRSNT_N	Rclr	1	1:No interrupt 0: Interrupt
1	FCM_SMB_CPLD_PRESENT_B	Rclr	1	1:No interrupt 0: Interrupt
0	FCM_SMB_CPLD_PRESENT_T	Rclr	1	1:No interrupt 0: Interrupt

Note: This register will return to H automatically after read

10.1.27 Offset 0x34: SCM and FCM Present Interrupt Mask (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:3	Reserve			
2	SCM_PRSNT_N	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

1	FCM_SMB_CPLD_PRESENT_B	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	FCM_SMB_CPLD_PRESENT_T	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

10.1.28 Offset 0x35: SCM and FCM Present Status (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	Reserve	NA	NA	NA
2	SCM_PRSNT_N	R	1	1:No SCM 0: SMB had plugged
1	FCM_SMB_CPLD_PRESENT_B	R	1	1:No SMB 0: SMB had plugged
0	FCM_SMB_CPLD_PRESENT_T	R	1	1:No SMB 0: SMB had plugged

10.1.29 Offset 0x40: System BMC (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	Reserve	NA		
6	CPLD_BMC_SPI_1_WP_N	R/W		
5	CPLD_BMC_PHY_WP	R/W		
4	CPLD_BMC_PHY_LOWPWR	R/W		
3	CPLD_SMB_PHY_WP	R/W		
2	CPLD_SMB_PHY_LOWPWR	R/W		
1	MAC_CPLD_PCIE_WAKE_L	R		
0	BMC_CPLD_HEARTBEAT_N	R		

10.1.30 Offset 0x41: System MISC-1 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	CPLD_USBHUB_OCS_N3	R/W	1	
6	CPLD_USBHUB_OCS_N1	R/W	1	
5	USBHUB_EN3	R		
4	USBHUB_EN1	R		
3	CPLD_SPI_SEC_BOOT_WP_N	R/W	0	
2	CPLD_MAC_WP	R/W	0	
1	CPLD_BRDID_EE_WP	R/W	0	
0	CPLD_CP211_EE_WP	R/W	0	

10.1.31 Offset 0x42: System MISC-2 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserve	NA		
5	LC4064_SYSCPLD	R		
4	SMB_CPLD_FCM_T_CPLD_SEL	R/W	1	
3	SMB_CPLD_FCM_B_CPLD_SEL	R/W	0	
2	SMB_CPLD_UART1_SEL	R/W	0	
1	CPLD_FGPA_PRG	R/W	1	
0	CPLD_IN_P1220	R/W	1	1: Turn ON TMIII 0: Turn OFF TMIII

10.1.32 Offset 0x43: System Power (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	Reserve	NA		

10.1.33 Offset 0x44: System Power (Read & Only)

Bit	Name	R/W	Reset Value	Description

7:2	Reserve	NA		
1	TH3_PWR_OK	R		
0	BMC_PWR_OK	R		

10.1.34 Offset 0x45: System PCA9543 Power (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	CPLD_PIM8_PCA9543_PWR	R/W	0	
6	CPLD_PIM7_PCA9543_PWR	R/W	0	
5	CPLD_PIM6_PCA9543_PWR	R/W	0	
4	CPLD_PIM5_PCA9543_PWR	R/W	0	
3	CPLD_PIM4_PCA9543_PWR	R/W	0	
2	CPLD_PIM3_PCA9543_PWR	R/W	0	
1	CPLD_PIM2_PCA9543_PWR	R/W	0	
0	CPLD_PIM1_PCA9543_PWR	R/W	0	

10.1.35 Offset 0x46: System MAC ROV (Read Only)

Bit	Name	R/W	Reset Value	Description
7	MAC_CPLD_ROV7	R		
6	MAC_CPLD_ROV6	R		
5	MAC_CPLD_ROV5	R		
4	MAC_CPLD_ROV4	R		
3	MAC_CPLD_ROV3	R		
2	MAC_CPLD_ROV2	R		
1	MAC_CPLD_ROV1	R		
0	MAC_CPLD_ROV0	R		

10.1.36 Offset 0x47: System CP2112A GPIO (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	Reserve	NA		
6	CP2112A_CPLD_GPIO6	R/W	0	
5	CP2112A_CPLD_GPIO5	R/W	0	
4	CP2112A_CPLD_GPIO4	R/W	0	
3	CP2112A_CPLD_GPIO3	R/W	0	
2	CP2112A_CPLD_GPIO2	R/W	0	
1	CP2112A_CPLD_GPIO1	R/W	0	
0	CP2112A_CPLD_GPIO0	R/W	0	

10.1.37 Offset 0x48: System SPI MUX-1 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	Reserve	NA		Reserve
6	SPI_2_B3	R/W	0	
5	SPI_2_B2	R/W	0	
4	SPI_2_B1	R/W	0	
3	SPI_2_B0	R/W	0	
2	SPI_1_B2	R/W	0	
1	SPI_1_B1	R/W	0	
0	SPI_1_B0	R/W	0	

10.1.38 Offset 0x49: System SPI MUX-2 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	Reserve	NA		Reserve
2	CPLD_BCM5396_MUX_SEL	R/W	0	
1	FPGA_SPI_MUX_SEL	R/W	0	

0	TH3_SPI_MUX_SEL	R/W	0	

10.1.39 Offset 0x4A: System Reserve-1 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	Reserve	NA		
4	BMC_CPLD_GPIO_SPARE5	R		
3	BMC_CPLD_GPIO_SPARE4	R		
2	BMC_CPLD_GPIO_SPARE3	R		
1	BMC_CPLD_GPIO_SPARE2	R		
0	BMC_CPLD_GPIO_SPARE1	R		

10.1.40 Offset 0x4B: System Misc-3 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	Reserve	NA		
6	CPLD_Reserved_4	NA		Reverse
5	CPLD_Reserved_3	R		
4	CPLD_Reserved_2	R		
3	CPLD_INT_BMC	R		
2	BMC_RST_FPGA	R		
1	LC4064_SYSCPLD	R		
0	PCA9555_INT	R		

10.2 SCM CPLD Register Descriptions

10.2.1 Offset 0x00: Board Info (Read Only)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved	NA	NA	
3:0	PCB_Version	RO	000	000: R0A 001: R0B

				010: R0C 011: R01 100: R02 101: R03 110: PVT1 110: PVT2 Others: Reserved

10.2.2 Offset 0x01: CPLD Version (Read Only)

Bit	Name	R/W	Reset Value	Description
7	Reserved	RO	0	
6	RELEASE_STA	RO	0	Released Bit 0= not released, 1= Released version after PVT
5:0	CPLD_VER	RO	0	CPLD Revision[5:0]

10.2.3 Offset 0x02: CPLD Sub Version (Read Only)

Bit	Name	R/W	Default Value	Description
7:0	CPLD_Sub_Version	RO		used for HW debug only

10.2.4 Offset 0x08: LED_TEST (Read & Write)

Bit	Name	R/W	Default Value	Description
7:5	Reserved		Reserved	
4	LED_TEST_EN	R/W	1	LED Control 0:LED controlled by Bit[3:0] 1:LED controlled by HW Logic – 7 color
3	LED_BLINK	R/W	0	LED_BLINK_EN 0: LED No blink 1: LED Blink is ON
2	SYS_BLUE	R/W	1	LED_BLUE 0: LED BLUE is ON 1: LED NLUE is OFF
1	SYS_GREEN	R/W	1	LED_GREEN 0: LED GREEN is ON 1: LED GREEN is OFF
0	SYS_RED	R/W	1	LED_RED 0: LED RED is ON 1: LED RED is OFF

10.2.5 Offset 0x09: SYSTEM_LED (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	RJ45_mode_SEL	R/W	1	LED_GREEN 0: Control by SW register 0x09[1:0] 1: Control by OOB_LED
6:4	Reserved	R/W	0	Reserved
3	SFP_LED3_P	R/W	0	LED_GREEN 0: LED GREEN is OFF 1: LED GREEN is ON
2	SFP_LED3_N	R/W	0	LED_ORANGE 0: LED ORANGE is OFF 1: LED ORANGE is ON
1	RJ45_LED2	R/W	0	LED_ORANGE 1: LED ORANGE is ON 0: LED ORANGE is OFF
0	RJ45_LED1	R/W	0	LED_GREEN 1: LED GREEN is ON 0: LED GREEN is OFF

10.2.6 Offset 0x0A: SYSTEM_LED (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	Reserved		0	Reserved
2	OOB_LED3_N	RO		
1	OOB_LED2_N	RO		
0	OOB_LED1_N	RO		

10.2.7 Offset 0x0C: Watch Dog (Read Only)

Bit	Name	R/W	Default Value	Description
7:1	Reserved	NA	NA	
0	ISO_COM_BRG_WDT	RO		

10.2.8 Offset 0x10: COMe_RST_CTRL (Read & Write)

Bit	Name	R/W	Default Value	Description
7:6	Reserved	NA	NA	
5	COM_PWR_BTN_N	R/W	1	0: write 0 to trigger reset 1: normal
4	COM_PWROK	R/W	1	0: write 0 to trigger reset 1: normal
3	PERST_N	R/W	1	0: write 0 to trigger M.2 reset

				1: normal
2	I2C_MUX_RST_1_N	R/W	1	0: write 0 to trigger PCA9548 reset 1: normal
1	CPLD_COM_PHY_RST_N	R/W	1	0: write 0 to trigger BCM54616S reset 1: normal
0	ISO_COM_RST_N	R/W	1	0: write 0 to trigger COMe reset 1: normal

10.2.9 Offset 0x11: COMe_STA (Read Only)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved		0	Reserved
3	ISO_COM_SUS_STAT_N	RO		COMe Module SUS_STAT_N Status
2	ISO_COM_SUS_S5_N	RO		COMe Module SUS_S5_N Status
1	ISO_COM_SUS_S4_N	RO		COMe Module SUS_S4_N Status
0	ISO_COM_SUS_S3_N	RO		COMe Module SUS_S3_N Status

10.2.10 Offset 0x12: COMe_BIOS_DIS_CTRL (Read & Write)

Bit	Name	R/W	Default Value	Description
7:2	Reserved	R/W		Reserved
1	ISO_BUFF_BRG_COM_BIOS_DIS1_N	R/W	0	Control COMe BIOS DIS1
0	ISO_BUFF_BRG_COM_BIOS_DIS0_N	R/W	0	Control COMe BIOS DIS0

10.2.11 Offset 0x14: COME_PWR_CTRL_REG (Read & Write)

Bit	Name	R/W	Default Value	Description
7:3	Reserved.		0	Reserved.
2	come_pwr_ctrl_reg[2] (com_exp_pwr_cycle)	R/W	1	PWR_CYC _N Write 0 to this bit will trigger CPLD power cycling the COMe Module, This bit will auto set to 1 after Power Cycle finish.
1	Reserved.		1	
0	come_pwr_ctrl_reg[0] (com_exp_pwr_enable)	R/W	0	PWR_COME_EN 0: COMe power is OFF 1: COMepower is ON

10.2.12 Offset 0x15: SPI_FLASH_SEL_CTRL (Read & Write)

Bit	Name	R/W	Default Value	Description
7:2	Reserved.		0	Reserved.
1	COM_SPI_OE_N	R/W	0	0:Enable 1:Disbale

0	COM_SPI_SEL	R/W	0	0:SPI Flash Accessed by COM-e. 1:SPI Flash Accessed by BMC.

10.2.13 Offset 0x21: SYSTEM_INTERRUPT (Read Only)

Bit	Name	R/W	Reset Value	Description
7	Reserved			Reserved
6	HOTSWAP_PG	RO		The Status of HOTSWAP_PG
5	DS100_INT_N	RO		1:No interrupt 0: Interrupt
4	HS_ALERT2	RO		1:No interrupt (Reserved) 0: Interrupt
3	HS_ALERT1	RO		1:No interrupt 0: Interrupt
2	HS_FAULT_N	RO		1:No interrupt 0: Interrupt
1	HS_TIMER	RO		1:No interrupt (Reserved) 0: Interrupt
0	PCIE_WAKE	RO		1:No interrupt 0: Interrupt

10.2.14 Offset 0x28: SYSTEM_INTERRUPT_MASK (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	Reserved			Reserved
6	HOTSWAP_PG_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
5	DS100_INT_N_MASK	R/W	1	1: CPLD blocks incoming the interrupt (Reserved) 0: CPLD passes the interrupt to CPU
4	HS_ALERT2_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	HS_ALERT1_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	HS_FAULT_N_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	HS_TIMER_MASK	R/W	1	1: CPLD blocks incoming the interrupt (Reserved) 0: CPLD passes the interrupt to CPU
0	PCIE_WAKE_MASK	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

10.2.15 Offset 0x30: SYSTEM_POWER_STATUS (Read Only)

Bit	Name	R/W	Reset Value	Description
7:5	Reserved			Reserved
4	PWRGD_PCH_PWROK	RO		1: Normal 0: Fail
3	A_3_3V_STBY_PG	RO		1: Normal

				0: Fail
2	C3_3V_STBY_PG	RO		1: Normal 0: Fail
1	C1P2_PG	RO		1: Normal 0: Fail
0	C1P0_PG	RO		1: Normal 0: Fail

10.2.16 Offset 0x31: SYSTEM_POWER_ENABLE (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	Reserved	R/W	1	Reserved
6	A_PWR_STBY_EN	R/W	1	1: Enable 0: disable
5	Reserved			Reserved
4	C12V_USERVER_EN	R/W	1	1: Enable 0: disable
3	C5V_PWR_STBY_EN	R/W	1	1: Enable 0: disable
2	VDD_1V8_EN	R/W	1	1: Enable 0: disable
1	C1P2_EN	R/W	1	1: Enable 0: disable
0	C1P0_EN	R/W	1	1: Enable 0: disable

10.2.17 Offset 0x32: SYSTEM_ISO_1 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	ISO_SPI_EN	R/W	0	0:Enable 1:Disbale
6	ISO_TPM_EN	R/W	0	0:Enable 1:Disbale
5	Reserved			Reserved
4	ISO_M2_EN	R/W	0	0:Enable 1:Disbale
3	ISO_UART_EN	R/W	0	0:Enable 1:Disbale
2	ISO_USBCDP	R/W	0	0:Enable 1:Disbale
1	ISO_USBHUB	R/W	0	0:Enable 1:Disbale
0	ISO_COM_I2C_EN	R/W	0	0:Enable 1:Disbale

Note: Default is L when ES

10.2.18 Offset 0x33: SYSTEM_ISO_2 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved	R/W		Reserved
5	ISO_DS100_EN	R/W	1	0:Enable 1:Disbale
4	ISO_TH3RP_EN	R/W	1	0:Enable 1:Disbale
3	ISO_FPGARP_EN	R/W	1	0:Enable 1:Disbale
2	ISO_BRG_THRM_N	R/W	1	Input from off-Module temp sensor indicating an over-temp situation.
1	Reserved			Reserved
0	ISO_PCIE_M2	R/W	0	0:Enable 1:Disbale

10.2.19 Offset 0x34: THERMAL2 (Read Only)

Bit	Name	R/W	Default Value	Description
7:1	Reserved	NA	NA	
0	ISO_BRG_THRMTRIP_N	RO		Indicating that the CPU has entered thermal shutdown.

10.2.20 Offset 0x35: SYSTEM_MISC_1 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	RTC_CLEAR	R/W	0	Control the state of RTC_CLEAR
6	DS100_EEPROM_WP	R/W	0	0: Normal 1: Write to the memory
5	DS80_EEPROM_WP	R/W	0	0: Normal 1: Write to the memory
4	A_DS80_EEPROM_WP	R/W	0	0: Normal 1: Write to the memory
3	USB_PWRON_N	R/W	1	0: Disbale 1: Enable
2	USB_DEBUG_EN	R/W	1	0: Disbale 1: Enable
1	I2C_BUS_EN	R/W	1	1: Enable 0: disable
0	Reserved			Reserved

10.2.21 Offset 0x36: SYSTEM_MISC_2 (Read & Write)

Bit	Name	R/W	Reset Value	Description

7:3	Reserved			
2	COMe_PWR_ON	RO	1	Reserved
1	SYS_EEPROM_WP	R/W	0	0:Enable 1:Disbale
0	G_BATLOW_N	R/W	0	0:Enable 1:Disbale

10.2.22 Offset 0x37: SYSTEM_MISC_3 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	CPLD_RESET_2	RO		
4	CPLD_RESET_1	RO		
3	DS100_SD_TH	RO		Controls LOS threshold setting
2	DS100_DONE_N	RO		0: External EEPROM load passed 1: External EEPROM load failed or incomplete
1	A_DS80_ALL_DONE_N	RO		0: External EEPROM load passed 1: External EEPROM load failed or incomplete
0	DS80_ALL_DONE_N	RO		0: External EEPROM load passed 1: External EEPROM load failed or incomplete

10.2.23 Offset 0x38: UART_SEL (Read Only)

Bit	Name	R/W	Default Value	Description
7:2	Reserved	NA	NA	
1	UART2_SEL	RO		0:Default mode 1:SOL mode
0	UART5_SEL	RO		0: Default mode 1: SOL mode

10.2.24 Offset 0x39: SYSTEM_MISC_4 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	RATE_S	RO		0: Reduced Bandwidth 1: Full Bandwidth
6	USB_PWRFLT_N	RO		Overcurrent
5	ISO_USB_FAULT	RO		USB over-current sense
4	I2C_USB_READY	RO		
3	I2C_BUS_READY	RO		
2	Reverse			
1	SCM_SEAT_N	RO		
0	HITLESS_EN	RO		

10.2.25 Offset 0x3A: SYSTEM_MISC_5 (Read Only)

Bit	Name	R/W	Reset Value	Description

7	SCM_PWR_BTN_N	RO		OCP debug card used
6	SCM_DEBUG_RST_BTN_N	RO	H	OCP debug card used When negative edge detect, The bit will flag
5	SCM_UART_SWITCH_N	RO	L	OCP debug card used When negative edge detect, The bit will flag
4	B_COM_TYPE2	RO		Module Type Descriptions
3	B_COM_TYPE1	RO		Module Type Descriptions
2	B_COM_TYPE0	RO		Module Type Descriptions
1	ISO_COM_GBE0_LINK1000_N	RO		Controller 0 1000 Mbit / sec link indicator
0	ISO_BRG_COM_GPO_0	RO		

10.2.26 Offset 0x3B: SYSTEM_MISC_6 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:2	Reserved			
1	clr_SCM_DEBUG_RST_BTN_N	R/W	1	0: Clear 0x3A Bit [6] data. 1: Normal
0	clr_SCM_UART_SWITCH_N	R/W	1	0: Clear 0x3A Bit [5] data. 1: Normal

10.2.27 Offset 0x3C: SYSTEM_MISC_7 (Read / Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
3	ISO_COM_THRM_EN	R/W	0	0: Enable 1: Disable
2	ISO_SWITCH_EN	R/W	0	0: Enable 1: Disable
1	ISO_COM_EARLY_EN	R/W	0	0: Enable 1: Disable
0	ISO_COM_WDT_EN	R/W	0	0: Enable 1: Disable

10.2.28 Offset 0x40: REPEATER_ENABLE (Read / Write)

Bit	Name	R/W	Default Value	Description
7:5	Reserved	NA	NA	
4	DS80_PRSNT	R/W	0	0: Enable 1:Disbale
3	A_DS80_PRSNT	R/W	0	0: Enable 1:Disbale
2	A_DS80_ENSMB	R/W	0	0: Disable

				1:Enable
1	DS80_ENSMB	R/W	0	0: Disable 1:Enable
0	DS100_ENSMB	R/W	0	0: Disable 1:Enable

10.2.29 Offset 0x41: SFP_STATUS (Read Only)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			Reserved
2	TX_FAULT	RO		Transmitter Fault Indication
1	TX_LOSS	RO		Loss of Signal
0	MOD_GN	RO		Indicate that the module is present

10.2.30 Offset 0x42: SFP_STATUS (Read / Write)

Bit	Name	R/W	Reset Value	Description
7:1	Reserved		0	Reserved
0	TX_DISABLE	R/W	1	

10.3 FCM CPLD Register Descriptions

10.3.1 Offset 0x00: BOARD_VERSION (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:4]	Version_ID[3:0]	R		000: R0A 001: R0B 100: R01 Others: Reserved
[3:0]	Board_ID[3:0]	R		00:ZZ 01: Reserved 10: Reserved 11: Reserved

10.3.2 Offset 0x01: CPLD Version (Read Only)

Bit	Name	R/W	Reset Value	Description
[7]	Reserved	R		Reserved
[6]	Released_Bit	R		0= not released 1= Released version after PVT
[5:0]	CPLD_Ver[5:0]	R		CPLD version

10.3.3 Offset 0x02: CPLD_SUB_VERSION (Read Only)

Bit	Name	R/W	Reset Value	Description

[7:0]	CPLD_SUB_VERSION	R		CPLD sub-version, used for HW debug only

10.3.4 Offset 0x06: FAN_BLOCK_VERSION (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:0]	FAN_BLOCK_VERSION	R		Fan block definition version.

10.3.5 Offset 0x07: TEMP_SENSOR (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved	N/A	N/A	
[1]	Temp sensor 2	R		
[0]	Temp sensor 1	R		

10.3.6 Offset 0x08: FAN_INT_TRIG_MOD (Read & Write)

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved			
[1:0]	FAN_INT_TRIG			00: FAN interrupt trigger by falling edge 01: FAN interrupt trigger by rising edge 10: FAN interrupt trigger by both falling edge and rising edge 11: FAN interrupt trigger by low level

10.3.7 Offset 0x09: FAN_INT_RPT (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:4]	Reserved	N/A	N/A	Reserved
[3]	FAN4_INT	R		FanTray-4 Interrupt 0: No interrupt 1: Fan4 interrupt is active
[2]	FAN3_INT	R		FanTray-3 Interrupt 0: No interrupt 1: Fan3 interrupt is active
[1]	FAN2_INT	R		FanTray-2 Interrupt 0: No interrupt 1: Fan2 interrupt is active
[0]	FAN1_INT	R		FanTray-1 Interrupt 0: No interrupt 1: Fan1 interrupt is active

10.3.8 Offset 0x0A: BMC_WDT_TRIGGER (Read & Write)

Bit	Name	R/W	Reset Value	Description
[7:1]	Reserved	RO		Reserved
[0]	BMC_WDT_TRIGGER	R/W		CMM BMC writes this bit to 1 to clear the count in CPLD. If CMM BMC didn't set this bit over 500S. The FANx_PWM register will set to default value. FAN will run with 50% RPM. This bit will always read back a 0 value.

10.3.9 Offset 0x0F: FCB_EEPROM_WP (Read & Write)

Bit	Name	R/W	Reset Value	Description
[7:1]	Reserved	N/A	N/A	Reserved
[0]	FCM_EEPROM_WP	R/W		FAN Control Board EERPOM Write Protect 1:Protect 0:Not protect

10.3.10 Offset 0x10: FAN_ENABLE_REG (Read & Write)

Bit	Name	R/W	Reset Value	Description
[7:4]	Reserved	N/A	N/A	Reserved
[3]	FAN4_ENABLE_REG	R/W	1	FAN4 Power Supply Enable 1: Enable the fan Power 0: Disable the fan power
[2]	FAN3_ENABLE_REG	R/W	1	FAN3 Power Supply Enable 1: Enable the fan Power 0: Disable the fan power
[1]	FAN2_ENABLE_REG	R/W	1	FAN2 Power Supply Enable 1: Enable the fan Power 0: Disable the fan power
[0]	FAN1_ENABLE_REG	R/W	1	FAN1 Power Supply Enable 1: Enable the fan Power 0: Disable the fan power

10.3.11 Offset 0x11: ADM1278 Alert Register (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:1]	Reserved	N/A	N/A	Reserved
[3]	HS_FAULT	R	1	1: no interrupt 0: interrupt happened
[2]	HS_ALERT2	R	1	1: no interrupt

				0: interrupt happened
[1]	HS_ALERT1	R	1	1: no interrupt 0: interrupt happened
[0]	HOTSWAP_PG	R	1	1: no interrupt 0: interrupt happened

10.3.12 Offset 0x12: ADM1278 Alert Register (Read & Write)

Bit	Name	R/W	Reset Value	Description
[7:1]	Reserved	N/A	N/A	Reserved
[3]	HS_FAULT_MASK	R/W	0	0: not mask 1: mask
[2]	HS_ALERT2_MASK	R/W	0	0: not mask 1: mask
[1]	HS_ALERT1_MASK	R/W	0	0: not mask 1: mask
[0]	HOTSWAP_PG_MASK	R/W	0	0: not mask 1: mask

10.3.13 Offset 0x11: ADM1278 Alert Register (Read Only)

Bit	Name	R/W	Reset Value	Description
[7]	PGB_FAN4	R	1	1: no interrupt 0: interrupt happened
[6]	PGB_FAN3	R	1	1: no interrupt 0: interrupt happened
[5]	PGB_FAN2	R	1	1: no interrupt 0: interrupt happened
[4]	PGB_FAN1	R	1	1: no interrupt 0: interrupt happened
[3]	FLTB_FAN4	R	1	1: no interrupt 0: interrupt happened
[2]	FLTB_FAN3	R	1	1: no interrupt 0: interrupt happened
[1]	FLTB_FAN2	R	1	1: no interrupt 0: interrupt happened
[0]	FLTB_FAN1	R	1	1: no interrupt 0: interrupt happened

10.3.14 Offset 0x12: ADM1278 Alert Register_MASK (Read & Write)

Bit	Name	R/W	Reset Value	Description
[7]	PGB_FAN4_MASK	R/W	0	1: no interrupt 0: interrupt happened
[6]	PGB_FAN3_MASK	R/W	0	1: no interrupt 0: interrupt happened
[5]	PGB_FAN2_MASK	R/W	0	1: no interrupt 0: interrupt happened
[4]	PGB_FAN1_MASK	R/W	0	1: no interrupt 0: interrupt happened
[3]	FLTB_FAN4_MASK	R/W	0	1: no interrupt 0: interrupt happened
[2]	FLTB_FAN3_MASK	R/W	0	1: no interrupt 0: interrupt happened
[1]	FLTB_FAN2_MASK	R/W	0	1: no interrupt 0: interrupt happened
[0]	FLTB_FAN1_MASK	R/W	0	1: no interrupt 0: interrupt happened

Note: Below register definition is the same for all Fans. Fan #1 control register range is 0x20-0x2F. Fan #2/3/4 register definition is same as Fan #1. Fan #2 register range is 0x30-0x3F. Fan #3 register range is 0x40-0x4F. Fan4 register range is 0x50-0x5F.

10.3.15 Offset 0x20: FAN1_TACH_F_N (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:0]	FAN1_TACH_F_N	RO		Fan1 Front Fan Speed

10.3.16 Offset 0x21: FAN1_TACH_B_N (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:0]	FAN1_TACH_B_N	RO		Fan1 Back Fan Speed

10.3.17 Offset 0x22: FAN1_PWM (Read & Write)

Bit	Name	R/W	Reset Value	Description
[7:]	Reserved	RO		Reserved
[6:0]	FAN1_PWM	R/W		FAN1_PWM[5:0] FanTray-1 PWM control signal Please refer to Table3 for the mapping to fan duty cycle.

10.3.18 Offset 0x24: FAN1_LED (Read & Write)

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved	R/W		Reserved
[1:0]	FAN1_LED	R/W		FAN1_LED_CTRL[1:0] 00: Under HW control 01: Red OFF, Blue ON 10: Red ON, Blue OFF 11: OFF If LED is under HW control Present_n=0, fan_alive_n=0, then Red OFF, Blue ON Present_n=1, fan_alive_n=x, then Red OFF, Blue OFF Present_n=0, fan_alive_n=1, then Red ON, Blue OFF

10.3.19 Offset 0x25: FAN1_EEPROM_WP (Read & Write)

Bit	Name	R/W	Reset Value	Description
[7:1]	Reserved	R/W		Reserved
[0]	FAN1_EEPROM_WP	R/W		FAN1 EERPOM Write Protect 1:Protect 0:Not protect

10.3.20 Offset 0x28: FAN1_PRESENT (Read Only)

Bit	Name	R/W	Reset Value	Description
[7:4]	Reserved	RO		Reserved
[3]	FFAN1_ALIVE	RO		Front Fan1 Alive Status 0: alive 1: bad
[2]	RFAN1_ALIVE	RO		Rear Fan1 Alive Status 0: alive 1: bad
[1]	FAN1_ALIVE	RO		Fan1 Alive Status 0: alive 1: bad
[0]	FAN1_PRESENT	RO		FanTray-1 Present 0: present 1: not present

10.3.21 Offset 0x29: FAN1_INT_MASK (Read & Write)

Bit	Name	R/W	Reset Value	Description
[7:4]	Reserved			Reserved
[3]	FFAN1_ALIVE_MASK	R/W	1	Front Fan1 Alive Status Interrupt Mask 0: not mask 1: mask
[2]	RFAN1_ALIVE_MASK	R/W	1	Rear Fan1 Alive Status Interrupt Mask 0: not mask 1: mask

[1]	FAN1_ALIVE_MASK	R/W	1	Fan1 Alive Status Interrupt Mask 0: not mask 1: mask
[0]	FAN1_PRE_MASK	R/W	1	FanTray-1 Present Interrupt Mask 0: not mask 1: mask

10.3.22 Offset 0x2A: FAN1_INT_STA (Read & Write)

Bit	Name	R/W	Reset Value	Description
[7:4]	Reserved	R/W		Reserved
[3]	FFAN1_ALIVE_STA	WC		Front Fan1 Alive Status Interrupt Status 0: not interrupt 1: interrupt happened (Base on Front Fan1 speed)
[2]	RFAN1_ALIVE_STA	WC		Rear Fan1 Alive Status Interrupt Status 0: not interrupt 1: interrupt happened (Base on Rear Fan1 speed)
[1]	FAN1_ALIVE_STA	WC		Fan1 Alive Status Interrupt Status 0: not interrupt 1: interrupt happened
[0]	FAN1_PRE_STA	WC		FanTray-1 Present Interrupt Status 0: not interrupt 1: interrupt happened

10.4 PDB CPLD Register Descriptions

10.4.1 Offset 0x00: Board Info (Read Only)

Bit	Name	R/W	Reset Value	Description
7	Reserve			NA
6:4	BRD_REV_ID[2:0]	R		
3:2	Reserved	NA		
1:0	PCB_Version[1:0]	R		00 for R0A 01 for R0B 10 for R0C 11 for R01

10.4.2 Offset 0x01: CPLD version (Read Only)

Bit	Name	R/W	Reset Value	Description
7	Reserved	R		
6	RELEASE_STA	R		Released Bit 0= not released, 1= Released version after PVT
5:0	CPLD_VER	R		CPLD Revision[5:0]

10.4.3 Offset 0x02: CPLD Sub Version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_Sub_Version	R		Used for HW debug only

10.4.4 Offset 0x10: SYSTEM_MISC_1 (Read & Write)

Bit	Name	R/W	Default Value	Description
7:2	Reserved		Reserved	
1	CPLD_PDB_L2_PSU_ON/ CPLD_PDB_R2_PSU_ON	R/W	1	0: L2/R2 PSU2 POWER OFF 1: L2/R2 PSU2 POWER ON
0	CPLD_PDB_L1_PSU_ON/ CPLD_PDB_R1_PSU_ON	R/W	1	0: L1/R1 PSU1 POWER OFF 1: L1/R1 PSU1 POWER ON

10.4.5 Offset 0x11: SYSTEM_MISC_2 (Read Only)

Bit	Name	R/W	Default Value	Description
7:4	Reserved		Reserved	
3	PSU_L2_PWR_OK / PSU_R2_PWR_OK	R	1	1: Normal 0:Fail
2	PSU_L1_PWR_OK / PSU_R1_PWR_OK	R	1	1: Normal 0:Fail
1	SMB_PSU_L_INPUT	R		
0	SMB_PSU_L_OUTPUT	R		

10.4.6 Offset 0x20: TIMER_BASE_SETTING (Read & Write)

Bit	Name	R/W	Default Value	Description
7:4	Reserved		Reserved	
3	TIMER_BASE_10s	R/W	0	Timer base 10s
2	TIMER_BASE_1s	R/W	0	Timer base 1s
1	TIMER_BASE_100ms	R/W	1	Timer base 100ms
0	TIMER_BASE_10ms	R/W	0	Timer base 10ms

10.4.7 Offset 0x21: TIMER_COUNTER_SETTING (Read & Write)

Bit	Name	R/W	Default Value	Description
7:0	TIMER_COUNTER_SETTING	R/W	0xFF	This timer is used for power up automatically, When counter down to zero, the power will re-power up. (Note: This value needs 0x23[1] to update)

10.4.8 Offset 0x22: TIMER_COUNTER_STATE (Read Only)

Bit	Name	R/W	Default Value	Description

7:0	TIMER_COUNTER_STATE	R		The counter state.

10.4.9 Offset 0x23: TIMER_MISC (Read & Write)

Bit	Name	R/W	Default Value	Description
7:2	Reserved		Reserved	
1	TIMER_COUNTER_SETTING_UPDATE	R/W	0	0: No Update 1: Update the 0x21 TIMER_COUNTER_SETTING
0	POWER_CYCLE_GO	R/W	0	0: No power cycle 1: Start the power cycle

10.5 IOB FPGA Register Definition

Following is a list of register types defined in this spec.

RO – read only.

RW – read and write.

W1C – write one to clear.

LOCK – special thread lock register.

10.5.1 PCI Configuration Space Registers

Following table defines PCI configuration space of the FPGA.

Offset	Bit	Type	Default	Definition
0x0	[31:16]	RO	0x0011	Device ID.
	[15:0]	RO	0x1d9b	Facebook Vendor ID.
0x04	[31:16]	RW		Status Register
	[15:0]	RW		Command register
0x08	[31:4]	RO	0x078000	Class Code – simple communication controllers, others.
	[3:0]	RO	0x01	Revision ID.
0x0C	[31:24]	RO	0	BIST
	[23:16]	RO	0	Header Type
	[15:8]	RO	0	Latency Timer
	[7:0]	RO	0	Cache Line Status
0x10	[31:0]	RW	0xFFF8,0000	BAR0, 512KB memory allocation.
0x14	[31:0]	RW	0	BAR1
0x18	[31:0]	RW	0	BAR2

0x1C	[31:0]	RW	0	BAR3
0x20	[31:0]	RW	0	BAR4
0x24	[31:0]	RW	0	BAR5
0x28			0	
0x2C	[31:16]	RO	0	Subsystem ID.
	[15:0]	RO	0	Subsystem Vendor ID.
0x30	[31:0]	RW	0	Expansion ROM Base Address
0x34	[31:4]	RO		Reserved
	[3:0]	RW		Capability Pointer.
0x38		RO		Reserved
0x3C	[31:24]	RO	0	Max Latency
	[23:16]	RO	0	Min Gnt.
	[15:8]	RO	0x01	Interrupt Pin.
	[7:0]	RO	0x00	Interrupt Line.

Following is the PCI device ID assigned by Facebook.

Device ID	Base Class	Sub-Class	Programming Interface	Device Name	Description
0x0011	0x07	0x80	0x00	IO Bridge	Class Code specifies this device belongs to "Communication Controllers, Others". Subsystem ID is 0.

10.5.2 PCI register mapping

FPGA PCI BAR0 requests 512KB of memory. PCIe configuration register BAR0 determines the base address of these registers. Following table defines the base address of each major function in the FPGA.

"direct" in "BMC Access" column means the corresponding function can be directly accessed through BMC over I2C 256B address. "indirect" in "BMC Access" column means the corresponding function can be indirectly accessed through some address/data/command registers at BMC I2C interface. Details can be found at "BMC Registers" section. ILA function is for HW debugging only. Please refer to DOM FPGA spec for reference of ILA function.

Base Address	End Address	Function	Block Size	Wishbone Slave	BMC Access
0x0,0000	0x0,003F	General Registers	64B	0.0	*Direct*

0x0,0040	0x0,007F	Secondary Registers	64B	0.1	*Direct*
0x0,0080	0x0,00BF	Reserved	64B	0.2	*Direct*
0x0,00C0	0x0,00FF	Reserved	64B	0.3	*Indirect*
0x0,0100	0x0,017F	Reserved	128B	0.4	*Indirect*
0x0,0180	0x0,01FF	Reserved(ila control)	128B	0.5	*Indirect*
0x0,0200	0x0,02FF	Reserved	256B	0.6	*Indirect*
0x0,0300	0x0,03FF	Reserved	256B	0.7	*Indirect*
0x0,0400	0x0,07FF	Reserved	1KB	0.8	*Indirect*
0x0,0800	0x0,0FFF	Reserved(ila memory)	2KB	0.9	*Indirect*
0x0,1000	0x0,13FF	Reserved	1KB	0.10	*Indirect*
0x0,1400	0x0,17FF	Reserved	1KB	0.11	*Indirect*
0x0,1800	0x0,1BFF	Reserved	1KB	0.12	*Indirect*
0x0,1C00	0x0,1FFF	Reserved	1KB	0.13	*Indirect*
0x0,2000	0x0,3FFF	Reserved	8KB	0.14	*Indirect*
0x0,4000	0x0,7FFF	Reserved	16KB	0.15	*Indirect*
0x0,8000	0x0,FFFF	Reserved	32K	1	*Indirect*
0x1,0000	0x1,7FFF	Reserved	32K	2	*Indirect*
0x1,8000	0x1,FFFF	Reserved	32K	3	*Indirect*
0x2,0000	0x2,7FFF	Reserved	32K	4	*Indirect*
0x2,8000	0x2,FFFF	Reserved	32K	5	*Indirect*
0x3,0000	0x3,7FFF	Reserved	32K	6	*Indirect*
0x3,8000	0x3,FFFF	Reserved	32K	7	*Indirect*
0x4,0000	0x4,7FFF	PIM#0	32K	8	*Indirect*
0x4,8000	0x4,FFFF	PIM#1	32K	9	*Indirect*
0x5,0000	0x5,7FFF	PIM#2	32K	10	*Indirect*
0x5,8000	0x5,FFFF	PIM#3	32K	11	*Indirect*
0x6,0000	0x6,7FFF	PIM#4	32K	12	*Indirect*
0x6,8000	0x6,FFFF	PIM#5	32K	13	*Indirect*
0x7,0000	0x7,7FFF	PIM#6	32K	14	*Indirect*
0x7,8000	0x7,FFFF	PIM#7	32K	15	*Indirect*

10.5.3 General Registers

10.5.3.1 Revision

Offset	Bit	Type	Default	Definition
0x0000	[31:24]	RO	0xa2	Device ID. 0xa2 – Minipack IOB FPGA ID.
	[23:8]	RO		FPGA revision register Bit[23:16] is major rev; bit[15:8] is minor rev.

	[7:0]	RO		Board ID Register. Data is from board strapping resistor. EVTA – 0x4 EVTB – 0x0 DVTA – 0x1 DVTB – 0x2 PVT – 0x3

10.5.3.2 Scratch_Pad

Offset	Bit	Type	Default	Definition
0x0004	[31:0]	RW	0x0000	Scratch pad. Software can write anything.

10.5.3.3 System_LED

Offset	Bit	Type	Default	Definition
0x000C	[31:0]	RW	0x0000	Reserved for Minipack

10.5.3.4 Up_Time

Offset	Bit	Type	Default	Definition
0x0014	[31:0]	RO	xx	FPGA up time counter. It increases by 1 every second after out of reset. On EVT-B and earlier units, this counter increases by 1 every 2 seconds.

10.5.3.5 MSI_Debug

Offset	Bit	Type	Default	Definition
0x0018	[31:8]	RW	0	MSI debug password.
	[7:0]	RW	0	MSI generation for debug purpose. When writing to 1, a corresponding MSI interrupt is generated if a correct password is input at bit[31:8].

10.5.3.6 Latency_Debug

Offset	Bit	Type	Default	Definition
0x001C	[31:16]	RO	0	Reserved
	[15:0]	RW	0	ACK delay configuration. Don't impact write operation to this register. 0 – Reading to latency_debug register will be ACKed ASAP; Other value – additional latency will be added to return latency_debug read ACK. For HW testing purpose.

10.5.3.7 Logic Reset

Offset	Bit	Type	Default	Definition
0x0020	[31:1]	RO	0	Reserved
	[0]	WO	0	Reset FPGA internal logic circuit without impact on PCIe;

10.5.3.8 Thread Control Register

Offset	Bit	Type	Default	Definition
0x0024	[31]	RO	0	Thread Lock. Please see Thread ID register for description.
	[30:24]	RO	0	Reserved
	[23:0]	LOCK	0	Thread ID. When Thread Lock bit is 0, software can write anything to Thread ID. Once Thread ID is successfully written, Thread Lock will be set to 1. When Thread Lock bit is 1, only writing the same value of Thread ID can clear both Thread ID and Thread Lock. No other write operation can take any effect.

10.5.3.9 Interrupt INTA Summary/MSI Interrupt Status

Offset	Bit	Type	Default	Definition
0x002C	[31:3]	RO	0	Reserved
	[2]	RO	0	PIM SLPC interrupt status
	[1]	RO	0	PIM FPGA interrupt status
	[0]	RO	0	PIM present status change interrupt status

10.5.4 IOB Specific Registers

10.5.4.1 PIM Status

Offset	Bit	Type	Default	Definition
0x0040	[31:24]	RO	0	Reserved
	[23:16]	RO	0	PIM Present Status. PIM present status is forced to enabled (0ohm to ground) on PIM card. 1 if the corresponding PIM is present; 0 if the corresponding PIM is not present.
	[15:8]	RO	0	PIM FPGA interrupt status. 1 indicates interrupt; 0 indicates no interrupt.

	[7:0]	W1C	0	PIM Present Status Change. 1 if the corresponding PIM presence status change has happened; 0 if the corresponding PIM presence status change has not happened;

10.5.4.2 PIM Present Interrupt Mask

Offset	Bit	Type	Default	Definition
0x0044	[31:8]	RO	All 1's	Reserved
	[15:8]	RW	0xFF	PIM interrupt mask. 1 PIM interrupt will not generate interrupt; 0 PIM interrupt will generate interrupt;
	[7:0]	RW	0xFF	PIM Present Status Change interrupt mask. 1 PIM Present Status Change will not generate interrupt; 0 PIM Present Status Change will generate interrupt;

10.5.4.3 SLPC Parity Enable

Offset	Bit	Type	Default	Definition
0x0048	[31:24]	RO	All 1's	Reserved
	[23:16]	RW	All 1's	SLPC interface error interrupt mask
	[15:8]	RO	All 1's	Reserved
	[7:0]	RW	0xFF	PIM SLPC parity generation enable. SLPC uses odd parity once enabled.

10.5.4.4 SLPC Parity Interrupt Status

Offset	Bit	Type	Default	Definition
0x004C	[31:8]	RO	All 0's	Reserved
	[7:0]	W1C	0	PIM SLPC interrupt error status. Once a bit is asserted, it is either a parity error or a timeout error has occurred on the particular SLPC interface.

10.5.4.5 SLPC Parity Error Count

Offset	Bit	Type	Default	Definition
0x0050	[31:16]	W1C	0	PIM#1 SLPC master received parity error
	[15:0]	W1C	0	PIM#0 SLPC master received parity error
0x0054	[31:0]	W1C	0	PIM#2&3 SLPC master received parity error
0x0058	[31:0]	W1C	0	PIM#4&5 SLPC master received parity error
0x005C	[31:0]	W1C	0	PIM#6&7 SLPC master received parity error

10.5.4.6 SLPC Timeout Error Count

Offset	Bit	Type	Default	Definition
0x0060	[31:16]	W1C	0	PIM#1 SLPC master received timeout
	[15:0]	W1C	0	PIM#0 SLPC master received timeout
0x0064	[31:0]	W1C	0	PIM#2&3 SLPC master received timeout
0x0068	[31:0]	W1C	0	PIM#4&5 SLPC master received timeout
0x006C	[31:0]	W1C	0	PIM#6&7 SLPC master received timeout

10.5.4.7 PCIE Debug Control

Offset	Bit	Type	Default	Definition
0x0080	[31:3]	RO	0	RESERVED
	[2]	RW	0	1 to disable BMC I2C access
	[1]	RW	0	1 to disable BMC I2C write
	[0]	RW	1	1 to enable PCIe debug register to capture malformed or unsupported TLP. 0 to allow PCIe debug register to capture normal TLP. For debugging purpose only.

10.5.4.8 PCIE Error Counter 0

Offset	Bit	Type	Default	Definition
0x0090	[31:0]	W1C	0	Unsupported TLP receive counter.

10.5.4.9 PCIE Error Counter 1

Offset	Bit	Type	Default	Definition
0x0094	[15:0]	W1C	0	Malformated TLP receive counter.

10.5.4.10 PCIE Access Counter

Offset	Bit	Type	Default	Definition
0x0098	[31:0]	W1C	0	Total TLP receive counter.

10.5.4.11 PCIE Debug TLP Registers

Offset	Bit	Type	Default	Definition
0x00A0	[31:0]	RO	0	TLP frame captured, 1st DW.
0x00A4	[31:0]	RO	0	TLP frame captured, 2nd DW.
0x00A8	[31:0]	RO	0	TLP frame captured, 3rd DW.

10.5.5 BMC Registers

Following is the registers on I2C slave interface. These registers are all 8bit.

The registers at address 0x0 -0xEF are directly shared between BMC and CPU. FPGA registers accessible by CPU are all 32bit in nature. Following is the mapping of I2C byte access to 32bit FPGA registers.

I2C Offset	FPGA Register bits
0	[31:24]
1	[23:16]
2	[15:8]
3	[7:0]

The registers at address 0XF0 and above defined in this section is dedicated for BMC only. CPU can't access 0XF0-0XFF registers in this section. BMC can use the address/data/command registers defined in address 0XF0- 0XFC to access FPGA full memory space. 0xFF is a debug register.

Reg Index	Type	Definition
0-0x3F	RW	FPGA general register direct access
0x40-0x7F	RW	FPGA QSFP IO register direct access
0x80-0xEF	RO	Reserved direct access to FPGA.
0xF0	RW	Indirect Access Address register [31:24]
0xF1	RW	Indirect Access Address register [23:16]
0xF2	RW	Indirect Access Address register [15:8]
0xF3	RW	Indirect Access Address register [7:0]
0xF4	RW	Indirect Access Write data register [31:24]
0xF5	RW	Indirect Access Write data [23:16]
0xF6	RW	Indirect Access Write data [15:8]
0xF7	RW	Indirect Access Write data [7:0]
0xF8	RO	Indirect Access Read data [31:24]
0xF9	RO	Indirect Access Read data [23:16]
0xFA	RO	Indirect Access Read data [15:8]
0xFB	RO	Indirect Access Read data [7:0]
0xFC	RW	Indirect Access Command Register. bit0 = 1 is for write; bit0 = 0 is for read. Writing to this register will trigger an indirect access.
0xFF	RO	Debug Register for HW only

		Bit7: MSI enable status Bit6: Data link layer link up status Bit5: PCIe entered POLL state Bit4: PCIe entered L0 state Bit[3:0]: LTSSM status. These 4bits are assigned to FPGA debug IO pins as shown belown. assign FPGA_RESERVED_1 = pcie_status_debug[0] ; assign FPGA_RESERVED_3 = pcie_status_debug[1] ; assign FPGA_RESERVED_4 = pcie_status_debug[2] ; assign FPGA_RESERVED_5 = pcie_status_debug[3] ;

10.6 DOM FPGA Register Definition

Following is a list of register types defined in this spec.

RO – read only.

RW – read and write.

W1C – write one to clear.

LOCK – special thread lock register.

10.6.1 SLPC register mapping

Eight PIM cards are seated in Minipack chassis. Each PIM has been allocated 32KB of memory. Following table shows the overall register mapping of eight PIM cards viewed by CPU.

Base Address	End Address	Function	Block Size	Wishbone Slave	BMC Access
0x0,0000	0x0,003F	General Registers	64B	0.0	*Direct*
0x0,0040	0x0,007F	Secondary Registers	64B	0.1	*Direct*
0x0,0080	0x0,00BF	*Reserved*	*64B*	0.2	*Direct*
0x0,00C0	0x0,00FF	*Reserved*	*64B*	0.3	*Indirect*
0x0,0100	0x0,017F	*Reserved*	128B	0.4	*Indirect*
0x0,0180	0x0,01FF	*Reserved(ila control)*	128B	0.5	*Indirect*
0x0,0200	0x0,02FF	*Reserved*	*256B*	0.6	*Indirect*

0x0,0300	*0x0,03FF*	*Reserved*	*256B*	0.7	*Indirect*
0x0,0400	0x0,07FF	*Reserved*	1KB	0.8	*Indirect*
0x0,0800	0x0,0FFF	*Reserved (ila memory)*	2KB	0.9	*Indirect*
0x0,1000	*0x0,13FF*	*Reserved*	*1KB*	0.10	*Indirect*
0x0,1400	*0x0,17FF*	*Reserved*	*1KB*	0.11	*Indirect*
0x0,1800	*0x0,1BFF*	*Reserved*	*1KB*	0.12	*Indirect*
0x0,1C00	*0x0,1FFF*	*Reserved*	*1KB*	0.13	*Indirect*
0x0,2000	*0x0,3FFF*	*Reserved*	*8KB*	0.14	*Indirect*
0x0,4000	*0x0,7FFF*	*Reserved*	*16KB*	0.15	*Indirect*
0x0,8000	*0x0,FFFF*	*Reserved*	*32K*	*1*	*Indirect*
0x1,0000	*0x1,7FFF*	*Reserved*	*32K*	*2*	*Indirect*
0x1,8000	*0x1,FFFF*	*Reserved*	*32K*	*3*	*Indirect*
0x2,0000	*0x2,7FFF*	*Reserved*	*32K*	*4*	*Indirect*
0x2,8000	*0x2,FFFF*	*Reserved*	*32K*	*5*	*Indirect*
0x3,0000	*0x3,7FFF*	*Reserved*	*32K*	*6*	*Indirect*
0x3,8000	*0x3,FFFF*	*Reserved*	*32K*	*7*	*Indirect*
0x4,0000	0x4,7FFF	PIM#0	32K	8	*Indirect*
0x4,8000	0x4,FFFF	PIM#1	32K	9	*Indirect*
0x5,0000	0x5,7FFF	PIM#2	32K	10	*Indirect*
0x5,8000	0x5,FFFF	PIM#3	32K	11	*Indirect*
0x6,0000	0x6,7FFF	PIM#4	32K	12	*Indirect*
0x6,8000	0x6,FFFF	PIM#5	32K	13	*Indirect*
0x7,0000	0x7,7FFF	PIM#6	32K	14	*Indirect*
0x7,8000	0x7,FFFF	PIM#7	32K	15	*Indirect*

Table 39 Global Memory Map

Following table defines the base address of each major function in each PIM/DOM FPGA.

Base Address	End Address	Function	Block Size	Wishbone Slave	BMC Access
0x0000	0x003F	General Registers	64B	0	Direct
0x0040	0x007F	QSFP Management Registers	64B	1	Direct
0x0080	0x00BF	DOM1_reg2	64B	2	Direct
0x00C0	*0x00FF*	*Reserved*	*64B*	*3*	*Indirect*
0x0100	0x017F	reserved	128B	4	Indirect
0x0180	0x01FF	Debug Registers	128B	5	Indirect
0x0200	0x02FF	MDIO	256B	6	Indirect
0x0300	*0x03FF*	*LED CONTROL*	*256B*	*7*	*Indirect*
0x0400	0x07FF	DOM and RTC Registers	1KB	8	Indirect
0x0800	0x0FFF	Debug Memory	2KB	9	Indirect
0x1000	*0x13FF*	*Reserved*	*1KB*	*10*	*Indirect*
0x1400	*0x17FF*	*Reserved*	*1KB*	*11*	*Indirect*
0x1800	*0x1BFF*	*Reserved*	*1KB*	*12*	*Indirect*
0x1C00	*0x1FFF*	*Reserved*	*1KB*	*13*	*Indirect*
0x2000	*0x3FFF*	*RTC data block*	*8KB*	*14*	*Indirect*
0x4000	0x41FF	DOM Data Block, Channel 0	512B	15	Indirect
0x4200	0x43FF	DOM Data Block, Channel 1	512B		
0x4400	0x45FF	DOM Data Block, Channel 2	512B		
0x4600	0x47FF	DOM Data Block, Channel 3	512B		
0x4800	0x49FF	DOM Data Block, Channel 4	512B		
0x4A00	0x4BFF	DOM Data Block, Channel 5	512B		
0x4C00	0x4DFF	DOM Data Block, Channel 6	512B		
0x4E00	0x4FFF	DOM Data Block, Channel 7	512B		
0x5000	0x51FF	DOM Data Block, Channel 8	512B		
0x5200	0x53FF	DOM Data Block, Channel 9	512B		
0x5400	0x55FF	DOM Data Block, Channel 10	512B		
0x5600	0x57FF	DOM Data Block, Channel 11	512B		
0x5800	0x59FF	DOM Data Block, Channel 12	512B		
0x5A00	0x5BFF	DOM Data Block, Channel 13	512B		
0x5C00	0x5DFF	DOM Data Block, Channel 14	512B		
0x5E00	0x5FFF	DOM Data Block, Channel 15	512B		
0x6000	*0x7FFF*	*Reserved*	*8KB*		

Table 40 DOM FPGA Memory Map

In the above tables, “direct” in “BMC Access” column means the corresponding function can be directly accessed through BMC over I2C 256B address. “indirect” in “BMC Access” column means the corresponding function can be indirectly accessed through some address/data/command registers at BMC I2C interface. Details can be found at “BMC Registers” section.

10.6.2 General Registers

General register section is a group of common register definition across multiple Facebook FPGA designs.

Please note that some of the registers in this document are defined to support max 32channles of QSFP ports for future designs. For Minipack DOM FPGA function, please ignore the bit definitions on the unused QSFP ports.

10.6.2.1 Revision

Offset	Bit	Type	Default	Definition
0x0000	[31:24]	RO	0xa2	Device ID. 0XA3 – Minipack DOM1 FPGA ID.
	[23:8]	RO		FPGA revision register Bit[23:16] is major rev; bit[15:8] is minor rev.
	[7:0]	RO		Board ID Register. Data is from board strapping resistor. 00000000 – PIM-16Q 00010000 – PIM-4DD 1111XXXX – PIM-16O

10.6.2.2 Scratch_Pad

Offset	Bit	Type	Default	Definition
0x0004	[31:0]	RW	0x0000	Scratch pad. Software can write anything.

10.6.2.3 System_LED

Offset	Bit	Type	Default	Definition
0x000C	[31:16]	RO	0x0000	reserved
	[15]	RW	0	LED color choice. 0 – amber 1 – blue
	[14]	RW	1	LED color mode 1 – bit 15 determines the color of the LED 0 – bit [11:0] determines the color of the LED.
	[13]	RW	0	LED flashing control when LED on/off =1. 1 – flashing enabled; 0 – normal operation.
	[12]	RW	1	LED on/off control. 1 – on; 0 – off. 00- OFF 01- ON 10- OFF 11- FLASH

	[11:8]	RW	0x0	Color B brightness control
	[7:4]	RW	0x2	Color G brightness control
	[3:0]	RW	0xF	Color R brightness control 0 : 0 % duty cycle 1: 1/15 duty cycle 2: 2 / 15 duty cycle …… E: 14/15 duty cycle F: 15/15 duty cycle

10.6.2.4 Up_Time

Offset	Bit	Type	Default	Definition
0x0014	[31:0]	RO	xx	FPGA up time counter. It increases by 1 every second after out of reset. On EVT-B and earlier units, this counter increases by 1 every 2 seconds.

10.6.2.5 MSI_Debug

Offset	Bit	Type	Default	Definition
0x0018	[31:8]	RW	0	PIM Interrupt debug password.
	[7:0]	RW	0	PIM Interrupt generation for debug purpose. When writing to 1, a corresponding MSI interrupt is generated if a correct password is input at bit[31:8].

10.6.2.6 Latency_Debug

Offset	Bit	Type	Default	Definition
0x001C	[31:16]	RO	0	Reserved
	[15:0]	RW	0	ACK delay configuration. Don't impact write operation to this register. 0 – Reading to latency_debug register will be ACKed ASAP; Other value – additional latency will be added to return latency_debug read ACK. For HW testing purpose.

10.6.2.7 Logic Reset

Offset	Bit	Type	Default	Definition
0x0020	[31:1]	RO	0	Reserved
	[0]	WO	0	Reset FPGA internal logic circuit . Auto clear to 0 after reset.

10.6.2.8 Thread Control Register

Offset	Bit	Type	Default	Definition
0x0024	[31]	RO	0	Thread Lock. Please see Thread ID register for description.
	[30:24]	RO	0	Reserved
	[23:0]	LOCK	0	Thread ID. When Thread Lock bit is 0, software can write anything to Thread ID. Once Thread ID is successfully written, Thread Lock will be set to 1. When Thread Lock bit is 1, only writing the same value of Thread ID can clear both Thread ID and Thread Lock. No other write operation can take any effect.

10.6.2.9 Interrupt INTA Summary/MSI Interrupt Status

Offset	Bit	Type	Default	Definition
0x002C	[31:7]	RO	0	Reserved
	[6]	RO	0	MDIO interrupt.
	[5]	RO	0	Power Interrupt.
	[4]	RO	0	Device interrupt. Please refer to device interrupt register for details.
	[3]	RO	0	QSFP RTC I2C interrupt
	[2]	RO	0	DOM engine interrupt status
	[1]	RO	0	QSFP transceiver interrupt status
	[0]	RO	0	QSFP present interrupt status

10.6.3 QSFP Management Registers

In this section, CN is used in the register definition table to represent the total channel number of this design supports. CN=16 for Minipack DOM.

10.6.3.1 QSFP GPIO

Offset	Bit	Type	Default	Definition
0x40	[31:17]	RO	0	Reserved.
	[16]	RW	0	GPIO control mode. 0 – This GPIO register controls GPIO signals; 1 – FPGA engine controls GPIO signals.
	[CN*2-1:0]	RW	0	GPIO signal control for MODSEL signals.

10.6.3.2 DOM MAX Temperature

Offset	Bit	Type	Default	Definition
0x044	[31:24]	RO		Max temperature sequence number
	[23:16]	RO	0	Max temperature QSFP location
	[15:0]	RO	0	Max temperature read out of the QSFPs

10.6.3.3 QSFP Present Register

Offset	Bit	Type	Default	Definition
0x0048	[31:CN]	RO	0	
	[CN-1:0]	RO	0	QSFP Present. 1 to indicate a QSFP is present.

10.6.3.4 QSFP Present Interrupt Register

Offset	Bit	Type	Default	Definition
0x0050	[31:CN]	RO	0	
	[CN-1:0]	W1C	All 1's	When a QSFP is inserted or removal, this signal will be asserted to 1. Write 1 clear. CN is the QSFP ports supported by this design.

10.6.3.5 QSFP Present Interrupt Mask Register

Offset	Bit	Type	Default	Definition
0x0058	[31:CN]	RO	All 1's	
	[CN-1:0]	RW	All '1s	1 to mask QSFP present interrupt. 0 to allow QSFP present interrupt.

10.6.3.6 QSFP Interrupt Register

Offset	Bit	Type	Default	Definition
0x0060	[31:CN]	RO	0	
	[CN-1:0]	RO	0	1 to indicate an interrupt is pending.

10.6.3.7 QSFP Interrupt Mask Register

Offset	Bit	Type	Default	Definition
0x0068	[31:CN]	RW	All 1's	
	[CN-1:0]	RW	All '1s	1 to mask QSFP interrupt. 0 to allow QSFP present interrupt.

10.6.3.8 QSFP Reset Register

Offset	Bit	Type	Default	Definition
0x0070	[31:CN]	RO	All 1's	

	[CN-1:0]	RW	All '1s	1 to hold QSFP reset active. 0 to release QSFP reset. This register is writeable when QSFP is present. It is set to 1's if the corresponding QSFP is not present.

10.6.3.9 QSFP LPmode Register

Offset	Bit	Type	Default	Definition
0x0078	[31:CN]	RO	All 1's	
	[CN-1:0]	RW	All '1s	1 to hold QSFP in low power mode. 0 to release QSFP from low power mode. This register is writeable when QSFP is present. It is set to 1's if the corresponding QSFP is not present.

10.6.4 DOM1 REG2

The registers in this section is for PIM DOM FPGA on Minipack.

10.6.4.1 SLPC Slave Parity

Offset	Bit	Type	Default	Definition
0x0080	[31:16]	W1C	0	SLPC slave received parity error counter.
	[15:1]	RO	0	Reserved.
	[0]	RW	1	SLPC slave parity enable. SLPC uses odd parity once enabled.

10.6.4.2 PHY FW Load Control/Status

Offset	Bit	Type	Default	Definition
0x0084	[31:8]	RO	0	Reserved.
	[7:4]	RO	X	PHY FW load status. 1- enable; 0- disable.
	[3:0]	RW	All 1's	PHY FW load enable control. 1- enable; 0- disable.

10.6.4.3 Device Interrupt Status

Offset	Bit	Type	Default	Definition
0x0088	[31:9]	RO	0	Reserved
	[8]	W1C	0	SLPC Parity Error Interrupt. 0 – normal; 1 – interrupt.
	[7:6]	RO	0	PCA9534 I2C IO expander interrupt [1:0] 0 – normal; 1 – interrupt.
	[5:4]	RO	0	Temperature sensor LM75 interrupt[1:0] 0 – normal; 1 – interrupt.
	[3:0]	RO	0	PHY[3:0] Interrupt. 0 – normal; 1 - interrupt

10.6.4.4 Device Interrupt Mask

Offset	Bit	Type	Default	Definition
0x008C	[31:9]	RO	All 1's	Reserved.
	[8:0]	RW	All 1's	Device interrupt mask 1 – to disable interrupt to the host if the corresponding device interrupt is asserted. 0 – to allow interrupt to the host if the corresponding device interrupt is asserted.

10.6.4.5 Device Power Bad Status

Offset	Bit	Type	Default	Definition
0x0090	[31]	RO	0	0-- Hotswap controller power good; 1 – power bad.
	[30]	RO	0	hotswap controller fault 0 -- normal; 1 – fault.
	[29:28]	RO	0	Hotswap controller alert[1:0] 0 – normal; if either bit is 1, an alert is asserted.
	[27]	RO	0	3.3V status 0 – normal; 1- 3.3V bad.
	[26]	R0	0	Reserved.
	[25]	RO	0	Power monitor MAX34461 fault 0 – normal; 1 – power monitor fault
	[24]	RO	0	Power monitor MAX34461 alert 0 – normal; 1 – power monitor alert
	[23:20]	RO	0	Reserved.
	[19:16]	RO	0	PHY[3:0] 1.0V analog voltage power good indicator. 0 – normal; 1 – alert
	[15:12]	RO	0	PHY[3:0] 0.8V VDDM power good indicator. 0 – normal; 1 – alert
	[11:8]	RO	0	PHY[3:0] 0.8V analog voltage power good indicator. 0 – normal; 1 – alert
	[7:4]	RO	0	PHY[3:0] 0.8V core voltage controller alert. 0 – normal; 1 - alert
	[3:0]	RO	0	PHY[3:0] 0.8V core voltage power good indicator. 0 – normal; 1 - alert

10.6.4.6 Device Power Good Mask

Offset	Bit	Type	Default	Definition
0x0094	[31:0]	RW	All 1's	1 – to disable interrupt to the host if the corresponding power good status goes bad.

				0 – to allow interrupt to the host if the corresponding power good status goes bad.

10.6.4.7 Device Power Control

Offset	Bit	Type	Default	Definition
0x0098	[31:28]	RW	All 1s	reserved
	[27]	RW	1	3.3V power control 1 1 – enable power; 0 – disable power
	[26]	RW	1	1.8V power control 1 – enable power; 0 – disable power
	[25]	RW	1	1.0V power control 1 – enable power; 0 – disable power
	[24]	RW	1	0.8V power control 1 – enable power; 0 – disable power
	[23:20]	RW	All 1s	1.8V power control 1 – enable power; 0 – disable power
	[19:16]	RW	All 1s	PHY[3:0] 1.0V analog voltage power control. 1 – enable power; 0 – disable power
	[15:12]	RW	All 1s	PHY[3:0] 0.8V VDDM power control. 1 – enable power; 0 – disable power
	[11:8]	RW	All 1s	PHY[3:0] 0.8V analog voltage power control. 1 – enable power; 0 – disable power
	[7:6]	RW	All 1s	reserved
	[5]	RW	1	3.3V CSD95372 power control 1 – enable power; 0 -disable power Reserved
	[4]	RW	1	0.8V CSD95372 power control 1 – enable power; 0 -disable power Reserved
	[3:0]	RW	All 1s	PHY[3:0] 0.8V core voltage power control. 1 – enable power; 0 – disable power

10.6.4.8 Device Reset Control

Offset	Bit	Type	Default	Definition
0x009C	[31:16]	RO	All 1s	Reserved
	[15:12]	RW	All 1s	Reserved
	[11:8]	RW	All 1s	OBO MRESETL control 1 – reset release; 0 – reset assert.
	[7]	RW	1	reserved

	[6]	RW	1	PCA9548 reset control 1 – reset release; 0 – reset assert.
	[5]	RW	1	MAX34461 reset control 1 – reset release; 0 – reset assert.
	[4]	RW	1	IDT N240 reset control 1 – reset release; 0 – reset assert.
	[3:0]	RW	All 1s	PHY Reset Control 1 – reset release; 0 – reset assert.

10.6.4.9 PIM Status

Offset	Bit	Type	Default	Definition
0x00A0	[31:1]	RO	0	Reserved
	[0]	RO	1	1 indicates that PIM is seated in chassis.

10.6.5 Logic Analyzer

There is a built-in logic analyzer inside FPGA for debugging or trouble shooting purpose. There are up to 32bits of signals can be monitored simultaneously. This feature is for HW debugging purpose only.

10.6.5.1 ILA Trigger Data Pattern and Mask 1

Offset	Bit	Type	Default	Definition
0x0180	[31:0]	RW	0	data pattern to be matched for triggering event 1.
0x0184	[31:0]	RW	all 1's	data mask to be matched for triggering event 1. If the unmasked data to be monitored matches the pattern, trigger capture state machine will advance.

10.6.5.2 ILA Trigger Data Pattern and Mask 2

Offset	Bit	Type	Default	Definition
0x0188	[31:0]	RW	0	data pattern to be matched for triggering event 2.
0x018C	[31:0]	RW	all 1's	data mask to be matched for triggering event 2. If the unmasked data to be monitored matches the pattern, trigger capture state machine will advance.

10.6.5.3 ILA Trigger Data Pattern and Mask 3

Offset	Bit	Type	Default	Definition
0x0190	[31:0]	RW	0	data pattern to be matched for triggering event 3.
0x0194	[31:0]	RW	all 1's	data mask to be matched for triggering event 3.

				If the unmasked data to be monitored matches the pattern, trigger capture state machine will advance.

10.6.5.4 ILA Trigger Data Pattern and Mask 4

Offset	Bit	Type	Default	Definition
0x0198	[31:0]	RW	0	data pattern to be matched for triggering event 4.
0x019C	[31:0]	RW	all 1's	data mask to be matched for triggering event 4. If the unmasked data to be monitored matches the pattern, trigger capture state machine will advance.

10.6.5.5 ILA Sieve Data Pattern

Offset	Bit	Type	Default	Definition
0x01A0	[31:0]	RW	0	When not all of 32bit data needs to be captured, we can use this sieve feature to extend sample counts. Bit of 0s will be selected to be stored in RAM; bit of 1s will be ignored. For example, if sieve pattern is 32'hFF00_F0F0, raw data bit[23:16, 11:8, 3:0] will be rearranged into pre-data[15:0] in this order. Then pre-data[15:0] is spread on to RAM data input bus [31:16],and [15:0], in this order, before being pushed into RAM. In this way, sample counts can be doubled.

10.6.5.6 ILA Command Register

Offset	Bit	Type	Default	Definition
0x01A4	[31:28]	RW	0	Triger State Machine Number. Specify how many trigger events are defined before trigger the scope capture.
	[27:26]	RW		Reserved
	[25]	RW	0	Active 1 to stop a capture.
	[24]	RW	0	Active 1 to start a capture. Auto clear to 0.
	[23:16]	RW	0	Capture Threshold. support threshold capture -- it can capture data before and after trigger event. threshold/256 portion of the FIFO will store sample data before trigger event. If no sieve function is enabled, an extra 1 DW data will be added before trigger event. Triggering point is optionally reported in status register.
	[15:8]	RW	0	Sample clock prescale. Sample rate = wb_clk_i freq/(prescale +1)
	[7:0]	RW	0xFF	IRQ interrupt

10.6.5.7 ILA Status Register

Offset	Bit	Type	Default	Definition
0x01A8	[31:16]	RO	0	Trigger Point – counts how many prime samples are captured before trigger event happens.
	[15:8]	RO	0	RESERVED.
	[7:4]	RO	0	ILA core state machine. 0 – idle; 1- prime; 2 – searching for trigger event; 4 – data capture; 8 – capture complete. Others – undefined.
	[3:2]	RO	0	RESERVED.
	[1]	RO	0	reserved.
	[0]	RO	0	1 -- ILA data RAM is full with captured data. Cleared once data RAM is read, or a new ILA capture command is executed.

10.6.5.8 ILA Reset

Offset	Bit	Type	Default	Definition
0x01AC	[31:1]	RO	0	Reserved
	[0]	WO	0	ILA function reset. Write 1 to reset ILA function. Auto-clear.

10.6.5.9 ILA RAM Data

Offset	Bit	Type	Default	Definition
0x0800 ~0x0FFC	[31:0]	RO	0	ILA captured data read from data RAM if capture is complete.

10.6.6 MDIO Controller

This section of register is for PIM DOM FPGA on Minipack.

10.6.6.1 MDIO Configuration Register

Offset	Bit	Type	Default	Definition
0x0200	[31]	WO	0	MDIO controller reset. 1- reset; 0 – reset release. Auto-clear.
	[30:9]	RO	0	Reserved
	[8]	RW	0	MDIO controller fast/normal mode control. 0 -- Normal mode 1 – Fast mode. MDIO idle time is significantly squeezed in fast mode.
	[7:0]	RW	0x14	MDC frequency division configuration. This register should be configured with a value = reference clock freq/MDC freq.

				Set it to decimal 20 for 2.5MHz MDC if reference clock is 50MHz.

10.6.6.2 MDIO Command Register

Offset	Bit	Type	Default	Definition
0x0204	[31:16]	RW	0	MDIO register address
	[15:13]	RW	0	Reserved
	[12:8]	RW	0	MDIO PHY device address. For device 0, assign 0x00; For device 1, assign 0x04; For device 2, assign 0x08; For device 4, assign 0x10
	[7]	RW	0	MDIO bus command register 0x1 -- Read command to MDIO bus 0x0 – Write command to MDIO bus Writing to this register will trigger MDIO transaction.
	[6:5]	RW	0	Reserved
	[4:0]	RW	0	MDIO PHY device type. BCM81724 device type is 0x1E when accessing through SDK for direct register access. BCM81724 device type is 0x1F when accessing per BCM81724 datasheet DS103 for indirect register access.

10.6.6.3 MDIO Write Data Register

Offset	Bit	Type	Default	Definition
0x0208	[31:16]	RO	0	Reserved
	[15:0]	RW	0	MDIO write data

10.6.6.4 MDIO Read Data Register

Offset	Bit	Type	Default	Definition
0x020C	[31:16]	RO	0	reserved
	[15:0]	RO	0	MDIO Read data

10.6.6.5 MDIO Status Register

Offset	Bit	Type	Default	Definition
0x0210	[31:16]	RO	0	reserved
	[15:8]	RO	0	MDIO debug status. [7] MDIO active status [6] MDIO frame counter [5:0] MDIO bit counter

	[7:3]	RO	0	Reserved
	[1]	W1C	0	MDIO bus transaction error has occurred. Write 1 to clear.
	[0]	W1C	0	MDIO bus transaction is done. Write 1 to clear.

10.6.6.6 MDIO Interrupt Mask

Offset	Bit	Type	Default	Definition
0x0214	[31:2]	RO	0	reserved
	[1]	RW	1	MDIO bus transaction error interrupt mask.
	[0]	RW	1	MDIO bus transaction done interrupt mask.

10.6.7 Port LED Control Register

10.6.7.1 Color Profile 0_1

Profile 0 default color is white; profile 1 default color is cyan.

Offset	Bit	Type	Default	Definition
0x0300	[31:28]	RO	0	RESERVED
	[27:24]	RW	0XF	Color profile 1 B brightness control
	[23:20]	RW	0XF	Color profile 1 G brightness control
	[19:16]	RW	0	Color profile 1 R brightness control
	[15:12]	RO	0	RESERVED
	[11:8]	RW	0XF	Color profile 0 B brightness control
	[7:4]	RW	0XF	Color profile 0 G brightness control
	[3:0]	RW	0XF	Color profile 0 R brightness control 0 : 0 % duty cycle 1: 1/15 duty cycle 2: 2 / 15 duty cycle …… E: 14/15 duty cycle F: 15/15 duty cycle

10.6.7.2 Color Profile 2_3

Profile 2 default color is blue; profile 3 default color is pink.

Offset	Bit	Type	Default	Definition
0x0304	[31:28]	RO	0	RESERVED
	[27:24]	RW	0XF	Color profile 3 B brightness control
	[23:20]	RW	0	Color profile 3 G brightness control
	[19:16]	RW	0XF	Color profile 3 R brightness control
	[15:12]	RO	0	RESERVED

	[11:8]	RW	0XF	Color profile 2 B brightness control
	[7:4]	RW	0	Color profile 2 G brightness control
	[3:0]	RW	0	Color profile 2 R brightness control

10.6.7.3 Color Profile 4_5

Profile 4 default color is red; profile 5 default color is orange.

Offset	Bit	Type	Default	Definition
0x0308	[31:28]	RO	0	RESERVED
	[27:24]	RW	0	Color profile 5 B brightness control
	[23:20]	RW	0X7	Color profile 5 G brightness control
	[19:16]	RW	0XF	Color profile 5 R brightness control
	[15:12]	RO	0	RESERVED
	[11:8]	RW	0	Color profile 4 B brightness control
	[7:4]	RW	0	Color profile 4 G brightness control
	[3:0]	RW	0XF	Color profile 4 R brightness control

10.6.7.4 Color Profile 6_7

Profile 6 default color is yellow; profile 7 default color is green.

Offset	Bit	Type	Default	Definition
0x030C	[31:28]	RO	0	RESERVED
	[27:24]	RW	0	Color profile 7 B brightness control
	[23:20]	RW	0XF	Color profile 7 G brightness control
	[19:16]	RW	0	Color profile 7 R brightness control
	[15:12]	RO	0	RESERVED
	[11:8]	RW	0	Color profile 6 B brightness control
	[7:4]	RW	0XF	Color profile 6 G brightness control
	[3:0]	RW	0XF	Color profile 6 R brightness control

10.6.7.5 Port LED control

Offset	Bit	Type	Default	Definition
0x0310	[31:5]	RO	0	RESERVED
	[4:2]	RW	0	Port#0 LED color profile 000 – color profile 0; 001 – color profile 1; … 111 – color profile 7.
	[1]	RW	0	Port#0 LED Flash control when LED on/off is set as ON. 0 – LED Flash disable

				1 – LED Flash enable
	[0]	RW	0	Port#0 LED on/off control 0 – LED off 1 – LED on
0x0314	[4:0]	RW	0	Port#1 LED control.
0x0318	[4:0]	RW	0	Port#2 LED control.
0x031C	[4:0]	RW	0	Port#3 LED control.
0x0320	[4:0]	RW	0	Port#4 LED control.
0X0324	[4:0]	RW	0	Port#5 LED control.
0X0328	[4:0]	RW	0	Port#6 LED control.
0X032C	[4:0]	RW	0	Port#7 LED control.
0X0330	[4:0]	RW	0	Port#8 LED control.
0X0334	[4:0]	RW	0	Port#9 LED control.
0X0338	[4:0]	RW	0	Port#10 LED control.
0X033C	[4:0]	RW	0	Port#11 LED control.
0X0340	[4:0]	RW	0	Port#12 LED control.
0X0344	[4:0]	RW	0	Port#13 LED control.
0X0348	[4:0]	RW	0	Port#14 LED control.
0X034C	[4:0]	RW	0	Port#15 LED control.

10.6.8 QSFP I2C Controller

Following is address mapping of these I2C controllers.

10.6.8.1 DOM Registers

10.6.8.1.1 I2C Protocol Profile 0 & 1

Offset	Bit	Type	Default	Definition
0x0400	[31:24]	RW	0x16	QSFP EEPROM temperature data bytes address, profile 0.
	[23:16]	RW	0x63	Clock divider for SCL, profile 0. 0x63 for 100KHZ SCL with 50MHz mclk. I2C_SCL_Div = 50MHz/(SCL Freq * 5) -1.
	[15:8]	RW	0x16	QSFP EEPROM temperature data bytes address, profile 1.
	[7:0]	RW	0x63	Clock divider for SCL, profile 1. 0x63 for 100KHZ SCL with 50MHz mclk. I2C_SCL_Div = 50MHz/(SCL Freq * 5) -1.

10.6.8.1.2 I2C State Machine Profile

Offset	Bit	Type	Default	Definition
0x0404	[31]	RW	0	1 -- Allow state machine timeout to reset the corresponding deadlock state machine. 0 – It is not allowed to reset deadlock state machine. Only error flags will be asserted upon deadlock detection.
	[30]	RW	0	1 – allow RTC controller auto reset at timeout It's suggested to disable this function since RTC controller has timeout scheme itself.
	[29]	RW	0	1 – allow scheduler auto reset at timeout
	[28]	RW	0	1 – allow DOM qport controller auto reset at timeout It's suggested to disable this function since DOM qport controller state machine has timeout scheme itself.
	[27:24]	RW	0	State machine timeout threshold in 500milliseconds for RTC Qport scheduler. If an active state is hanging for too long, a timeout event could be fired to reset the corresponding state machine. A value of zero disables this watchdog timer.
	[23:20]	RW	0	State machine timeout threshold in 500milliseconds for DOM qpor_scheduler. If an active state is hanging for too long, a timeout event could be fired to reset the corresponding state machine. A value of zero disables this watchdog timer.
	[19:16]	RW	0	State machine timeout threshold in 500milliseconds for DOM qport_controller. If an active state is hanging for too long, a timeout event could be fired to reset the corresponding state machine. A value of zero disables this watchdog timer.
	[15:0]	RW	0	Channel setup time for OBO in unit of us. 0x800 is suggested for OBO with 2.048ms setup time. Always use 0 for pluggable QSFP.

10.6.8.1.3 I2C Protocol Profile Configuration

Offset	Bit	Type	Default	Definition
0x0408	[31:CN]	RW	0	Reserved
	[CN-1:0]	RW	0	Per port I2C protocol profile selection. Each bit maps to a port. Bit 0 is for port 0, bit 1 is for port 1, etc.

				0 – use I2C protocol profile 0; 1 – use I2C protocol profile 1. The purpose of the timing profiles is to support both 400KHz SCL/SFF-8636 and 1MHz SCL/ACMIS on a same platform.

10.6.8.1.4 DOM I2C Controller Reset

Offset	Bit	Type	Default	Definition
0x040C	[31]	WO	0	Write 1 to reset DOM and RTC function. Auto-clear to 0.
	[30:CN/4]	RO	0	Reserved
	[CN/4-1:0]	WO	0	DOM/RTC controller per channel reset. Write 1 to reset the DOM I2C controller. Auto-clear to 0.

10.6.8.1.5 DOM Control Configuration

Offset	Bit	Type	Default	Definition
0x0410	[31]	RW	0	DOM memory manufacture test mode if this bit is 1. For normal operation, this bit should be always 0.
	[30:24]	RW	0x0	DOM refresh cycle bit[7:0] in seconds. If DOM data is not restarted by host in the specified refresh cycle, DOM engine will trash the DOM data already collected and restart DOM collection. The default DOM refresh cycle 0 disables auto refresh function. Max timeout setting is 2047s, which is about 34mins.
	[23:20]	RW	0x0	DOM refresh cycle bit[11:8]. Value of 1 in this register represents about 2mins of refresh cycle setting.
	[19:10]	RW	0x000	Reserved
	[11]	RW	1	DOM memory parity error interrupt mask
	[10]	RW	1	DOM state machine timeout interrupt mask
	[9]	RW	1	DOM global error interrupt mask.
	[8]	RW	1	DOM global done status interrupt mask.
	[7:1]	RW	0	RESERVED
	[0]	RW	0	0: DOM data collection is disabled. 1: DOM data collection is enabled. When DOM function is disabled, no DOM data collection will be executed.

10.6.8.1.6 DOM Global Status

Offset	Bit	Type	Default	Definition
0x0414	[31]	WO	0	Write 1 to enforce DOM engine to kick off a DOM data collection. Auto-clear to 0. Writing this register to 1 will also clear DOM status register bits – reg0x414.bit[3:0], reg0x418 and reg0x454.
	[30:24]	RO		Reserved
	[23:16]	RO	0	DOM data sequence number, increased by 1 when a new batch of data collection is completed.
	[15:4]	RO	0	Reserved
	[3]	W1C	0	DOM memory parity error.
	[2]	W1C	0	State machine timeout happened if it is 1.
	[1]	W1C	0	Global error status for DOM data collection. 0 – no errors during I2C access; 1 – DOM hit errors during I2C access. Write 1 to clear. Write 1 also clears “DOM Port Error Status”. QSFP not present is NOT considered as an error condition. Only I2C error and NACK are considered as error condition.
	[0]	W1C	0	Global done status for DOM data collection. 0 – DOM data is not ready; 1 – DOM data is ready. Write 1 to clear. In automode, a new start of DOM data collection will clear this bit. Write 1 also clears “DOM Port Done Status”. DOM data is ready for collection when all the ports meet one of the following conditions: 1. QSFP data is collected; 2. QSFP not present at the port; 3. I2C error or NACK has occurred.

10.6.8.1.7 DOM Per Port Valid Status

Offset	Bit	Type	Default	Definition
0x0418	[31:CN]	RO		
	[CN-1:0]	W1C	0x0	Per port DOM data is valid when 1. Each bit corresponds to one port. Bit0 – port 0; bit1 – port 1; etc. Write 1 to clear.

				When global DONE status register is cleared, these per port status register bits will be cleared too.

10.6.8.1.8 DOM Data Timestamp

Offset	Bit	Type	Default	Definition
0x041C	[31:0]	RO	0x0	When DOM global status is asserted DONE, this register will latch the current UP_TIME register value.

10.6.8.1.9 DOM Debug Register

Offset	Bit	Type	Default	Definition
0x0420	[31:29]	W1C	0	**QPort #1 scheduler/controller timeout**
	[28:24]	RO	0	State machine status, DOM Qport Scheduler #1
	[23:20]	RO	0	State machine status, DOM Qport Controler #1,
	[19:16]	RO	0	State machine status, RTC Qport controller #1
	[15]	W1C		QPort #0 scheduler timeout
	[14]	W1C		QPort #0 DOM controller timeout
	[13]	RO	0	Qport#0 RTC controller timeout
	[12:8]	RO	0	State machine status, DOM Qport scheduler, #0
	[7:4]	RO	0	State machine status, DOM Qport controller #0,
	[3:0]	RO	0	State machine status, RTC Qport controller #0
Offset	**Bit**	**Type**	**Default**	**Definition**
0x0424	[31:16]	RO/W1C	0	Debug, Qport #3
	[15:0]	RO/W1C	0	Debug, Qport #2
Offset	**Bit**	**Type**	**Default**	**Definition**
0x0428	[31:16]	RO/W1C	0	Debug, Qport #5, if applicable.
	[15:0]	RO/W1C	0	Debug, Qport #4, if applicable.
Offset	**Bit**	**Type**	**Default**	**Definition**
0x042C	[31:16]	RO/W1C	0	Debug, Qport #7, if applicable.
	[15:0]	RO/W1C	0	Debug, Qport #6, if applicable.

10.6.8.1.10DOM Page Descriptor 0-3

Offset	Bit	Type	Default	Definition
0x0430	[31:0]	RW	0x8000,0001	Bit[0] Descriptor valid. 1 – valid; 0 – invalid. Bit[3:1] Reserved. Bit[7:4] DOM bank number Bit[15:8] DOM page number, Bit[23:16] DOM data start address, default is 0. Bit[31:24] DOM data byte length, default is 0x80, for 128B.
0x0434	[31:0]	RW	0x0	
0x0438	[31:0]	RW	0x0	
0x043C	[31:0]	RW	0x0	

				Total of four descriptors are defined for DOM data collection. Each descriptor supports up to 128B of data collection. Descriptor 0 is mapped to the first 128B of data in DOM data block of a channel; descriptor 1 is mapped to the second 128B; descriptor 2 is mapped to the third 128B; and descriptor 3 is mapped the last 128B. If a descriptor is enabled, FPGA will collect the corresponding data from QSFP. If not, FPGA will fill zeros to the page data block.

10.6.8.1.11DOM MAX Temperature (For easy debugging)

Offset	Bit	Type	Default	Definition
0x0450	[31:24]	RO	0	Max temperature sequence number
	[23:16]	RO	0	Max temperature QSFP location
	[15:0]	RO	0	Max temperature read out of the QSFPs

10.6.8.1.12DOM Per Port Error Status (For debugging purpose)

Offset	Bit	Type	Default	Definition
0x0454	[31:CN]	RO		
	[CN-1:0]	W1C	0x0	Per port DOM data has error when 1. Each bit corresponds to one port. Bit0 – port 0; bit1 – port 1; etc. Write 1 to clear. When global DONE status register is cleared, these per port status register bits will be cleared too.

10.6.8.1.13I2C state machine status 0 (For debugging purpose)

Offset	Bit	Type	Default	Definition
0x0458	[31:24]	RO	0	I2C controller 3 state machine status
	[23:16]	RO	0	I2C controller 2 state machine status
	[15:8]	RO	0	I2C controller 1 state machine status
	[7:0]	RO	0	I2C controller 0 state machine status

10.6.8.1.14I2C state machine status 1 (For debugging purpose)

Offset	Bit	Type	Default	Definition
0x045C	[31:24]	RO	0	I2C controller 7 state machine status, if applicable.
	[23:16]	RO	0	I2C controller 6 state machine status, if applicable.
	[15:8]	RO	0	I2C controller 5 state machine status, if applicable.

	[7:0]	RO	0	I2C controller 4 state machine status, if applicable.

10.6.8.1.15I2C Advanced Timing Profile

Offset	Bit	Type	Default	Definition
0x0460	[31:24]	RW	0	Reserved
	[23:16]	RW	0	I2C sample rate profile 1 and I2C tBUF profile 1
	[15:8]	RW	0	Reserved.
	[7:5]	RW	4	I2C sample rate profile 0. Default is about 40ns sample period for 50MHz main clock and 100KHz SCL. 0 – sample period is main clock cycle x (SCL_DIV /4+1); 1 – sample period is main clock cycle x (SCL_DIV /8+1). 2 – sample period is main clock cycle x (SCL_DIV /16+1). 3 – sample period is main clock cycle x (SCL_DIV /32+1). 4 – sample period is main clock cycle x (SCL_DIV /64+1). Default. Etc…
	[4:0]	RW	0	I2C tBUF profile 0 Addition tBUF in microseconds inserted before Sr and before START.

10.6.8.1.16QSFP Tsensor Value

Offset	Bit	Type	Default	Definition
0x0480	[31:0]	RO	0	Each 32bit register contains two QSFP port temperature reading data. Reg0x0480 has temperature data for port 2 (bit[31:16]) and port 1 (bit[15:0]); Reg0x048c has temperature data for port 4 and port3. The remaining registers in this section follow this pattern.
0x0484	[31:0]	RO	0	
0x0488	[31:0]	RO	0	
0x048C	[31:0]	RO	0	
0x0490	[31:0]	RO	0	
0x0494	[31:0]	RO	0	
0x0498	[31:0]	RO	0	
0x049C	[31:0]	RO	0	
0x04A0	[31:0]	RO	0	QSFP port temperature reading data for port 17 – 32 if applicable.
0x04A4	[31:0]	RO	0	
0x04A8	[31:0]	RO	0	
0x04AC	[31:0]	RO	0	
0x04B0	[31:0]	RO	0	
0x04B4	[31:0]	RO	0	
0x04B8	[31:0]	RO	0	
0x04BC	[31:0]	RO	0	

10.6.8.2 QSFP Real Time Access Registers

10.6.8.2.1 I2C RTC0 Descriptor

Offset	Bit	Type	Default	Definition
0x0500	[31:30]	RW	0	Reserved
	[29:28]	RW	2'b11	I2C Command. When this register is being written, a corresponding I2C command will kick off. 00 – Write 01 – Read 10 – SCL Flush. 9 SCL + 1 STOP sequence. 11 -- reserved (descriptor is invalid)
	[27:24]	RW	0	Reserved
	[23:16]	RW	0	Reserved
	[15:8]	RW	0	Reserved
	[7:0]	RW	0	Number of I2C Data in byte. This register supports 0, 1, 2 and up to 128 bytes of I2C data access.
0x0504	[31]	RW	0	Descriptor Valid bit 1 – to trigger a new I2C transaction.
	[30:26]	RW	0	Reserved.
	[25:24]	RW	0	Channel ID. 0-3 to specify the desired I2C channel for access.
	[23:16]	RW	0	Bank byte
	[15:8]	RW	0	Page byte
	[7:0]	RW	0	I2C Register Address Byte.
0x0508 0x050C	[31:0]	RW	C0000000	I2C RTC0 Descriptor #1
0x0510 0x0514	[31:0]	RW	C0000000	I2C RTC0 Descriptor #2
0x0518 0x051C	[31:0]	RW	C0000000	I2C RTC0 Descriptor #3

10.6.8.2.2 I2C RTC[1:5] Descriptor

Offset	Bit	Type	Default	Definition
0x0520- 0x053C	[31:0]	RW	C0000000	I2C RTC1 Descriptor #0-3
0x0540- 0x055C	[31:0]	RW	C0000000	I2C RTC2 Descriptor #0-3
0x0560- 0x057C	[31:0]	RW	C0000000	I2C RTC3 Descriptor #0-3

0x0580-0x059C	[31:0]	RW	C0000000	I2C RTC4 Descriptor #0-3, if applicable.
0x05A0-0x05BC	[31:0]	RW	C0000000	I2C RTC5 Descriptor #0-3, if applicable.
0x05C0-0x05DC	[31:0]	RW	C0000000	I2C RTC6 Descriptor #0-3, if applicable.
0x05E0-0x05FC	[31:0]	RW	C0000000	I2C RTC7 Descriptor #0-3, if applicable.

10.6.8.2.3 I2C RTC0 Status

Offset	Bit	Type	Default	Definition
0x0600	[31:17]	RO	0	RESERVED.
	[16]	W1C	0	Memory parity error
	[15:14]	RO	0	RESERVED
	[13:12	W1C	0	I2C Controller #0 descriptor #3 status.
	[11:10]	RO	0	RESERVED.
	[9:8]	W1C	0	I2C Controller #0 descriptor #2 status.
	[7:6]	RO	0	Reserved
	[5:4]	W1C	0	I2C Controller #0 descriptor #1 status.
	[3]	RO	0	RESERVED
	[2]	RO		I2C controller Busy when 1. For debugging only.
	[1]	W1C	0	I2C controller #0 descriptor #0error when 1. Write 1 to clear. This register will be also cleared whenever a new I2C transaction starts. The error defined for this register bit includes no ACK and I2C bus lock up.
	[0]	W1C	0	I2C controller done when 1. Write 1 to clear. This register will be also cleared whenever a new I2C transaction starts.

10.6.8.2.4 I2C RTC[1:5] Status

Offset	Bit	Type	Default	Definition
0x0604	[31:0]	RO	0	I2C RTC1 status
0x0608	[31:0]	RO	0	I2C RTC2 status
0x060C	[31:0]	RO	0	I2C RTC3 status
0x0610	[31:0]	RO	0	I2C RTC4 status, if applicable.
0x0614	[31:0]	RO	0	I2C RTC5 status, if applicable.
0x0618	[31:0]	RO	0	I2C RTC6 status, if applicable.

0x061C	[31:0]	RO	0	I2C RTC7 status, if applicable.

10.6.8.2.5 I2C RTC0 Interrupt Mask

Offset	Bit	Type	Default	Definition
0x0620	[31:17]	RO	0	RESERVED.
	[16]	RW	1	Parity error interrupt mask
	[15:14]	RO	0	Reserved
	[13:12]	RW	All 1's	I2C interrupt mask for I2C controller#0 descriptor #3.
	[11:10]	RO	0	RESERVED.
	[9:8]	RW	All 1's	I2C interrupt mask for I2C controller#0 descriptor #2.
	[7:6]	RO	0	
	[5:4]	RW	All 1's	I2C interrupt mask for I2C controller#0 descriptor #1.
	[3:2]	RO	0	
	[1]	RW	1	I2C error interrupt mask. 1 to mask I2C controller error interrupt.
	[0]	RW	1	I2C done interrupt mask. 1 to mask I2C controller done interrupt.

10.6.8.2.6 I2C RTC[1:5] Interrupt Mask

Offset	Bit	Type	Default	Definition
0x0624	[31:0]	RW	All 1's	I2C RTC1 interrupt mask
0x0628	[31:0]	RW	All 1's	I2C RTC2 interrupt mask
0x062C	[31:0]	RW	All 1's	I2C RTC3 interrupt mask
0x0630	[31:0]	RW	All 1's	I2C RTC1 interrupt mask
0x0634	[31:0]	RW	All 1's	I2C RTC1 interrupt mask
0x0638	[31:0]	RW	All 1's	I2C RTC2 interrupt mask
0x063C	[31:0]	RW	All 1's	I2C RTC3 interrupt mask

10.6.8.3 I2C RTC Data Block

10.6.8.3.1 I2C Descriptor Write Data

Offset	Bit	Type	Default	Definition
0X2000-0X21FF	[31:24]	RW	0x0	I2C Write Data Byte 3.
	[23:16]	RW	0x0	I2C Write Data Byte 2.
	[15:8]	RW	0x0	I2C Write Data Byte 1.
	[7:0]	RW	0x0	I2C Write Data Byte 0. If data length is 1, this byte is the valid byte. This byte is transferred first. RTC0 I2C Descriptor 0-3 write data memory
0x2200-0x23FF	[31:0]	RW	0	RTC1 I2C Descriptor 0-3 write data memory

0x2400-0x25FF	[31:0]	RW	0	RTC2 I2C Descriptor 0-3 write data memory
0x2600-0x27FF	[31:0]	RW	0	RTC3 I2C Descriptor 0-3 write data memory
0x2800-0x29FF	[31:0]	RW	0	RTC4 I2C Descriptor 0-3 write data memory, if applicable.
0x2A00-0x2BFF	[31:0]	RW	0	RTC5 I2C Descriptor 0-3 write data memory, if applicable.
0x2C00-0x2DFF	[31:0]	RW	0	RTC6 I2C Descriptor 0-3 write data memory, if applicable.
0x2E00-0x2FFF	[31:0]	RW	0	RTC7 I2C Descriptor 0-3 write data memory, if applicable.

10.6.8.3.2 I2C Read Data 0-7

Offset	Bit	Type	Default	Definition
0x3000	[31:24]	RO	0x0	I2C Read Data Byte 3.
	[23:16]	RO	0x0	I2C Read Data Byte 2.
	[15:8]	RO	0x0	I2C Read Data Byte 1.
	[7:0]	RO	0x0	I2C Read Data Byte 0. If data length is 1, this byte is the valid byte. This byte is received first. This memory can be overwritten in manufacture test mode. RTC0 I2C Descriptor 0-3 read data memory
0x3200-0x33FF	[31:0]	RW	0	RTC1 I2C Descriptor 0-3 read data memory
0x3400-0x35FF	[31:0]	RW	0	RTC2 I2C Descriptor 0-3 read data memory
0x3600-0x37FF	[31:0]	RW	0	RTC3 I2C Descriptor 0-3 read data memory
0x3800-0x39FF	[31:0]	RW	0	RTC4 I2C Descriptor 0-3 read data memory, if applicable.
0x3A00-0x3BFF	[31:0]	RW	0	RTC5 I2C Descriptor 0-3 read data memory, if applicable.
0x3C00-0x3DFF	[31:0]	RW	0	RTC6 I2C Descriptor 0-3 read data memory, if applicable.
0x3E00-0x3FFF	[31:0]	RW	0	RTC7 I2C Descriptor 0-3 read data memory, if applicable.

10.6.9 DOM Data Block

Offset	Bit	Type	Default	Definition

0x4000 ~0x41FF	[31:0]	RO*	0x0	512B DOM data block for port 0. For normal operation, this memory is read only. The last byte of the 512B block is a sequence number being updated automatically every time DOM data block is collected. Byte 0 is LSB. Sequence number is Byte 3, bit[31:24]. The sequence number in the DOM data memory lags the sequence number in "DOM Global Status" register and "DOM Max temperature" register by 1 count by design. When manufacture test mode is enable, this memory can be write/read for testing purpose.
0x4200 ~0x43FF	[31:0]	RO*	0x0	512B DOM data block for port 1
0x4400 ~0x45FF	[31:0]	RO*	0x0	512B DOM data block for port 2
0x4600 ~0x47FF	[31:0]	RO*	0x0	512B DOM data block for port 3
0x4800 ~0x49FF	[31:0]	RO*	0x0	512B DOM data block for port 4
0x4a00 ~0x4bFF	[31:0]	RO*	0x0	512B DOM data block for port 5
0x4c00 ~0x4dFF	[31:0]	RO*	0x0	512B DOM data block for port 6
0x4e00 ~0x4fFF	[31:0]	RO*	0x0	512B DOM data block for port 7
0x5000 ~0x51FF	[31:0]	RO*	0x0	512B DOM data block for port 8
0x5200 ~0x53FF	[31:0]	RO*	0x0	512B DOM data block for port 9
0x5400 ~0x55FF	[31:0]	RO*	0x0	512B DOM data block for port 10
0x5600 ~0x57FF	[31:0]	RO*	0x0	512B DOM data block for port 11
0x5800 ~0x59FF	[31:0]	RO*	0x0	512B DOM data block for port 12
0x5a00 ~0x5bFF	[31:0]	RO*	0x0	512B DOM data block for port 13
0x5c00 ~0x5dFF	[31:0]	RO*	0x0	512B DOM data block for port 14

0x5e00 ~0x5fFF	[31:0]	RO*	0x0	512B DOM data block for port 15
0x4000 +n*0x200	[31:0]	RO*	0x0	512B DOM data block for port n if applicable.

10.6.10 BMC Registers

The I2C slave 7bit device ID: IOB I2C SLAVE DEV ID IS 0X35; PIM DOM SLAVE DEV ID IS 0X60)

Following is the registers on I2C slave interface. These registers are all 8bit.

The registers at address 0x0 -0xEF are directly shared between BMC and CPU. FPGA registers accessible by CPU are all 32bit in nature. Following is the mapping of I2C byte access to 32bit FPGA registers.

I2C Offset	FPGA Register bits
0	[31:24]
1	[23:16]
2	[15:8]
3	[7:0]

The registers at address 0XF0 and above defined in this section is dedicated for BMC only. CPU can't access 0XF0-0XFF registers in this section. BMC can use the address/data/command registers defined in address 0XF0- 0XFA to access FPGA full memory space.

Reg Index	Type	Definition
0-0x3F	RW	FPGA general register direct access
0x40-0x7F	RW	FPGA QSFP IO register direct access
0x80-0xEF	RO	Reserved direct access to FPGA.
0xF0	RW	Indirect Access Address register 31:24]
0xF1	RW	Indirect Access Address register [23:16]
0xF2	RW	Indirect Access Address register [15:8]
0xF3	RW	Indirect Access Address register [7:0]
0xF4	RW	Indirect Access Write data register [31:24]
0xF5	RW	Indirect Access Write data [23:16]
0xF6	RW	Indirect Access Write data [15:8]
0xF7	RW	Indirect Access Write data [7:0]
0xF8	RO	Indirect Access Read data [31:24]
0xF9	RO	Indirect Access Read data [23:16]
0xFA	RO	Indirect Access Read data [15:8]
0xFB	RO	Indirect Access Read data [7:0]

0xFC	RW	Indirect Access Command Register. bit0 = 1 is for write; bit0 = 0 is for read. Writing to this register will trigger an indirect access.

11 Optics Transceivers Supported

11.1 100G optics

- QSFP28 CWDM4-OCP 100G transceiver
- QSFP28 CWDM4 100G transceiver (MSA)
- QSFP28 LR4/LR4-lite 100G transceiver (IEEE)
- QSFP28 SR4 100G transceiver (IEEE)

11.2 200G optics

- QSFP56 FR4 200G transceiver
- QSFP56 DR4 200G transceiver

11.3 400G optics

- QSFP56-DD FR4 400G transceiver
- QSFP56-DD DR4 400G transceiver

11.4 40G optics

- QSFP+ LR4 40G transceiver
- QSFP+ SR4 40G transceiver

12 Host CPU and BMC Functional Features

12.1 COM-Express CPU BIOS Feature List

The COM-Express module vendor shall be responsible for supplying, customizing, and sustaining the BIOS for the SOC. The requirements are outlined below. However, new requirements may arise in the full product life cycle.

- **Intel TXT support, and supporting Intel Dynamic Boot (DRTM – Dynamic Root of Trust for Measurements)**
- UEFI compatible
- Configuration and features
    - Disable unused devices including video interfaces and GPU if supported by hardware
    - BIOS setup menu
    - SoC settings to allow tuning to achieve the optimal combination of performance and power consumption
- Linux-based BIOS settings tool
- Default boot device priority
    - Network / PXE -> 1st off-module SATA -> Other removable devices
- PXE boot
    - Supports IPv4 and IPv6 UEFI PXE boot and provide the ability to modify the boot sequence. When PXE booting, the card first attempts to boot from the first Ethernet device (eth0).
    - PXE timeout timer set to 10 seconds
    - Supports UEFI mode
    - Supports both PXE boot over IPv4 and IPv6, and be able to boot from a PXE server on a different IPv4 or IPv6 subnet
- Other boot options
    - Also supports booting from SATA and USB interfaces
    - Provides the capability to select boot options
- Remote BIOS update
    - Scenario 1: Sample / audit BIOS settings
    - Scenario 2: Update BIOS with pre-configured set of BIOS settings
    - Scenario 3: BIOS / firmware update with a new revision
    - Update from the CentOS operating system over the LAN

    - Can complete BIOS update or setup change with a single reboot (no PXE boot, no multiple reboots)
    - No user interaction (e.g., prompts)
    - BIOS updates and option changes do not take longer than five minutes to complete.
    - Can be scripted and propagated to multiple machines
- Event log
    - Implement SMBIOS Type 15 System Event Log per SMBIOS specification Rev 2.6
    - Hold more than 500 event records (assuming the maximum event record length is 24 bytes, then the size will be larger than 12KB)
    - Each event record includes enhanced information identifying the error source device's vendor ID, card slot ID, and device ID.
    - A system access interface and application software to retrieve and clear the event log from the BIOS
- Logged errors
    - Single-bit ECC error
    - Multi-bit ECC error
    - PCIe error
    - SATA error
    - POST error
    - NMI error
    - System reboot events
    - Sensor values exceeding warning or critical thresholds
- Error thresholds
    - Setting must be enabled for both correctable and uncorrectable errors.
    - Threshold for Memory Correctable ECC is 1.
    - PCIe error threshold is 1.
- Console redirection to the serial ports
    - Console redirection shall be enabled whenever the CPU starts booting and kept enabled after the OS starts running.
- POST codes
    - To be provided on the serial console
    - To be provided on the LPC bus
- DMI
    - Model
    - Serial Number
    - Additional information if requested by Facebook

- ATA Security State 2
    - The BIOS shall not send out ATA “frozen” command to the SSDs attached to the SATA ports.
- Support AMI RuntimeMemoryHole eModule, so that we can avoid using the kernel module of SCELNX and AFULNX.
- Off-module BIOS Flash on the SPI interface of the COM-Express connector
    - The SoC shall use the off-module BIOS when BIOS_DIS[1:0]# = 0b01.
- **ONIE support is required.**

12.2 BMC Feature Support

The BMC on Minipack modules need to support the following features:

- All SEL commands
- All sensor commands
- All SDR commands
- TPM 2.0 support
- Power on/off/cycle / hardware reset / soft reset commands
- I2C access to Power Sequencer, and DC-DC convertor
- Inventory EEPROM access
- Fan-tray present status check, fan PWM control and speed status read
- Dual SPI boot
- On-board OOB switch MDIO interface access
- On-board PHY MDIO interface access
- CPLD and FPGA online upgrade

13 Mechanical Architecture

13.1 Chassis

Minipack is designed to fit in an EIA 19” rack with 4 RU height.

Dimension	Specification	Comment
Chassis Width	440.4mm (17.34”)	Outer dimension
Chassis Depth	738.1mm (29.06”)	Outer dimension
Chassis Height	176.2mm (6.94”)	Outer dimension

Table 41: Minipack Chassis Dimensions

A fully-populated Minipack chassis with PIM-16Q weights about 54Kg.

The following diagrams show the Minipack chassis assembly from front and from rear.

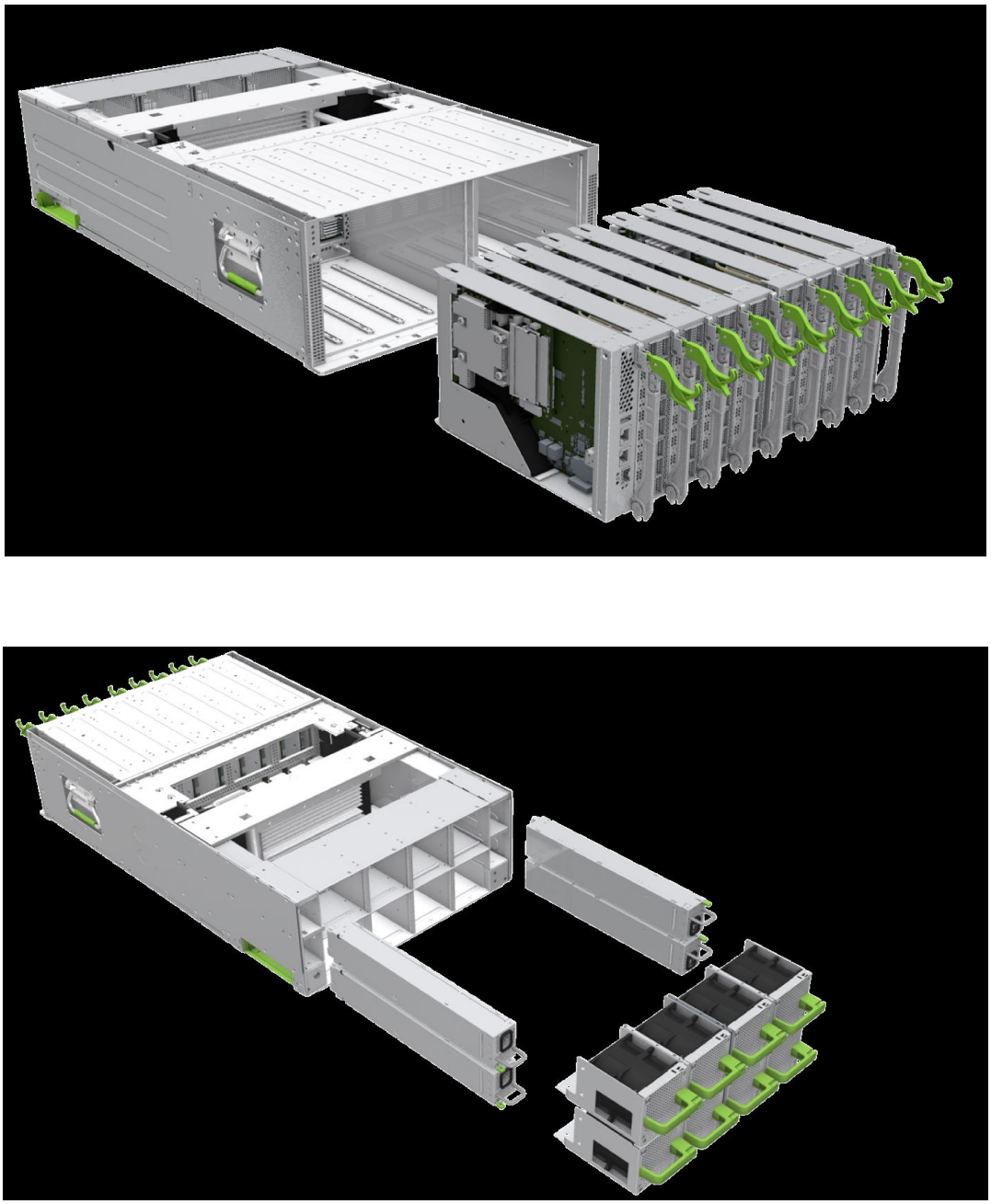


Figure 13-1: Minipack Chassis Assembly Diagrams

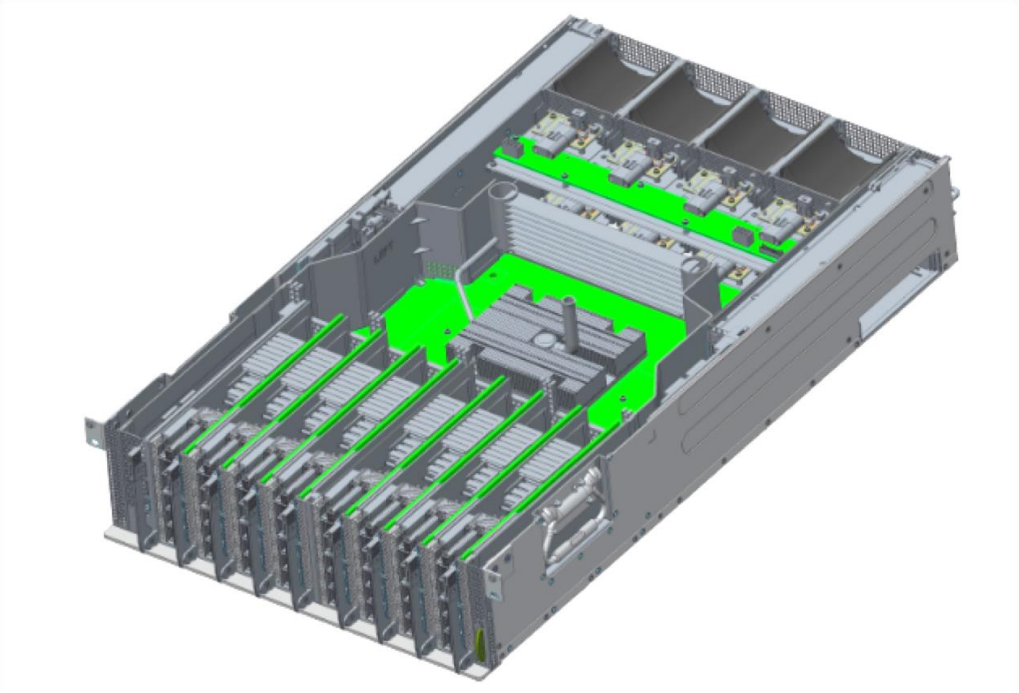


Figure 13-2: Minipack Top Cross-Sectional View

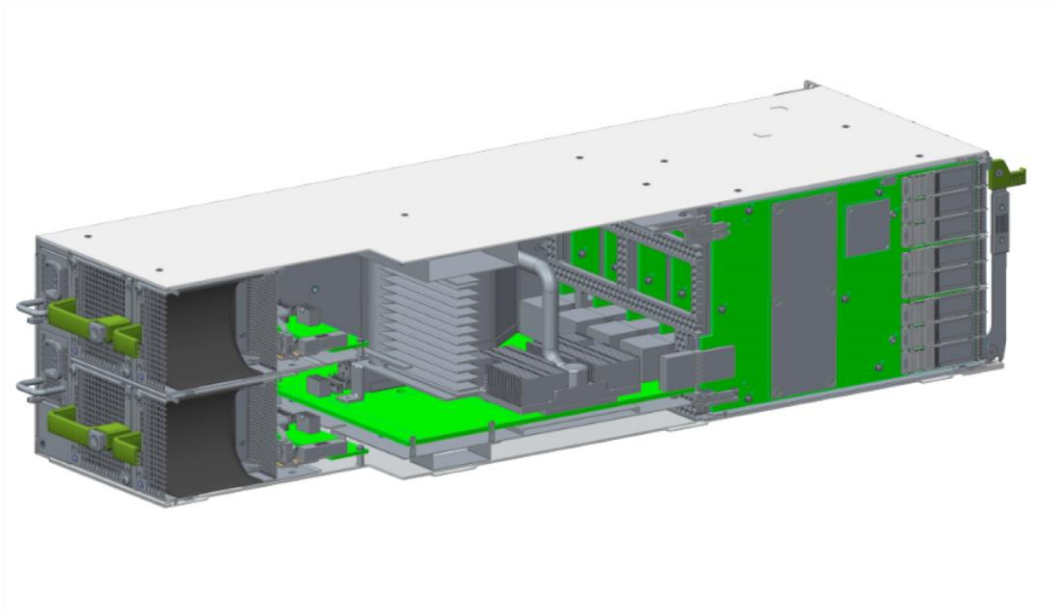


Figure 13-3: Minipack Side Cross-Sectional View

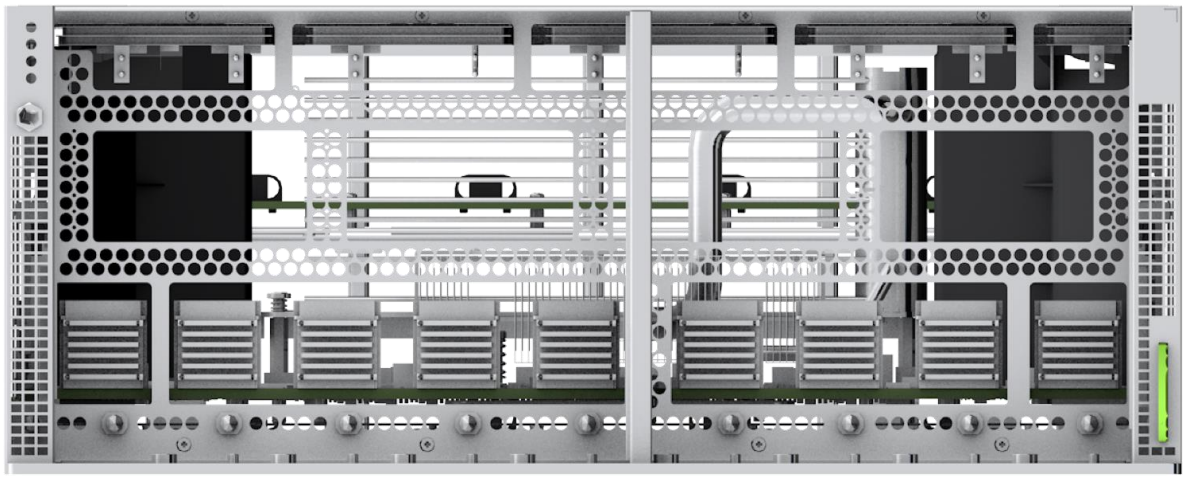


Figure 13-4: Minipack Chassis Middle Frame with Venting Holes\

14 Regulatory Compliance, Environmental, and Reliability Requirements

14.1 Regulatory Compliance Requirements

Compliance reports must be from labs accredited to a current version of IEC 17025. The reports and certificates must name the ODM as the applicant.

- **CE Declaration to the following Regulatory Directives by ODM:**
  - EMC Directive 2014/30/EU
  - Low Voltage (LVD) Directive 2014/35/EU
- **Safety certification**
  - CB certificate/report to IEC 62368-1 including all national deviations
  - CB certificate/report to IEC/EN 60950-1 including all national deviations
  - UL/CSA/IEC/EN 60950-1 with all latest amendments
  - UL/IEC 62368-1 with all latest amendments
  - CNS14336 Taiwan BSMI safety regulation
  - EN 60825-1 Safety of Laser products – part 1
  - UL 94-V0 Flammability rating
- **EMC certification**
  - FCC Part 15 (Class A)
  - ICES-003 (Canada) Class A
  - EN55032 (Europe) Class A
  - CISPR32 (International) Class A
  - AS/NZS CISPR32 (Australia and New Zealand) Class A
  - VCCI CISPR 32 (Japan) Class A
  - CNS 13438 (Taiwan) Class A
  - EN61000-3-2
  - EN61000-3-3
  - EN55024
  - EN 61000-4-2 ESD
  - EN 61000-4-3 Radiated Immunity
  - EN 61000-4-4 EFT
  - EN 61000-4-5 Surge
  - EN 61000-4-6 Low Frequency Conducted Immunity
  - EN 61000-4-11 Voltage Variations and Dips

- **Immunity levels**

Network Equipment						
Immunity Standard	**Description**	**Standard Criteria (Required)**	**FB Criteria (Goal)**	**Standard Level (Required)**	**FB Level (Goal)**	**Remarks**
IEC 61000-4-2	**Electrostatic Discharge (ESD)**	**B**	**A**	**4 kV Cont. / 8 kV Air**	**8 kV Cont. / 15 kV Air**	**Criteria A (FB Goal) is highly desirable for any level**
IEC 61000-4-3	**Radiated Immunity**	**A**	**A**	**3 V/m**	**10 V/m**	**For communication cables >3 meters**
IEC 61000-4-4	**EFT**	**B**	**B**	**0.5 kV**		**Ports: Signal &Telecom (>3 meters), DC power input**
		B	**B**	**1 kV**		**Ports: AC power input & AC/DC Converter**
IEC 61000-4-5	**Surges**	**C**	**A**	**1 kV**		**Ports: Signal and Telecom connected to outdoor cables**
		B	**A**	**0.5 kV**		**Ports: DC power input**
				1 kV L-L / 2 kV L-GND		**Ports: AC power input & AC/DC Converter**
IEC 61000-4-6	**Conducted Immunity**	**A**	**A**	**3 V**	**10 V**	**Ports: Signal & Telecom (>3 meters), AC and DC power input**

IEC 61000-4-8	**Magnetic Field**	**A**	**A**	**1 A/m**		**Only EUT containing devices susceptible to magnetic fields**
IEC 61000-4-11	**Voltage Dips**	**B**	**B**	**>95% Reduction**		**Ports: AC power input & AC/DC Converter (0.5 Period)**
		C	**C**	**30% Reduction**		**Ports: AC power input & AC/DC Converter (25 Periods)**
	Voltage Interruptions	**C**	**C**	**>95% Reduction**		**Ports: AC power input & AC/DC Converter (250 Periods)**

The ODM must strive to design to the FB Goal at the start and during the project. Facebook will decide if levels below the goal are acceptable. Off the shelf power supplies must meet the required level at a minimum.

- **Sound levels**

Network Equipment				
	OHSA (Required)	**Directive 2003/10/EC (Goal)**	**FB Design Goal**	**Remarks**

Sound Limit (dBA)	**85**	**80**	**78**	**Under normal operation at 25 °C, the system must not produce a A-weighted sound power level above the required limit. The FB design goal should be targeted during development of the product. The Directive goal represents the limit that requires hearing protection to be provided to our Data Center Staff in Europe. The ODM must provide the result of the formal testing.**

The ODM must strive to design to the FB Goal at the start and during the project. Facebook will decide if levels above the goal are acceptable. The sound power level limits apply to the normal operating conditions where the system is configured and equipped in its deployed state with the worst case configuration to produce the loudest noise. Maintenance conditions, open covers, are not considered normal conditions and do not need to be measured. Sound from alarms does not need to be measured. Maximum fan speed expected under normal operation should be measured.

14.2 Materials of Concern Requirements

Regulatory

- RoHS Directive (2011/65/EU), including provisions of RoHS 3 Directive (2015/863) upon coming into effect.
- REACH Regulation (EC) No 1907/2006
- Waste Electrical and Electronic Equipment ("WEEE") Directive (2012/19/EU)
- The Persistent Organic Pollutants Regulation (EC) No. 850/2004
- The California Safe Drinking Water and Toxic Enforcement Act of 1986 ("Prop 65")
- The Packaging and Packaging Waste Directive 94/62/EC
- Batteries Directive 2006/66/EC

Corporate Sustainability Requirements

- **RoHS Exemptions position:** Compliance to the latest version of RoHS Directive is mandatory, and FB requires the use of no exemption where practical. If not practically possible, using the following exemption is allowed based on EU directive (2011/65/EU, 2015/863/EU) or future decision by European commission. As of the last revision date of this standard, relevant exemptions include 5a, 5b, 6a, 6b, 6c, 7a, 7c-I, 7c-II, 7c-IV, 8b, 9, 9b, 13(a), 13(b), 15, 21
- **Halogens (Bromine & Chlorine and their compounds)***
- **Phthalates (DEHP, DBP, DiBP, BBP)***
- **Arsenic and its compounds***
- **Emerging: US Conflict Minerals law: section 1502 of the Dodd-Frank Act**; requires companies using tin, tantalum, tungsten, and gold ("3TG") in in-scope products to verify and disclose the mineral source.

See the table (below) for scope, concentration limits, exemptions, and compliance deadlines for requirements marked with an asterisk (*).

HAZARDOUS SUBSTANCE	CAS NUMBER	SCOPE	CONCENTRATION LIMIT OF INTEREST (FOR ALL HOMOGENOUS MATERIALS)	EXEMPTIONS	COMPLIANCE DEADLINE
Halogens (incl. PVC, BFRs/CFRs)	Br: 7726-95-6 Cl: 7782-50-5	All Parts	900 ppm for Br or Cl, or 1500 ppm combined	N/A	Dec 31, 2019
Phthalates (DEHP, DBP, DiBP, BBP)	DEHP: 117-81-7 DBP: 84-74-2 DiBP: 84-69-5 BBP: 85-68-7	All Parts	1000 ppm (or 0.1% by weight)	N/A	Jul 22, 2019 (RoHS 3.0)
Arsenic	Includes but is not limited to: 7440-38-2	Glass and non-metals	50 ppm (or 0,005% by weight)	Semiconductors, optical elements	Dec 31, 2020
		Metals and alloys	1000 ppm (or 0.1% by weight)	Copper foil for printed circuit boards	

Table 42: Corporate sustainability scope, concentration limits, exemptions, and compliance deadlines

14.3 Environmental Requirements

The Minipack system should meet the following environmental requirements:

- Gaseous contamination: Severity Level G1 per ANSI/ISA 71.04-1985
- Operating and storage relative humidity: 10% to 85% (non-condensing)
- Operating temperature range (with 100G CWDM4 MSA optics): 0°C to +45°C
- Operating temperature range (with 100G CWDM4-OCP optics): +15°C to +35°C
- Storage temperature range: -40°C to +70°C (long-term storage)
- Transportation temperature range: -55°C to +85°C (short-term storage)
- Operating altitude with no de-rating: up to 6,000 feet
- Shock and Vibration: IEC 68-2-36, IEC 68-2-6

14.4 Mean Time Between Failures (MTBF) Requirements

The MTBF of Minipack is required to be at least 5 years or 43,800 hours.

15 Labels and Markings

15.1 PCBA Labels and Markings

Minipack PCBAs shall include the following labels on the component side of the boards. The labels shall not be placed in such a way that may cause them to disrupt the functionality or the airflow path of the system.

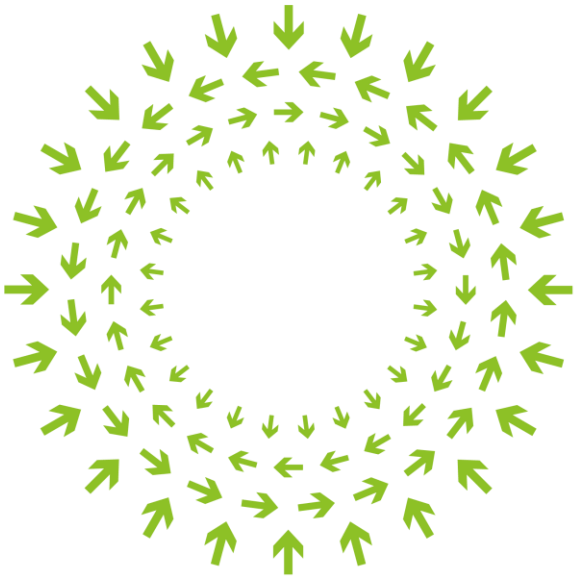
Table 43 PCBA Label Requirements

Description	Type	Barcode Required?
Safety markings	Silkscreen	No
Vendor P/N, S/N, REV (revision would increment for any approved changes)	Adhesive label	Yes
Vendor logo, name & country of origin	Silkscreen	No
PCB vendor logo, name	Silkscreen	No
Facebook P/N	Adhesive label	Yes
Date code (industry standard: WEEK/YEAR)	Adhesive label	Yes
DC input ratings	Silkscreen	No
RoHS compliance	Silkscreen	No
WEEE symbol:  The motherboard will have the crossed out wheeled bin symbol to indicate that it will be taken back by the manufacturer for recycling at the end of its useful life. This is defined in the European Union Directive 2002/96/EC of January 27, 2003 on Waste Electrical and Electronic Equipment (WEEE) and any subsequent amendments.	Silkscreen	No

15.2 Chassis Labels and Markings

The pull-out tag at the front panel of the chassis includes system model number, serial number, and Facebook asset tag.

16 Appendix A: Facebook Panel Indicator Specification (For Information Only)



Facebook Panel Indicator Specification

Version 1.0

Authors: Michael Haken - Facebook

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Table of Contents

2 Introduction

Current OCP hardware uses a variety of indicators to communicate information to service technicians. In many cases, these indicators are inconsistent, conflict with various diagnostic tools, communicate information of little use, or do not accommodate color-blind data center personnel. These issues can be alleviated by developing and adopting an indicator specification that address these concerns.

3 Guiding Principles

1. The primary function of indicators is to assist data center personnel in maintaining, servicing, or repairing data center equipment. Any indicators that exist solely to serve hardware teams during product development should be removed or deactivated before mass production.
2. The total set of permitted indicator behaviors and colors should be as simple as possible.
3. Indicators should not conflict with other diagnostic tools.
4. An indicator should communicate a clear message. A “decoder ring” should not be necessary.
5. Indicators should be consistent in behavior, colors, nomenclature, and graphics – both within and across all OCP products.
6. Indicators should do one or more of the following: provide component status, guide personnel to components that require service and/or identify actionable issues.
7. Indicators should conform to a constrained pallet of colors, be easily viewable, and accommodate users with color perception deficiencies.

4 General Rules

4.1 Indicator Colors

1. **Blue** and **amber** (yellow) are the permitted indicator colors. These two colors are easy to distinguish from each other for persons with the most common type of color perception deficiency.
2. Each color has a defined set of meanings and wavelengths. One or more meanings may be relevant, depending on the context:

Table 44. Permitted indicator colors

Color	Meaning(s)	Nominal Value (nm)	Acceptable Range (nm)
Blue	Power On, Functioning, Status Good, Link, Active	470	445-480
Amber	Fault, Locate	590	580-600

4.2 Indicator Intensity

1. The luminosity requirement depends on the indicator implementation. The luminosity of any light pipe viewing surface shall be controlled within the parameters below:

Table 45. Permitted luminosity of light pipes

Color	Nominal Value (Cd/m^2)	Acceptable Range (Cd/m^2)
Blue	1000	850-1150
Amber	2000	1700-2300

2. When LEDs with integrated glass viewing surfaces are used, the luminous intensity shall be controlled within the parameters below:

Table 46. Permitted intensity

Color	Nominal Value (mCd)	Minimum (mCd)
Blue	10	8

Amber	15	12

3. The required visible view angle of any indicator shall be ± 40 degrees horizontally and vertically. The luminosity within the view angle above shall be controlled within $\pm 25\%$ of the nominal spec value above. When possible, the vertical view angle should be ± 55 degrees.
4. Light pipe viewing surfaces shall receive texture to control brightness variance across the surface.
5. Indicators should not cause color-bleed or cross-talk in adjacent indicators. The cross-talk should not cause an increase of more than 20 Cd/m^2 in an adjacent indicator.

4.3 Indicator Behaviors

Indicators should be constrained to the following three behaviors:

OFF
ON (Steady on)
BLINK (1 Hz rate – 0.5s On, 0.5s Off)

Note: The blue LED graphic only serves as an example.

These behaviors only have meaning when they are combined with an indicator color, as will be shown in the *Permitted Indicator States* section.

4.4 Indicator Placement

1. All system or module status should be communicated with a pair of blue and amber indicators. For example, every fan module should have a blue indicator for Power/OK, and a separate amber indicator for Fault/Locate.
2. Indicator pairs must be arranged as: blue-left/amber-right, or blue-above/amber-below.
3. Paired indicators should be near each other while allowing for printed legends, and other panel features.
4. Whenever possible, indicators should not be closer than 6mm from one another (edge to edge).
5. Where space is limited, a single blue/amber indicator is permitted.
6. If more than one type of fault condition is to be communicated, additional amber indicators are permitted. They are to be to the right of, or below, the amber Fault/Location indicator.
7. For modules that are not visible from the front panel of a system, indicators for those modules should appear on the front panel of the system, via light pipes, cabled connections, etc.
8. Indicators should be visible on the front or rear panel of a system when viewing the panel from a perpendicular direction.

9. Indicators should always be surrounded by a panel to reduce background visual noise and provide a location for printed legends. No bare LEDs on PCBs are permitted.

4.5 Indicator Nomenclature

1. Where possible, all indicators should be identified with a legend that is adjacent to the indicator.
2. Text should be in black Arial condensed bold font with a minimum of 2.5mm font size whenever possible.
3. Where space is limited for placement of a legend, no legend will be required. For example, LEDs on a Quad Small Form-factor Pluggable (QSFP) cage.
4. Consistent nomenclature should be maintained on indicators for all products. Below are recommended legends for the most commonly found indicators on OCP equipment:

Table 47. OCP indicator legends

Meaning	Preferred	Alternate
Power On/Good		PWR
AC Good		AC OK
DC Good		DC OK
Fault		FAULT
Status		STS
Fan		FAN
Over Temperature		OVER TEMP
Drive #		DRIVE #
End of Life Reached (BBU)	EOL	N/A

Table 48. OCP icon reference standards

Indicator Icon	Reference Standard
	IEC 60417 - 5009
	IEC 60417 - 5032
	IEC 60417 - 5031
	ISO 7010 - W001
	IEC 60417 - 6334B

5 Permitted Indicator States

Separate LEDs **(preferred)**		Combined Blue/Amber LED **(use only if space is limited)**	Meaning(s) Communicated by each LED **(one or more meanings may be valid for blue LED)**	
Blue	**Amber**		**Blue**	**Amber**
OFF	OFF	OFF	Off/Not Functioning/Not Present. Service Action Allowed.	No Fault
ON	OFF	BLUE ON	On/Functioning. Link Established – No Activity.	No Fault
BLINK	OFF	BLUE BLINK	On/Functioning. Drive/Network Activity.	No Fault
OFF	ON	AMBER ON	Off/Not Functioning. Service Action Allowed.	Fault
OFF	BLINK	AMBER BLINK	Off/Not Functioning/Not Present. Service Action Allowed.	Locate
N/A[1]	N/A[1]	BLUE/AMBER Alternate	On/Functioning. Firmware Update in Progress. No Service Action Allowed	

[1] Firmware Update in Progress is indicated with alternating Blue/Amber blinking LEDs. A multi-color LED is required. Blinking frequency shall be 1Hz (i.e., 0.5sec blue followed by 0.5sec amber).

6 Indicator States as Applied to Specific Hardware

6.1 System Power Control/Status

If the product has a power button, it is permissible to integrate the Blue LED with the button. There should be a separate amber LED paired with the Power LED to indicate Fault or Locate. The blue power LED should not be used for these functions.

In the Permitted States descriptions, "/" = "and/or", "+" = "with"

Table 49. System power control/status LEDs

Permitted States	Separate LEDs	
	PWR (Blue)	**FAULT/LOC** (Amber)
System Off/Service Action Allowed		
System On/Status OK		
System Off + Fault		
System On + Locate		
System Off + Locate		
System On + Fault		

6.2 System General Status

Some products, such as Backpack[2], have LEDs that indicate the overall status for particular types of modules within the system chassis. For example, a pair of status LEDs might indicate the condition of all of the fan modules, without reporting the condition of any particular fan module. In this case, the locate function is inappropriate.

Table 50. System general status LEDs

Permitted States	Separate LEDs **(preferred)**		Combined Blue/Amber LED **(limited space)**
	STS (Blue)	**FAULT** (Amber)	STS
All Modules (e.g Fans, PSUs, etc.) present and OK.			
One or more modules are not plugged in.			
One of more modules has a fault or alarm condition.			

6.3 Generic Module/Compute Node Status

Table 51. Generic module/compute node status LEDs

Permitted States	Separate LEDs **(preferred)**		Combined Blue/Amber LED **(limited space)**
	STS (Blue)	**FAULT/LOC** (Amber)	STS
Module Off/Service Action Allowed			
Module On/Status OK			
Module Off + Fault			
Module Off + Locate			

[2] http://www.opencompute.org/wiki/Networking/SpecsAndDesigns#Facebook_Backpack_-_128x100G

Module On + Locate			
Firmware Update in Progress	N/A	N/A	

6.4 PSU Status

If multiple fault conditions exist for Power Supply Units (PSUs), there should be separate amber LEDs for each type of fault that is being identified (e.g. under voltage, AC outage, etc.). In this case, the general FAULT LED should be used for the LOCATE function.

Table 52. PSU status LEDs

Permitted States

AC	**AC OK** (Blue/Amber)	**FAULT/LOC** (Amber)	**LOW V** (Amber)	**BACK UP** (Amber)
AC OK				
AC Fault				
AC Under Voltage				
Backup due to AC Outage				
Locate				
Firmware Update in Progress				

DC	**DC OK** (Blue)	**FAULT/LOC** (Amber)	**LOW V** (Amber)	**SHUT DOWN** (Amber)
DC OK				
DC Voltage out of Regulation				
DC Shutdown				

6.5 BBU Status

Table 53. BBU status LEDs

Permitted States	Separate LEDs			
	BBU OK (Blue)	**FAULT/LOC**(Amber)	**LOW V** (Amber)	**EOL** (Amber)
Sleep				
BBU On/Available + Status OK				
BBU Fault				
BBU Under Voltage				
End of Life Reached				
BBU Off/Not OK + Locate				
BBU On/OK + Locate				

6.6 QSFP Module Status

Each QSFP module has a corresponding receive (RX) and transmit (TX) LED on the QSFP cage into which it is plugged. The table below lists the permitted states for both receive and transmit.

Table 54. QSFP module status LEDs

Permitted States (both RX and TX LEDs)	Combined Blue/Amber LED
Link is Down	
Link Established + No Activity	
Link Established + Activity	

Port Error	
Locate	

6.7 HDD

Table 55. HDD LEDs

Permitted States	Separate LEDs (preferred)		Combined
	DRIVE (Blue)	**FAULT/LOC**(Amber)	Blue/Amber LED (limited space) DRIVE
No Drive/Drive Off/Drive Not Seated/No Link			
Drive On + Link Established + No Activity			
Drive On + Link Established + Activity			
Drive Off + Fault			
Locate			

6.8 Fan Module

Table 56. Fan module LEDs

Permitted States	Separate LEDs **(preferred)**		Combined
	FAN (Blue)	**FAULT/LOC** (Amber)	Blue/Amber LED **(limited space)** FAN
Fan Off			
Fan On and is within Normal Speed Range			
Fan Off + Fault/Below Threshold Speed			

Locate   

7 LED Brightness and Wavelength Test Procedure

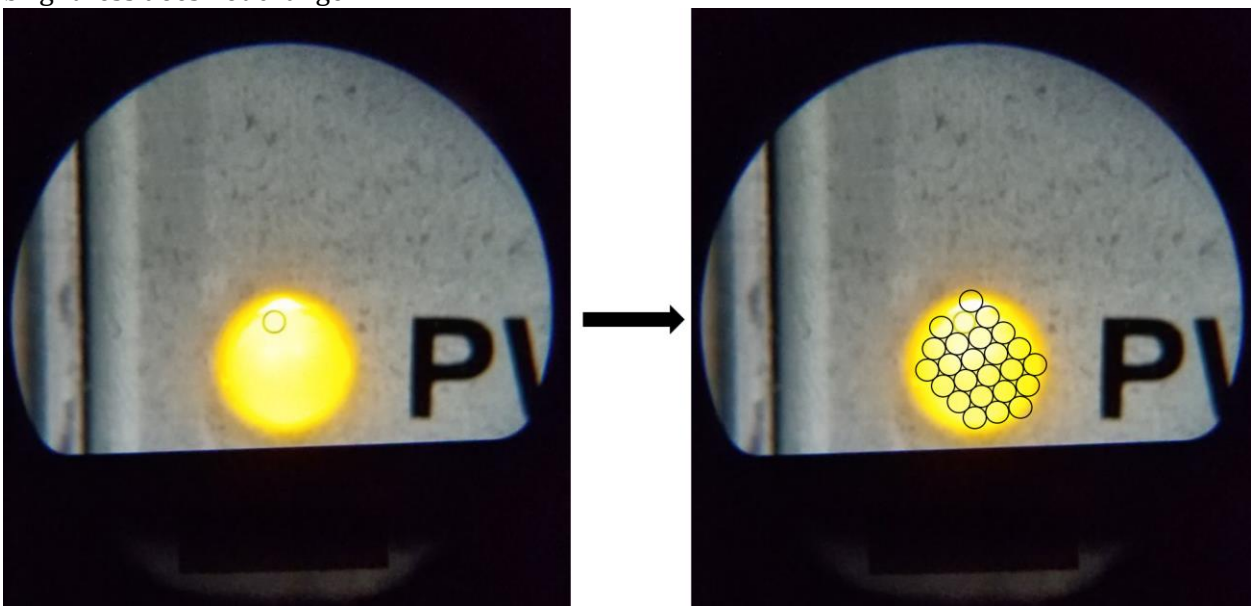
7.1 Equipment

- Konica Minolta LS-160 or equivalent
- Close-up lens No. 110 or equivalent
- Tripod with 3 axis fine adjustment

7.2 Procedure

Follow test procedure as outlined in luminosity sensor manual. For Konica Minolta LS-160:

1. Determine the required distance from the light source as dictated by the lens. The LS-160 with close-up lens #110 should be placed 214mm from the light source.
2. Adjust the viewfinder until the measuring circle is clearly visible.
3. Adjust the lens focus until the front panel is clearly visible. Note: the measuring circle for the #110 lens should appear approximately 0.5 mm in diameter when 214 mm from the light source. The measuring circle should be small enough to capture any brightness variations on the surface of the indicator.
4. Measure as many locations on the surface of the light source until the entire surface has been measured, without any overlapping measurements. This will create a grid of measurements sufficient to determine the brightness variation on the surface. Take an average of the measurements and make sure the min and max values are within the required range. Throughout the measurement process, ensure the ambient room brightness does not change.



5. Repeat this procedure at the required view angle 4 times (left, right, top, and bottom)

6. To determine the dominant wavelength present, set the luminosity sensor to wavelength mode and measure one location at the center of the indicator. When measuring wavelength, try to avoid any hot spots that might be present on the surface.