The UADP Family

The history of UADP ASIC began in 2013 when Cisco introduced the Catalyst 3850 switch. As discussed, the ASIC design and manufacturing process is very complex and can take several years for any individual component or product. Several years of innovative work went into developing UADP.

UADP 1.0 took longer to design than most other fixed ASICs at the time as many components were entirely new and designed to be flexible. UADP 1.0 was the first version of a family of UADP ASICs which all share a common architecture. UADP 1.0 was built on a 65 nanometer (nm) process, while the latest UADP 3.0 was built on 16 nm. UADP has progressed significantly in terms of ASIC technology and has incorporated more transistors with each generation. Each additional transistor means additional performance, scalability, features, and functionalities can be built into the ASIC.

UADP 1.0/1.1

UADP 1.0 is a single core ASIC with 1.3 billion transistors, capable of 56Gbps of aggregate bandwidth. It was the first to deliver many of the programmable features discussed in previous sections. Due to its flexible nature, UADP 1.0 was one of the first ASICs to enable support for different, flexible types of packet encapsulations. The first generation of Catalyst 3850 and 3650 used UADP 1.0.

By 2015, a newer version of the same ASIC design (version 1.1) was introduced. The core element and the architecture of the ASIC remained essentially the same, but with some important new additions. The key difference between UADP 1.0 and 1.1 is the use of a dual-core architecture inside the ASIC.

Unlike UADP 1.0, the UADP 1.1 has two ASIC cores with 3 billion transistors. The result is similar to using two UADP 1.0 chips in a single ASIC package. UADP 1.1 also provides higher aggregate bandwidth and performance of up to 160Gbps (80Gbps per core), as well as some new and updated micro-engines. Some of the new features that UADP 1.1

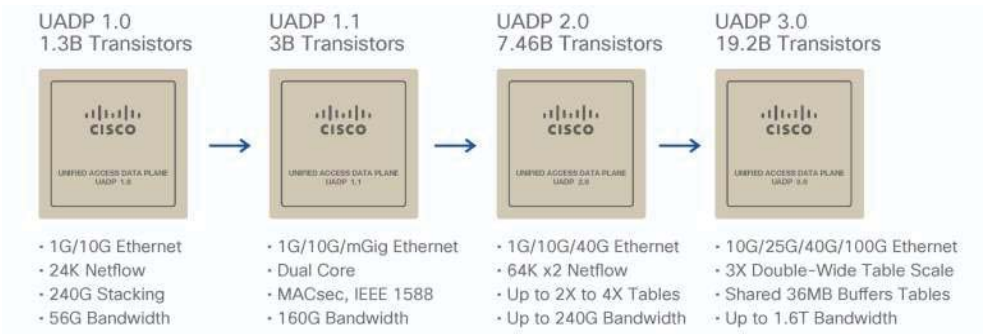
supports include IEEE 1588 timestamps and MACsec 256-bit encryption (AES-256-GCM). The second generation of MultiGigabit and SFP+ versions of Catalyst 3850 and 3650 use UADP 1.1.

UADP 2.0

Catalyst 9000s are built on the next generations of UADP - the UADP 2.0 and 3.0 ASICs.

The UADP 2.0 is a dual-core ASIC (similar to UADP 1.1) with 7.46 billion transistors to provide even higher aggregate bandwidth up to 240Gbps. UADP 2.0 also has larger, more flexible memory tables that can be reprogrammed, giving the option to deploy the same device in multiple network areas, as discussed in Chapter 14 Campus Network Design.

DIAGRAM Comparison of UADP 1.0, 1.1, 2.0, and 3.0



UADP 2.0 ASICs have two variants: UADP 2.0 and UADP 2.0 XL. Both have the same architecture, but the aggregate bandwidth, table scale and overall performance of UADP 2.0 has been optimized for Access layer devices. Catalyst 9300 platforms utilize UADP 2.0.

UADP 2.0 XL has been optimized for modular access and/or distribution layer switches. It has larger memory table sizes (hence the XL designation) with greater aggregate

bandwidth and overall performance to support the port speeds and density of these roles. UADP 2.0 XL also has dual data paths of 720Gbps inter-ASIC connectivity, making it more suitable for platforms where multiple ASICs may be required. The first Catalyst 9500 platforms and the Catalyst 9400 Supervisor-1 and Supervisor-1XL use UADP 2.0 XL.

TABLE UADP 2.0 and 2.0 XL Comparison

	UADP 2.0	UADP 2.0 XL
Total Bandwidth	Up to 160G	Up to 240G
Table Sizes	Standard	XL Tables
TCAM Entries	20K	54K
Buffers	16MB	32MB
Stack Bandwidth	240G	720G
Stack Ring	1	2

UADP 3.0

The need for network speed is never-ending, driven by new wireless speeds, the increasing number of attached devices (IoT) and high-definition video conferencing. New technologies are appearing every day and driving new requirements for network performance and scale.

The UADP 3.0 is a dual-core ASIC with 19.2 billion transistors, to provide an aggregate bandwidth up to 1.6Tbps. UADP 3.0 is the most recent version of UADP, designed to address the challenges brought on by new interface speeds (e.g. 25G and 100G) and new network designs and solutions. A single UADP 3.0 ASIC is capable of 16 ports of 100G line rate.

In addition to increased bandwidth, UADP 3.0 also incorporates several new improvements to make it the ideal ASIC for campus core and distribution. UADP 3.0 has larger shared packet buffers (36MB) to support the interface speed increases. It has

larger double-wide memory table sizes to store both IPv4 (32bit) and IPv6 (128bit) addresses in a single entry. Many other ASICs and previous generations of UADP only support single-width tables, requiring an additional lookup cycle to support IPv6. The first products available with the new UADP 3.0 ASIC are the new 10/25/40/100G Catalyst 9500 platforms.