UfiSpace S9500-22XST

Disaggregated Cell Site Gateway (DCSG) Specification

Revision 1.0

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2 Revision History

Date	Rev	Author	Summary of Change
Jun. 04, 2021	R1.0	Tom Chen	First Draft Release

3 Overview

This document describes the technical specifications of the S9500-22XST disaggregated cell site gateway designed for telecom service applications.

The S9500-22XST provides 1GE, 10GE, 25GE and 100GE high speed Ethernet ports together with hardware support for IEEE 1588v2 and SyncE timing synchronization features. It enables service providers to deliver next-generation technologies such as a 5G mobile Ethernet network, which requires high data bandwidth and very precise timing synchronization.

With temperature-hardened, high-throughput, small form factor, low-power-consumption and redundancy features, the S9500-22XST disaggregated cell site gateway delivers high system reliability, Ethernet switching performance and intelligence to the network edge in a flexible 1RU form factor that helps reduce infrastructure and administrative costs.

Front View

Rear View

4 High-Level Description

This section describes key features, system block diagram and system mechanical outline for S9500-22XST.

4.1 Feature Summary

- 1+1 redundant power supply
  - 200W output
  - -36~72V DC input
  - Field replaceable
- 2+1 redundant fan module
  - 25000 RPM
  - Front to back airflow
  - Field replaceable
- Ethernet I/O ports:
  - 4 x 10/100/1000 Base-T ports
  - 8 x 10GbE SFP+ ports
  - 8 x 25GbE SFP28 ports
  - 2 x 100GbE QSFP28 ports
- Front/Real panel LED indicators:
  - 1 x Power status LED
  - 1 x FAN status LED
  - 1 x System status LED
  - 1 x Synchronization status LED
  - 1 x GNSS\GPS status LED
  - Per port FAN status LED
  - Per port PSU status LED
  - Per port link status LED
- Management interfaces:
  - 1 x GbE OOB management port (CPU)
  - 1 x USB2.0 Type-A general purpose port
  - 1 x RS232 console port in RJ45 form factor
  - 1 x USB console port in Micro USB form factor
  - 1 x Tact switch for system reset/reload default configuration
- Timing Synchronization:
  - 1588V2 and SyncE with T-GM, T-TSC, T-TC, T-OC, T-BC support
  - Input source : GNSS/GPS, E1/T1, ToD, 1PPS and 10MHz
  - Output source : 1PPS and 10MHz

4.2 Component Summary

- PCBA:
  - 1 x Switch board
  - 1 x CPU card
  - 1 x FAN card
  - 1 x PSU card
  - 1 x LED card
- On board key components:
  - Switch Board
    - 1 x MAC Qumran-AX BCM88470

- 4 x 512MB DDR4 SDRAM @ 1200MHz
- 1 x Quad port 1GbE PHY BCM54140
- 1 x Management CPLD 10M04SAU169I7G
- 1 x PCIe/NCSI NIC I210-IT for CPU & BMC
- 1 x SyncE & IEEE 1588 DPLL 82P33831
- 1 x Clock jitter attenuator buffer Si5344D
- 1 x GNSS/GPS module NEO-M8T
- 1 x T1/E1 transceiver 82P2281

■ CPU Card
- 1 x CPU Broadwell-DE D-1519 with quad core @ 1.5GHz
- 1 x 8GB DDR4 SODIMM memory module with ECC support
- 1 x 32GB SATA3 M.2 SSD Memory module

● PSU& FAN:
- 2x 200W slim PSUs with redundancy support
- 3x 4028 FAN tray modules with redundancy support

4.3 Switch Board Functional Block Diagram

S9500-22XST system functional block diagram is shown as below:

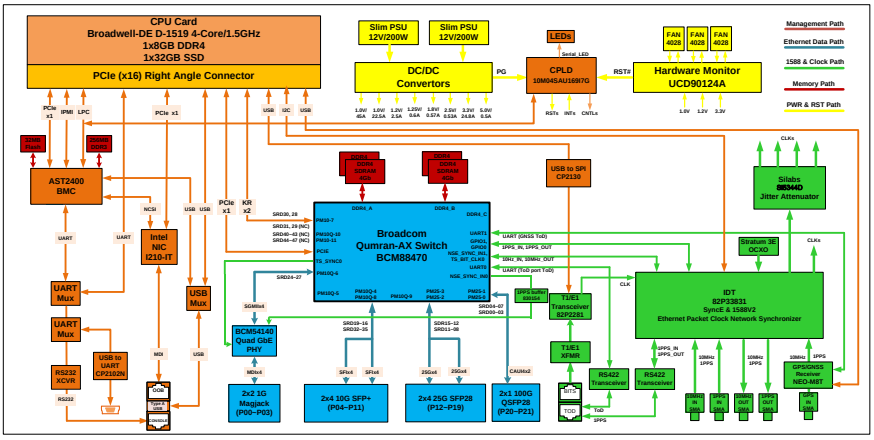

Figure 4-1 Switch Board Block Diagram

S9500-22XST switch main board placement is shown as below, parts highlight in yellow are installed on PCB top side while components in blue are staffed on bottom side:

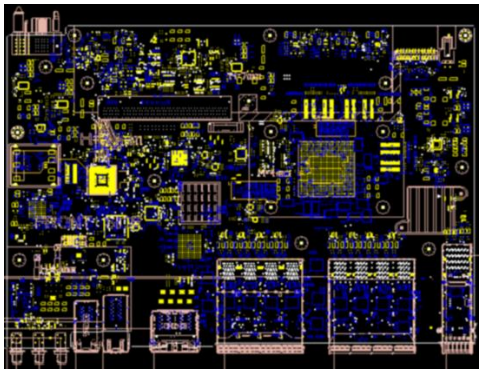

Figure 4-2 Switch Board PCB Layout

Main Board	Inches	Millimeters
Width	12.34	313.5
Depth	8.36	212.23

Table 4-1 Switch Board Dimension

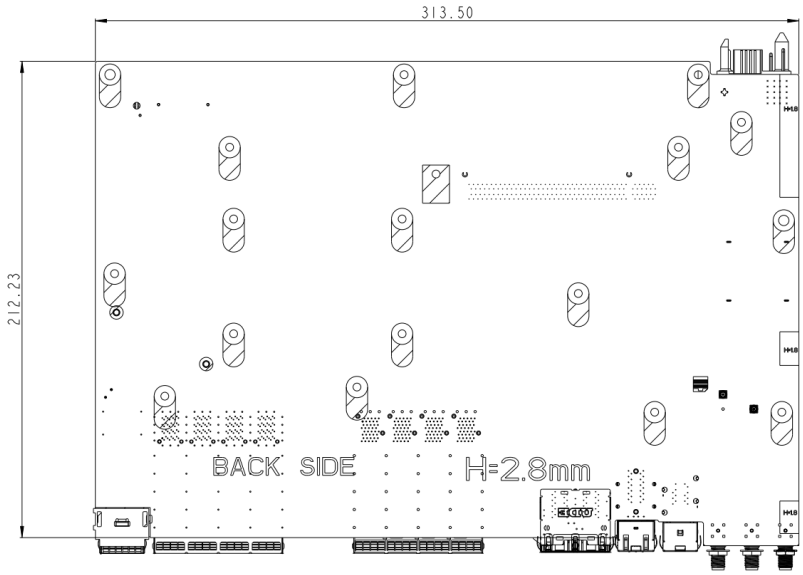

Figure 4-3 Switch Board Dimension

4.4 CPU Card Functional Block Diagram

S9500-22XST CPU card block diagram is shown as below:

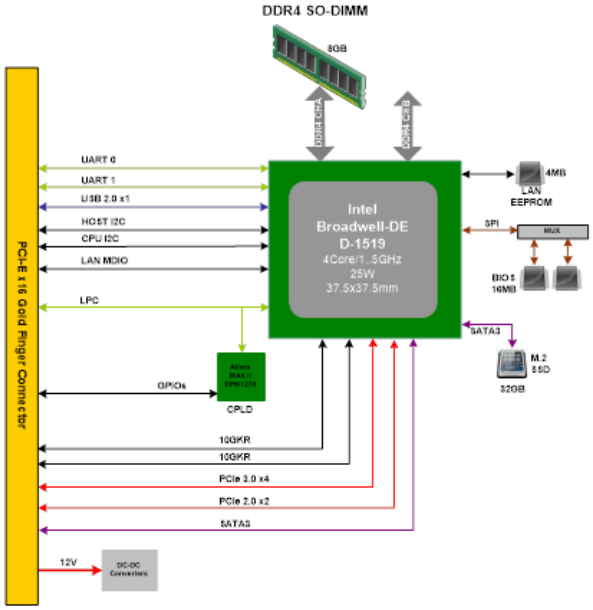

Figure 4-4 CPU Board Functional Block Diagram

S9500-22XST CPU card placement is shown as below:

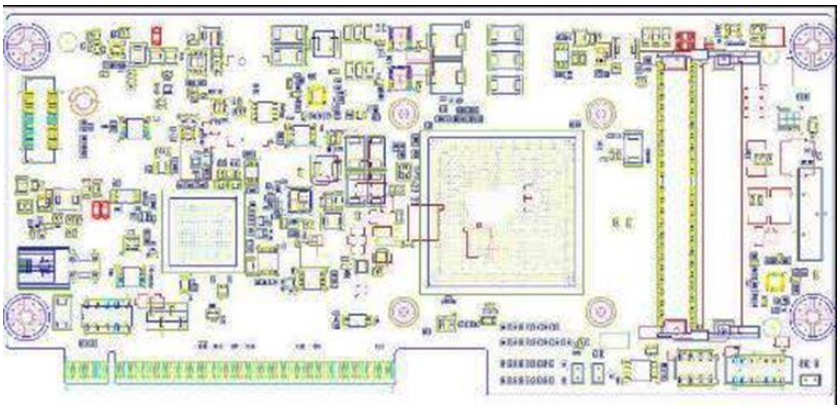

Figure 4-5 CPU Board PCB Layout

Main Board	Inches	Millimeters
Width	3.78	96
Depth	8.27	210

Table 4-2 CPU Board PCB Dimension

4.5 Mechanical Outline

The S9500-22XST chassis is designed to meet cabinets with 19’’ depth. This 1RU system mechanical dimension is: 440mm (W) x 302mm (D) x 43.5mm (H).

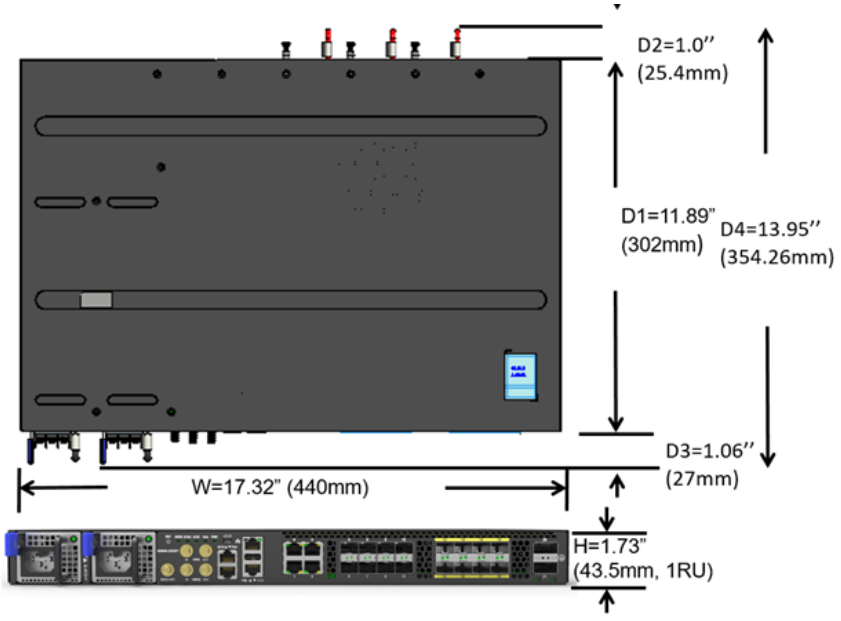

Figure 4-6 S9500-22XST Mechanical Outline

4.6 System Explode Diagram

Below shows the S9500-22XST system explode diagram. The mainboard will be populated inside the base chassis along with the fan control board and air baffle together, which are fixed with screws. Next is the CPU card, which will be installed onto the right angle PCIe connector and fixed with standoffs/screws. The fan and PSU modules will be plugged into fan and PSU slots after chassis top cover is fixed.

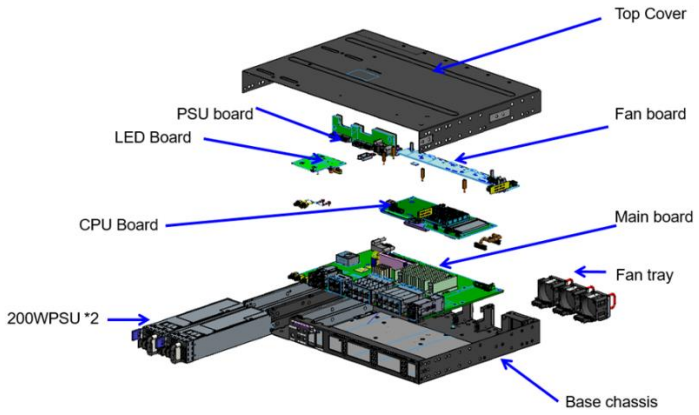

Figure 4-7 S9500-22XST System Explode Diagram

The S9900-22XST system top view without top cover is shown as below :

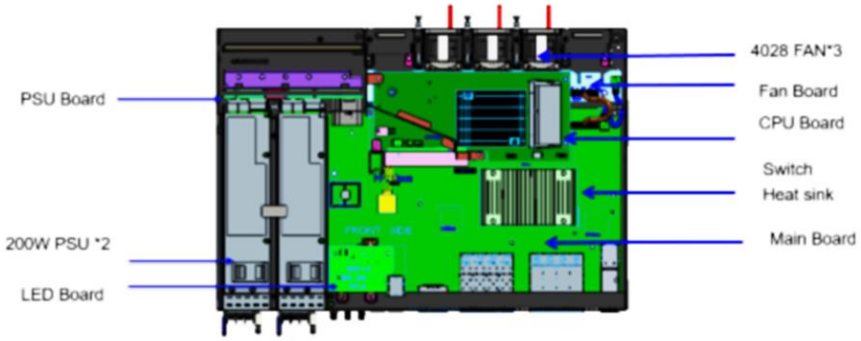

Figure 4-8 S9500-22XST System Top View

5 Hardware Architecture

This section describes key features, system block diagrams and major components used on the S9500-22XST.

5.1 CPU Subsystem

Intel's x86 embedded SoC processor Broadwell-DE D1519 is equipped on S9500-22XST CPU board. The major onboard components and interfaces to switch board is listed as below:

- Intel's Broadwell-DE Processor
  - ✓ Capable of supporting up to 8-core processor
  - ✓ Two DDR4 ECC SO-DIMMs, up to 8GB
  - ✓ Single M.2 22*42mm SSD module up to 32GB
  - ✓ Dual 16MB SPI boot/BIOS flash components
- PCIe x16 gold finger to switch board
  - ✓ Single x4 PCIe Gen3 interface
  - ✓ Single x2 PCIe Gen2 interface
  - ✓ Two 10Gbps Ethernet interfaces
  - ✓ Two UART interfaces
  - ✓ Three USB interfaces
  - ✓ Three I2C interfaces

5.2 BMC Subsystem

The BMC subsystem is designed on the switch board.

5.2.1 BMC Subsystem Block Diagram

In the S9500-22XST, the baseboard management controller (BMC) automatically monitors system's health including temperature, voltage, fan speed, etc.

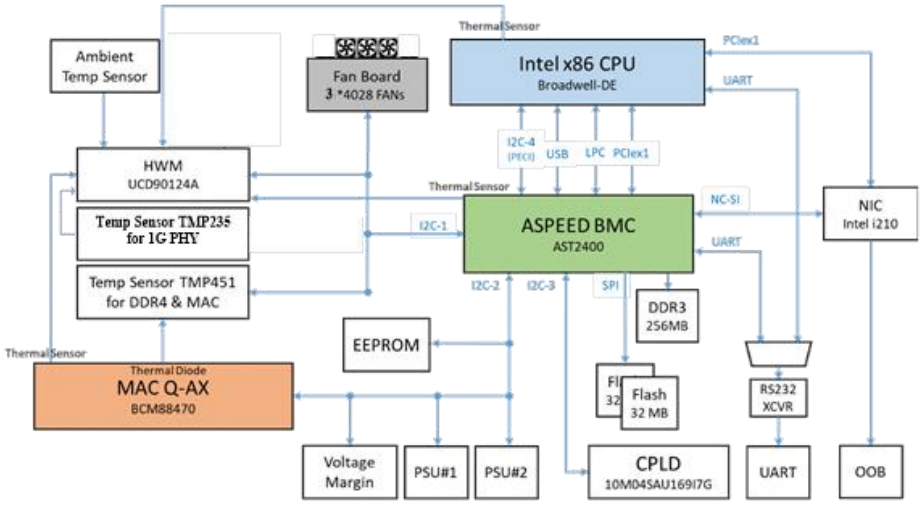

Figure 5-1 S9500-22XST BMC Block Diagram

5.2.2 BMC Chipset Heater Control

S9500-22XST is designed to operate in -40~65°C environment, all components except BMC are -40~85°C operating temperature capable components. There is no industrial rating version for AST2400, it can only operate at 0~70°C. To make this commercial chipset works under -40~0°C ambient temperature, an additional chipset heater is adopted for BMC AST2400.

BMC heater is controlled by HWM UCD90124A. It is powered by standby power rails, it monitors chassis and BMC, chipset heater temperature and controls, after receive BMC heater heating enable signal from CPLD, BMC heater DC/DC power enable & power output circuits, BMC heater DC/DC convertor is turned on if chassis and BMC temperature is lower than -0°C, heater power will be turned off if chassis temperature is higher than 0°C. UCD90124A will assert BMC heating complete indication to CPLD within 5 minutes, otherwise CPLD will turn off heater power after one timeout retry.

After BMC sensor reaches pre-defined temperature, UCD90124A will enable BMC DC/DC power rails and BMC start boot up, heater is being turned on continue to make BMC temperature keep in plus °C environment.

An additional comparator for heater over temperature protection is adopted to prevent heater overheating, when the heater temperature reaches 70’C, this comparator will turn off heater and will be released once the temperature is lower than 70’C.

By default, UCD90124A controls heater power based on ambient, BMC & heater temperature. To make heater power control more flexible, BMC can also control the heater by disabling the control from HWM and controls heater DC/DC convertor output power directly. BMC control heater on/off mechanism is HW ready but not implemented in BMC firmware.

5.2.3 LPC

Low-pin-count interface is an important interface for communication among Broadwell-DE,CPLD and BMC. The OS running in x86 use this interface to communicate with BMC’s IPMI message handler.

5.2.4 USB

AST2400 provides three USB interfaces for different functional objectives. The four USB controllers of AST2400 meet USB specification revision 2.0 and 1.1 and also compliant with EHCI and UHCI specification.

5.2.5 10/100/1000 Mbps Fast Ethernet MAC

AST2400 integrates two MACs compliant with IEEE802.3 and IEEE802.3z specification. And the transfer rate is up to 10/100/1000M bps. BMC share the same management port in front-panel by connecting NC-SI interface to Intel I210 controller’s NC-SI. Administrator can disable NC-SI if need.

In system shutdown mode, BMC works and can be accessed by RJ45 console port only, OOB port connection is lost in this case.

5.2.6 UART

AST2400 supports up to five sets UART IO interface with full flow control pins, and 1 set with Tx/Rx only for BMC console. The administrator can switch x86 and BMC console easily and choose to connect to front panel console RJ45 or micro-USB connector. Also, disabling BMC console is allowed by command.

5.2.7 I2C

AST2400 integrates up to 14 sets of multi-function I2C/SMBus bus controllers. In the S9500-22XST, BMC use 4x I2C interfaces to collect voltage, temperature, fan speed, FRU, and manufacture information. BMC continues to monitor system's health after it boots up. And BMC should record and handle the event if sensor's value is over the reasonable range.

5.2.8 GPIO

AST2400 Integrates one set of Parallel GPIO Controller with maximum 216 control pins, which are 28 sets, to provide general-purpose input/output functions. All functional parallel GPIOs of S9500-22XST in different group are listed as below, net names ended with '_N' means this signal is active low, otherwise it's active high or it's a mux select pin.

5.2.9 Watchdog Timer/Keep Alive

AST2400 has two build-in sets of 32-bit WDT modules. In S9500-22XST, we use WDT #1 to keep alive with x86 system. The OS running in x86 can enable watchdog timer, set timeout counter, and timeout behavior by using IPMI command. If OS was halted, BMC would reset x86 system after watchdog timer expired. And BMC will implement WDT #2 internally to monitor the status itself. If BMC was halted, BMC would reset itself without affecting x86 system.

5.2.10 SPI Boot Flash

There are two 32MB (256Mb) SPI boot flashes for AST2400 U-boot, OS and application software storage. In manufacture, both of these two components store the same BMC image. By default, system boots from primary SPI flash (CS0#). It will swap to backup SPI flash (CS#1) when system boot up fail from primary flash.

Dual boot flash design is also useful for BMC firmware upgrade, in the case of the flash is crash during firmware upgrade, it will be recovered by the original image stored in the backup flash.

5.2.11 DDR3 SDRAM

The memory controller unit integrated in AST2400supports x16 data bus width DDR3 SDRAM. One 128Mb x16 DDR3 SDRAM is installed for AST2400.

5.3 Switching Subsystem

This section details switch board component features/functionalities summary and hardware system design.

5.3.1 MAC Component -- BCM88470

The Broadcom® BCM88470 AX series, based on the Dune switching architecture, is a new member of the centralized switching solutions family from the StrataDNX™ scalable-switching product line.

The BCM88470 series of devices processes up to 300Gbps traffic at Layer 2 through Layer 4, with integrated deep-buffer traffic management capabilities and1GbE, 2.5GbE, 10GbE, 25GbE, 40GbE, 50GbE, and 100GbE MAC network interfaces, supporting various port rate combinations.

The BCM88470 packet classification engine is flexible and microcode programmable, with built-in support for data center, carrier access/aggregation, metro Ethernet, MBH, uWave access, and transport applications. The large on-chip classification databases can be further extended off-chip using an external KBP device from Broadcom.

The BCM88470 traffic manager integrates deep packet buffers with state-of-the-art hierarchical QoS, transmission scheduling, and flow control. These advanced scheduling and queuing schemes natively support all the latest innovations in data center networking, such as PFC, ETS, QCN, delay-based ECN, and overlay networks, allowing per-customer/per-service scheduling in carrier access/aggregation and aggregation switches.

Industry grade BCM88470IFSBG is selected on S9500-22XST project.

5.3.1.1 Features Summary

Jericho2 has 6 MIIM interfaces MIIM[6:0]. The S9500-22XST connects to OP2(BCM16000) by MIIM6.

- High performance
  - 300 Gb/s full-duplex integrated traffic manager and packet processor.
  - 300 Mpps processing rate.
- Flexible network interface
  - Total of 48 SerDes.
  - Pool of 16 SerDes at up to 25.78125 Gb/s each: flexible assignment to protocols.
  - Supported protocol blocks for the 16x 25G SerDes:
    - ✓ 16 × GbE, over SGMII/1000Base-X (1000Base-X may use SFI)
    - ✓ 16 × 10GbE, over 10GBase-R/XAUI (10GBase-R may use SFI/XFI and KR).
    - ✓ 8 × 40GbE, over XLAUI-2/XLAUI.
    - ✓ 4 × 100GbE, over CAUI-4 4-lane.
  - Pool of 32 SerDes at up to 12.5 Gb/s each; flexible assignment to protocols.
  - Supported protocol blocks for the 32x12.5G SerDes:
    - ✓ 96 x GbE, over QSGMII (only 24 SerDes out of the 32 supports QSGMII).
    - ✓ 32 x GbE, over SGMII/1000Base-R (1000Base-X may use SFI).
    - ✓ 32 x 10GbE, over 10GBase-R/XAUI/RXAUI (10GBase-R may use SFI/XFI and KR).
    - ✓ 8 x 40GbE, over XLAUI 4-lane.
  - Packets lengths supported in the range 64B–10KB.

- Traffic Manager
  - 32k programmable wire-rate queues.
  - Deep buffering: 24 Gb DRAM-based.
  - Congestion management:
    - ✓ Hierarchical WRED and tail drop policies.
    - ✓ Congestion notification: CNM generation and CNM reception (proxy).
    - ✓ Flow Control generation: fully programmable, in-band and out-of-band.
    - ✓ Flow Control reception-any level: interface, port, class, flow, traffic type-in-band& out-of-band.
    - ✓ Priority Flow Control (PFC): eight levels.
    - ✓ Congestion tracking statistics.
  - Hierarchical scheduling and shaping: fully programmable to any depth.
  - MEF, DSL-FORUM TR-059-compliant scheduling and shaping.
  - Ingress shaping: efficient with pointer manipulation only.
- Packet processor:
  - Metro Ethernet, enterprise, and data center.
  - Large, on-chip databases and optional off-chip database expansions.
  - Full-featured: bridging, routing, MPLS. VPLS, L2VPNs, L3VPNs, OAM, and so on.
  - Microcode controlled hardware: flexible and future-proof.
- Multicast: pointer-based ingress and/or egress multicast replication.
- Statistics interface: expandable, off-chip statistics gathering:
  - SerDes-based: The SerDes used for the statistics interface shared with NIF SerDes.
  - Efficient packet-based protocol: simplifies connectivity to FPGAs.
- OTN and TDM support:
  - Low delay/jitter for 64B–256B TDM packets.
  - TDM packets bypass ingress/egress traffic managers.
- In-band management.
- PCIe x1 lanes Gen 2 host interface with DMA.
- The BCM88470 device supports back-to back connectivity to one peer BCM88470 device over 25G lanes.

5.3.1.2 Network Port Design

5.3.1.2.1 Port Assignments

Figure 5-2 Physical Port Assignment

The table below shows the network ports numbering and speed.

Function	Port#	Speed	Notes
RJ45 Ports	P0	10M/100M/1G	1GBASE MT-RJ
	P1	10M/100M/1G	1GBASE MT-RJ

	P2	10M/100M/1G	1GBASE MT-RJ
	P3	10M/100M/1G	1GBASE MT-RJ
SFP+ Ports	P4	100M/1G/10G	10GBASE ZR SFP+
	P5	100M/1G/10G	10GBASE ZR SFP+
	P6	100M/1G/10G	10GBASE ZR SFP+
	P7	100M/1G/10G	10GBASE ZR SFP+
	P8	100M/1G/10G	10GBASE ZR SFP+
	P9	100M/1G/10G	10GBASE ZR SFP+
	P10	100M/1G/10G	10GBASE ZR SFP+
	P11	100M/1G/10G	10GBASE ZR SFP+
SFP28 Ports	P12	1G/10G/25G	25GBASE LR SFP28
	P13	1G/10G/25G	25GBASE LR SFP28
	P14	1G/10G/25G	25GBASE LR SFP28
	P15	1G/10G/25G	25GBASE LR SFP28
	P16	1G/10G/25G	25GBASE LR SFP28
	P17	1G/10G/25G	25GBASE LR SFP28
	P18	1G/10G/25G	25GBASE LR SFP28
	P19	1G/10G/25G	25GBASE LR SFP28
QSFP28 Ports	P20	40G/100G	100GBASE LR4 QSFP28
	P21	40G/100G	100GBASE LR4 QSFP28

Table 5-1 Network Port Connection

5.3.1.3 Port Mapping

Front Port		PHY_BCM54140			MAC_BCM88470								PHY_BCM54140			Front Port	
		Line Side		System Side	System Side TX					System Side RX				System Side		Line Side		
Speed	Port Ordering	Physical Port	PHY ADDR	RX_Lane (SGMII)	TX_Lane (SGMII)	TX PN swap (Y/N)	TX Lane Swap (Y/N)	SRD Number	PM	SRD Number	RX Lane Swap (Y/N)	RX PN Swap (Y/N)	RX_Lane (SGMII)	TX_Lane (SGMII)	PHY ADDR	Physical Port	Port Ordering	Speed
1G	1	P0	0x00000	0	1	Y	Y	SRD25	PM10Q-6	SRD24	N	N	0	0	0x00000	P0	1	1G
1G	0	P2	0x00001	1	2	Y	Y	SRD26		SRD26	Y	N	2	1	0x00001	P2	0	1G
1G	3	P1	0x00010	2	3	Y	Y	SRD27		SRD27	Y	N	3	2	0x00010	P1	3	1G
1G	2	P3	0x00011	3	0	Y	Y	SRD24		SRD25	Y	N	1	3	0x00011	P3	2	1G

Front Port_TX				MAC_BCM88470								Front Port_RX			
				System Side_TX					System Side_RX						
Speed	Port Ordering	Physical Port	TX_Lane	TX_Lane (NIF)	TX P/N Swap (Y/N)	TX Lane Swap (Y/N)	SRD Number	PM	SRD Number	RX Lane Swap (Y/N)	RX P/N Swap (Y/N)	RX_Lane (NIF)	RX_Lane	Physical Port	Port Ordering	Speed
10G	4	8	3	3	N	N	SRD19	PM10Q-4	SRD19	N	N	3	3	8	4	10G
10G	5	9	2	2	Y	N	SRD18		SRD18	N	N	2	2	9	5	10G
10G	6	10	1	1	N	N	SRD17		SRD17	N	N	1	1	10	6	10G
10G	7	11	0	0	Y	N	SRD16		SRD16	N	N	0	0	11	7	10G
10G	8	12	0	0	N	N	SRD32	PM10Q-8	SRD32	N	N	0	0	12	8	10G
10G	9	13	1	1	Y	N	SRD33		SRD33	N	N	1	1	13	9	10G
10G	10	14	2	2	N	N	SRD34		SRD34	N	N	2	2	14	10	10G
10G	11	15	3	3	N	N	SRD35		SRD35	N	N	3	3	15	11	10G
25G	12	20	3	3	N	N	SRD15	PM25-3	SRD14	Y	Y	2	3	20	12	25G
25G	13	21	2	2	N	N	SRD14		SRD15	Y	Y	3	2	21	13	25G
25G	14	22	1	1	N	N	SRD13		SRD13	N	N	1	1	22	14	25G
25G	15	23	0	0	N	N	SRD12		SRD12	N	Y	0	0	23	15	25G
25G	16	24	3	3	N	N	SRD11	PM25-2	SRD11	N	N	3	3	24	16	25G
25G	17	25	2	2	N	N	SRD10		SRD10	N	Y	2	2	25	17	25G
25G	18	26	1	1	N	N	SRD9		SRD9	N	N	1	1	26	18	25G
25G	19	27	0	0	N	N	SRD8		SRD8	N	Y	0	0	27	19	25G
100G	20	Z0	0	3	N	Y	SRD3	PM25-0	SRD3	Y	N	3	0	Z0	20	100G
			1	1	N	N	SRD1		SRD1	N	N	1	1			
			2	2	N	N	SRD2		SRD0	Y	N	0	2			
			3	0	N	Y	SRD0		SRD2	Y	N	2	3			
100G	21	Z1	0	3	N	Y	SRD7	PM25-1	SRD4	N	N	0	0	Z1	21	100G
			1	1	N	N	SRD5		SRD7	Y	N	3	1			
			2	2	N	N	SRD6		SRD5	Y	N	1	2			
			3	0	N	Y	SRD4		SRD6	Y	N	2	3			

Table 5-2 Network Port Mapping

5.4 Timing Subsystem

The timing subsystem is designed on the switch board

5.4.1 Timing Subsystem Block Diagram

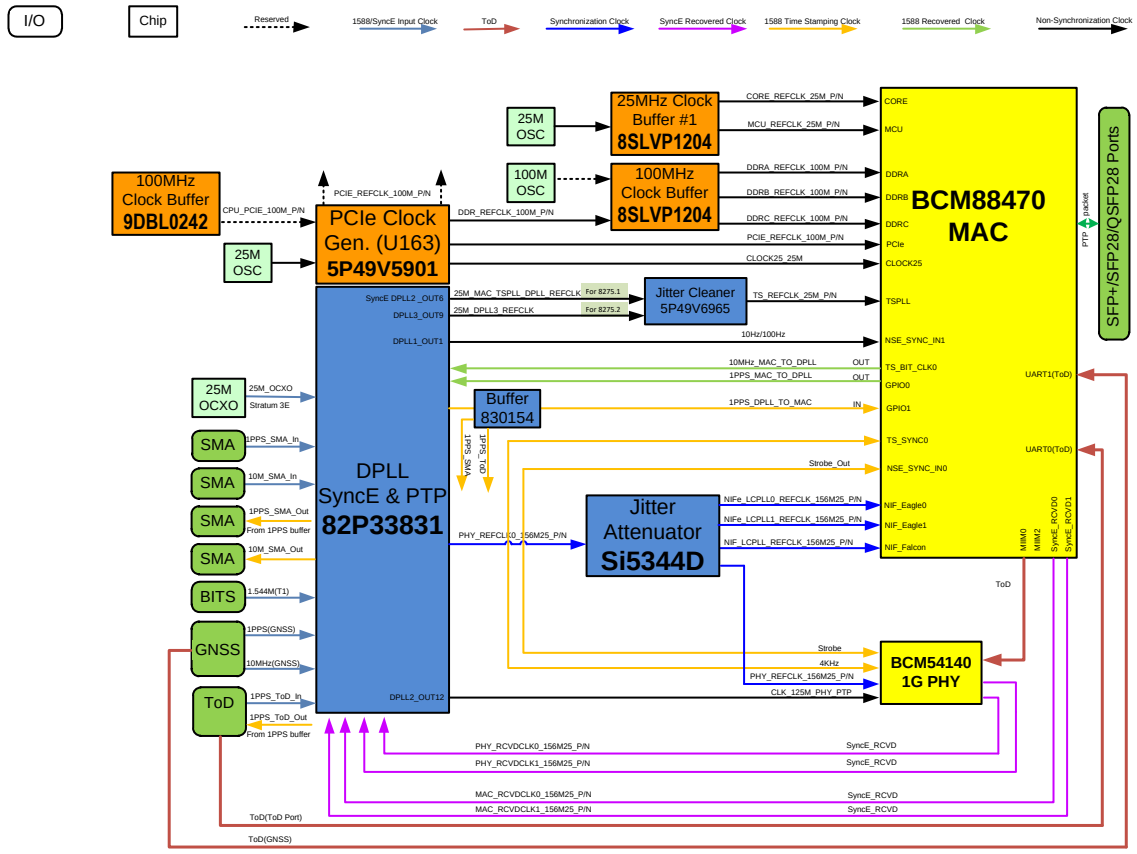

Figure 5-3 S9500-22XST Switch Board Clock and Timing Block Diagram

5.4.2 Timing Subsystem Features

- IEEE-1588v2(PTP) & SyncE.
- Multiple external timing interfaces are connected to IDT's DPLL.
    - GNSS input port (SMA)
    - 1PPS input port (SMA)
    - 1PPS output port (SMA)
    - 10MHz input port (SMA)
    - 10MHz output port (SMA)
    - Time of day (TOD) input port (RJ45)

- Building-Integrated Timing System (BITS) input port (RJ45)

5.5 Fan, LED, and PSU Cards

5.5.1 FAN, LED, and PSU Card Placements

Fan Card

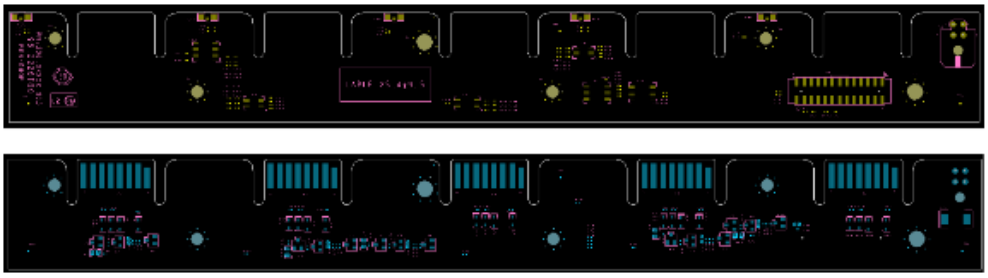

Figure 5-4 Fan Card PCB Placement

LED Card

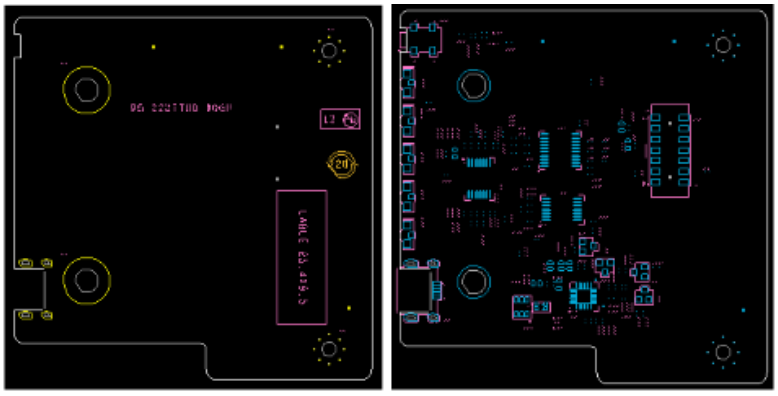

Figure 5-5 LED Card PCB Placement

PSU Card

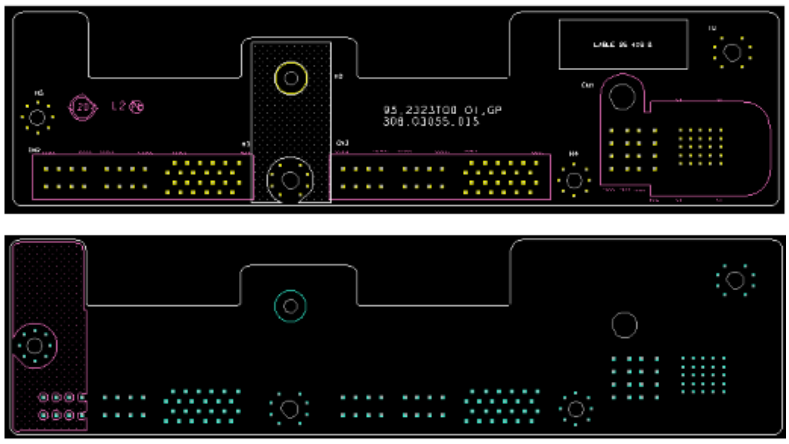

Figure 5-6 PSU Card PCB Placement

5.5.2 FAN, LED and PSU Card Dimensions

The PSU board is a passive board that bridges 12V power and control signals to the PSU.

Fan Card

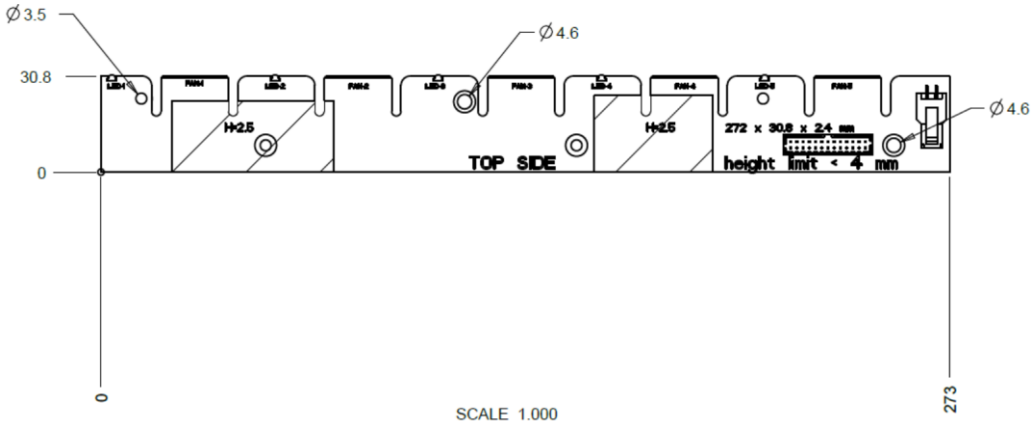

Figure 5-7 Fan Card PCB Dimension

LED Card

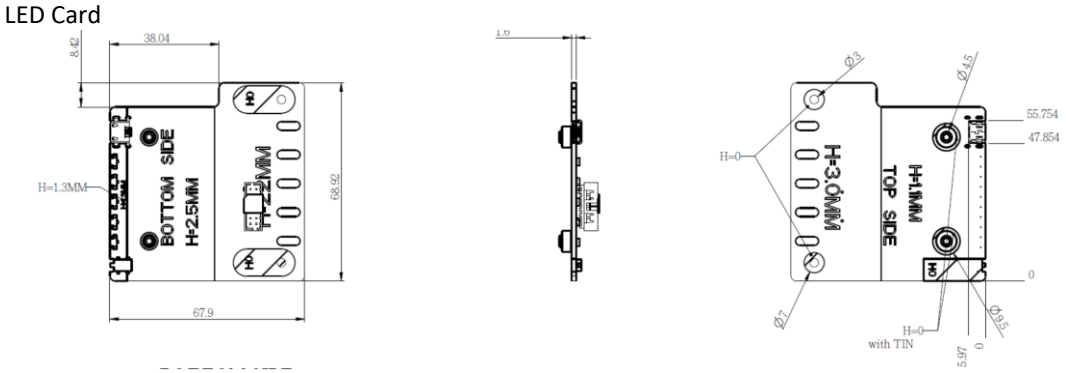

Figure 5-8 LED Card PCB Dimension

PSU Card

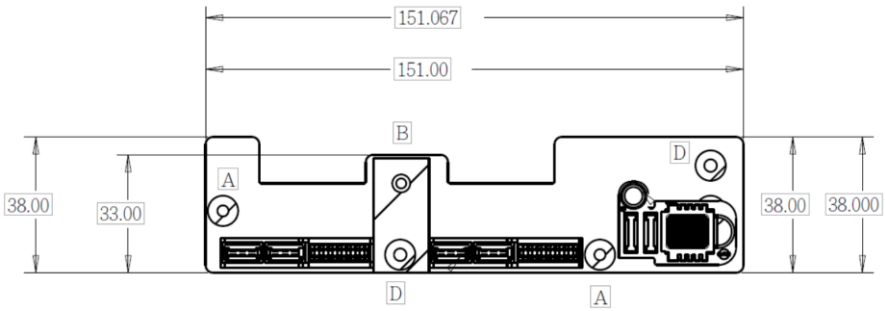

Figure 5-9 PSU Card PCB Dimension

5.6 Front Panel Design

The S9500-22XST front panel IO ports and LED include the functionalities below:

- System status LED
  - ✓ Power status LED
  - ✓ FAN status LED
  - ✓ GNSS status LED
  - ✓ Synchronization status LED
- Ethernet ports LED
  - ✓ OOB copper ports LED
  - ✓ Data traffic fiber ports LED
- Management ports (Share between CPU and BMC)
  - ✓ 1x OOB port
  - ✓ 1x Type A USB port
  - ✓ 1x console port in RJ45
  - ✓ 1x console port in Micro-USB
- Ethernet data ports
  - ✓ 4x 1G Copper ports
  - ✓ 8x 25G SFP28 ports
  - ✓ 8x 10G SFP+ ports
  - ✓ 2x 100G QSFP28 ports
- Timing sychronization ports
  - ✓ 1x GNSS port with SMA connector
  - ✓ 1x T1/E1 port with RJ45 form factor
  - ✓ 1x ToD port with RJ45 form factor
  - ✓ 4x SMA ports with 1PPS and 10MHz ref. clock input/output

The S9500-22XST rear panel design:

- Fan module
- Fan status LED

Detailed IO arrangement is shown as below:

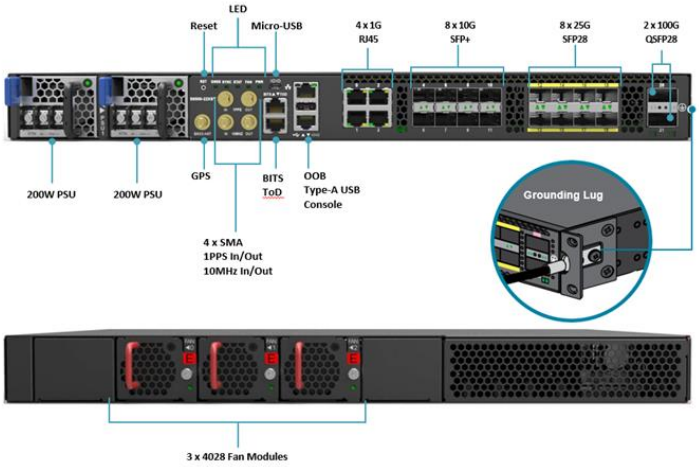

Figure 5-10 Front Panel IO Arrangement

5.6.1 System LED Indicators

The front panel system status LED are placed on LED card.

LED Function/State	Meaning	Comment
PWR (Green/Yellow):		
OFF	No power or in shutdown mode.	
Solid Green	System power good & BMC heating done	
Blinking Green	System power good & BMC is heating	
Solid Yellow	System power good but BMC heating fail	
Blinking Yellow	System power fail	
FAN (Green/Yellow):		
OFF	Reserved	
Solid Green	All FAN modules work well	
Blinking Green	Reserved	
Solid Yellow	Reserved	
Blinking Yellow	One or more FAN module(s) fail or no FAN module present	
STAT (Green/Yellow):		
OFF	System no boot	
Solid Green	System boot complete	
Blinking Green	System is booting	
Solid Yellow	Reserved	
Blinking Yellow	Reserved	
GNSS (Green/Yellow):		
OFF	GNSS is not configured.	
Solid Green	GNSS is in normal state. Self-survey is complete.	
Blinking Green	GNSS is in learning state. Self-survey is not completed.	
Solid Yellow	Power up. GNSS is not tracking any satellite.	
Blinking Yellow	GNSS antenna is short to ground.	
SYNC (Green/Yellow):		
OFF	System timing synchronization is disabled or in free-run mode.	
Solid Green	System timing core is synchronized to external timing source (ex: GNSS, 1PPS, PTP, BITS, etc)	
Blinking Green	System is synchronized in SyncE mode.	
Solid Yellow	System timing core is in acquiring state or holdover mode.	
Blinking Yellow	System timing synchronization fail.	

PSU LED Function/State	Meaning
OFF	No DC power to all PSUs
Flashing Red	No DC power to this PSU
Flashing Green	DC present, only standby output on. Poor contact
Green	PSU DC output ON and OK
Red	PSU failure.
Flashing between Green and Red	Warning. Working condition not satisfied. Please check the voltage, electric current, and temperature.

Fan LED Function/State	Meaning
OFF	Main board 3.3V power fail or Fan is not present.
Solid Green	Fan is present and interrupt de-assert
Blinking Green	N/A
Solid Yellow	N/A
Blinking Yellow	Fan is present but interrupt assert.

Table 5-3 System LED Description

For RJ45, SFP+, SFP28 and QSFP28 ports controlled by serial LED interface of MAC.

LED Function/State	Meaning	Comment
RJ45 (port 0-3) (Green/Yellow):		
OFF	No link on the RJ45 port	
Solid Green	RJ45 port link at 1G mode	
Blinking Green	RJ45 port is transmitting at 1G mode	
Solid Yellow	RJ45 port link at 10M/100M mode	
Blinking Yellow	RJ45 port is transmitting at 10M/100M mode	
SFP+ (port 4-11) (Green/Yellow):		
OFF	No link on the SFP+ port	
Solid Green	SFP+ port link at 10G mode	
Blinking Green	SFP+ port is transmitting at 10G mode	
Solid Yellow	SFP+ port link at 1G/100M mode	
Blinking Yellow	SFP+ port is transmitting at 1G/100M mode	
SFP28 (port 12-19) (Green/Yellow):		
OFF	No link on the SFP28 port	
Solid Green	SFP28 port link at 25G mode	
Blinking Green	SFP28 port is transmitting at 25G mode	
Solid Yellow	SFP28 port link at 10G/1G mode	
Blinking Yellow	SFP28 port is transmitting at 10G/1G mode	
QSFP28 (port 20-21) (Green/Yellow):		
OFF	No link on the QSFP28 port	

Solid Green	QSFP28 port link at 100G/25G mode	
Blinking Green	QSFP28 port is transmitting at 100G/25G mode	
Solid Yellow	QSFP28 port link at 40G/10G mode	
Blinking Yellow	QSFP28 port is transmitting at 40G/10G mode	
OOB port (Green/Yellow):		
OFF	No link on the OOB port	
Solid Green	OOB port link at 1G mode	
Blinking Green	OOB port is transmitting at 1G mode	
Solid Yellow	OOB port link at 10M/100M mode	
Blinking Yellow	OOB port is transmitting at 10M/100M mode	

Table 5-4 Ethernet Ports LED Description

5.6.2 OOB Ports

The S9500-22XST includes 1standard GE RJ45 port for out of band (OOB) management, shared between CPU and BMC. It supports the IEEE 802.3 specification for 10/100/1000Mbps operation.

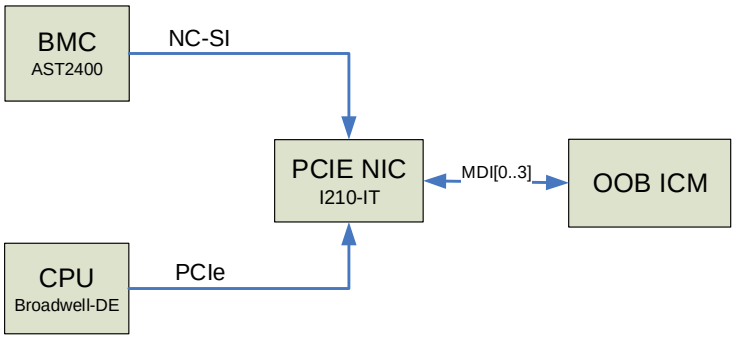

Figure 5-11 CPU OOB Interface Diagram

5.6.3 Console Port

Two console ports are available for the S9500-22XST system access, RS232 and Micro USB console. Both of them can be used for CPU or BMC access. The pin definition of the RS232 console port is shown as below.Pin3 is the TX signal from internal processor to external RS232 interface, and Pin6 is the RX signal from external RS232 interface to internal processor. The bound rate is 115200 by default.

PIN #	Definition	Direction	Note
1	NC		
2	NC		
3	UART_TXD	Out	Console TX
4	GND		

5	GND		
6	UART_RXD	In	Console RX
7	GND		
8	GND		

Table 5-5 Pin Definition of RJ45 Console Connector

5.6.4 USB 2.0 Port

The S9500-22XST integrates a USB 2.0 host controller that supports a single port operating at high speed (HS) at 480 Mbps (USB 2.0).

USB 5V power will be enabled during system initialization, software should de-assert 'PWR_EN' by pulling this pin low once over current event (USB device consumes >0.5A current more than 20mS) is received. 'PWR_EN' need set as 'HIGH' to re-enable USB port.

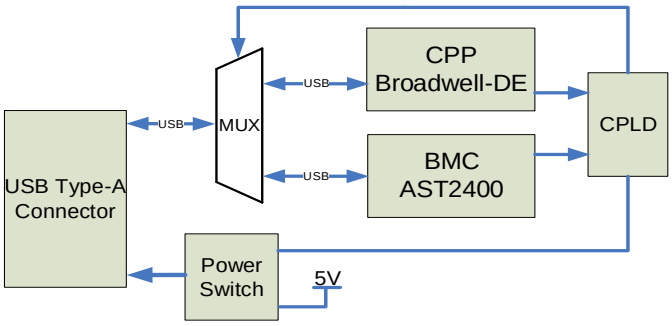

Figure 5-12 USB Interface Diagram

5.6.5 Network Synchronization Ports

- 1x GNSS port with SMA antenna interface
- 1x BITS(T1/E1) port with RJ45 form factor (RJ48 cable)
- 1x ToD port with RJ45 form factor
- 4x SMA ports with 1PPS and 10MHz ref. clock input/output

5.7 Power Consumption

System consumes the maximum power @ 65°C with full traffic loading & all FAN runs at max. 25000RPM. The actual system power consumption will be calculated based on Beta verification data.

Per system power estimation data, the switch board power consumption is around 110W with below configuration: timing interface & BMC works normally, 4x port RJ45 loopback with 0.3W power, 8x port SFP+ loopbacks with 1.5W power, 8x port SFP28 loopback with 1.5W power, 2x port QSFP28 loopback with 5W, 2x DDR4 SDRAM packet buffer enabled, MAC runs at 300Gpbs traffic switching/forwarding, 3x FAN modules runs at 25000RPM.

Measurement of existing Broadwell-DE CPU (4-core/2.2GHz) with 8GB SODIMM and 32GB SSD is 60W max.

System total input power consumption measured by power meter is 170W.

To consider AC PSU efficiency 90% overall system power requirement will be 170 / 0.9 = 189W.

6 Field Replaceable Components

6.1 Fan Module

New developed FAN tray with 40x40x28mm FAN is adopted on S9500-22XST system to meet chassis depth requirement.

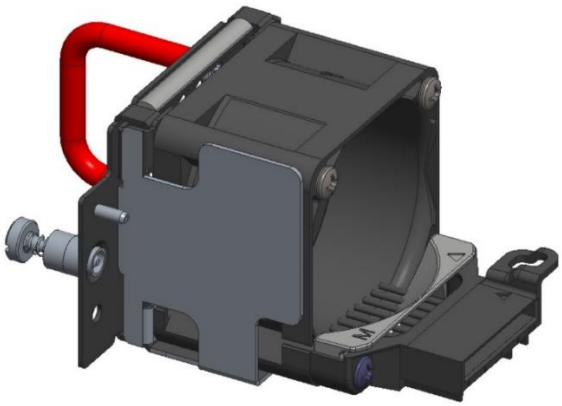

Figure 6-1 4028 FAN Module

6.1.1 Electrical Specifications

Rated voltage	12 VDC
Rated current	900mA, 1035mA, max.
Rated power consumption	10.8W, 12.42W, max.
Operating voltage range	10.2~13.2 VDC
Starting voltage	10.2 VDC (25 degC)
Operating temperature	-40~70 degC
Rated speed	25000 RPM+/-10% at rated voltage
Air flow	31.3CFM, 27.6 CFM min.
Static pressure	2.81 Inch-H2O, 1.96 Inch-H2O min.
Acoustic noise	62.0 dB(A), 69.5 dB(A) max.

Table 6-1 FAN Tray Characteristics

6.1.2 Fan Module Pinout

Molex 46856-0003 connector is assembled in FAN tray and mated with FAN card gold finger. Following Table 5-2 shows S9500-22XST FAN tray interface pinout.

Pin #	Pin Definition	I/O	Function Description	FAN Tray Connector Connection	FAN Connection
1	+12V	-	FAN 12V power	To inlet, outlet FAN +	Out, +
2	GND	-	FAN GND	To outlet FAN -	Out, -
3	FAN_PRSNT_N	O	FAN module presence signal sent by FAN	Jump to Pin2	PIN 2
4	FAN_PWM_OUTLET	I	Outlet FAN speed PWM control signal from HWM	To outlet FAN PWM	Out, PWM
5	FAN_TACH_OUTLET	O	FAN speed tachometer sent by outlet FAN	From outlet FAN tachometer	Out, 3rd
6					
7					
8					

Table 6-2 Connector Pin Definition of FAN Tray

6.2 Power Supply

The S9500-22XST adopts 200W hot swappable power supply units made by 3Y. The PSU modules supports: 1) 220Vac input to +12 Vdc output AC/DC PSU ; 2) -48 V to +12Vdc output DC/DC PSU.

6.2.1 Physical Size

The physical size of the power supply enclosure is intended to accommodate the power range of up to 200W. The physical size is 40.2mm x 50.5mm x 211mm (height x width x length). The Gold finger height was adjusted to 5mm.

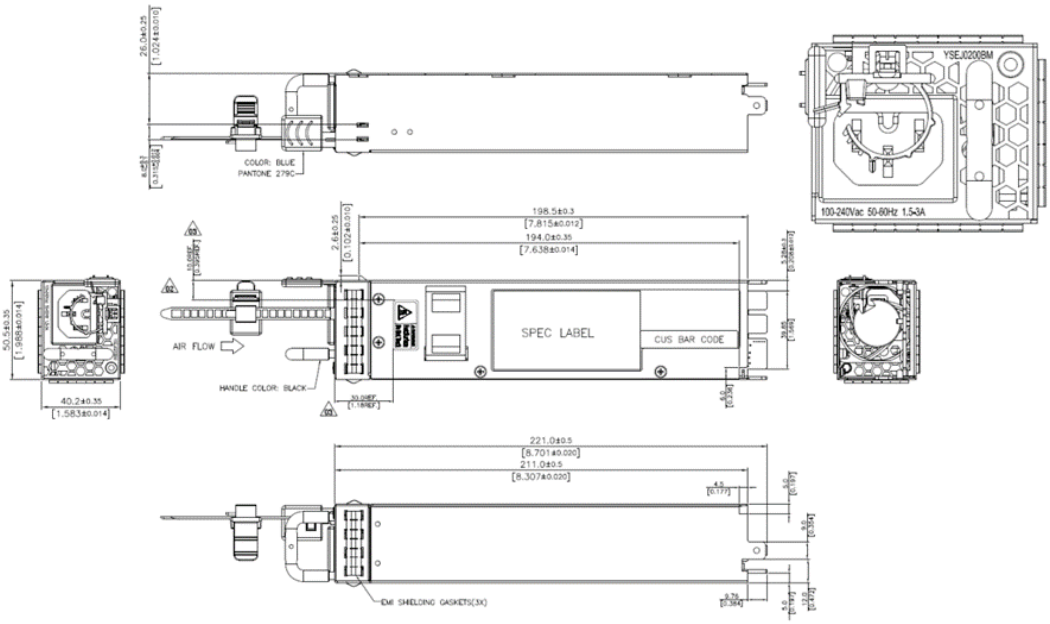

Figure 6-2 200W AC/DC Power Supply Dimension

Figure 6-3 System with 200W AC/DC Power Supply

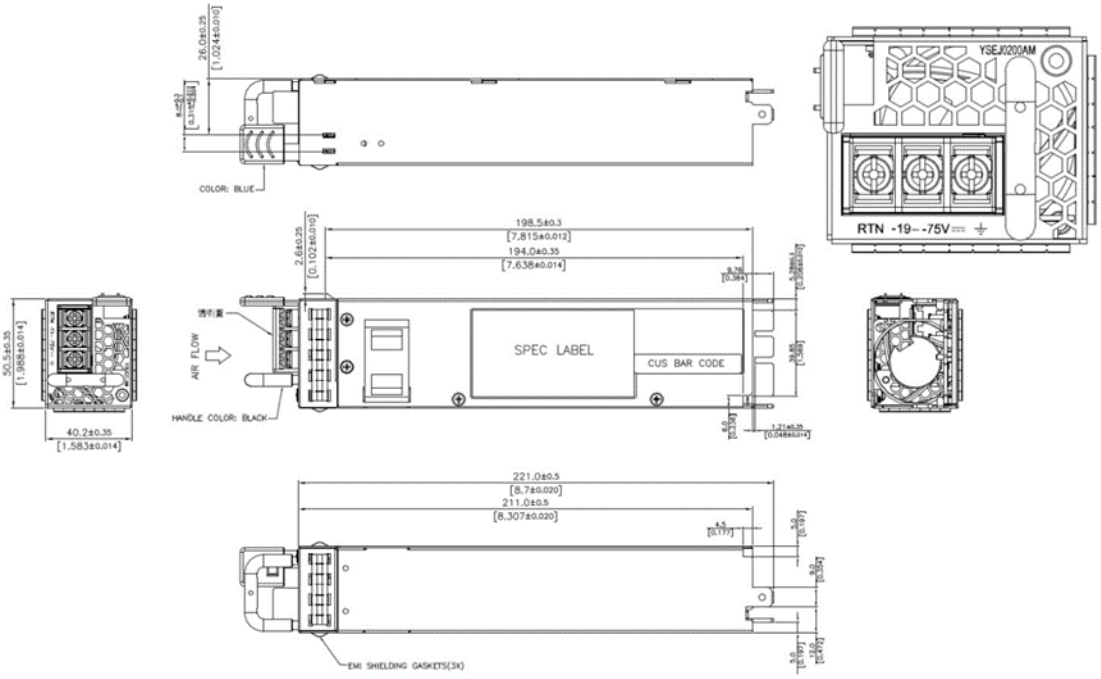

Figure 6-4 200W DC/DC Power Supply Dimension

Figure 6-5 System with 200W DC/DC Power Supply

6.2.2 Electrical Specifications

The detailed electrical specifications of AC/DC PSU are shown as below:

INPUT SPECIFICATIONS	
Input Voltage Range	90 ~ 264 Vac
Input Frequency	47 ~ 63 HZ
Input Current	3A
Inrush Current	60A max.
OUTPUT SPECIFICATIONS	
Output Voltage (Volts)	+12V
Output Current (Amps)	16A(+12V)
Max Power (Watt)	–40°C to 65°C 200W
Output Voltage (Volts)	+5VSB
Output Current (Amps)	3A (+5VSB)
Efficiency	>88% @20% load, >92 @50% load, >88% @100% load
Ripple P-P (mV) (max.)	+12V:120, +5VSB:50
Total Regulation	±5%
GENERAL SPECIFICATIONS	

Hold-up Time (min.)	16mS
Over Voltage Protection	Latch off
Over Current & Short Circuit Protection	Auto Recovery
Over Temperature Protection	Auto Recovery
FAN Failure Protection	Auto Recovery
Hot Swap	Yes, 1+1 redundant
Load Sharing	Yes
Hi-pot	1500VAC
ENVIRONMENTAL SPECIFICATIONS	
Operating Temperature Range	–40°C to 65°C
Storage Temperature Range	–40°C to +70°C
Humidity, Non-Condensing	0 to 95% RH
EMI	Meets FCC/CISPR 22 Class A(under 6dB) Specification

Table 6-3 AC/DC Power Supply Specification

The detailed electrical specifications of Neg48 DC/DC PSU are shown as below:

INPUT SPECIFICATIONS	
Input Voltage Range	-36 ~ -75VDC
Input Current	10A max
Inrush Current	60A max.
OUTPUT SPECIFICATIONS	
Output Voltage (Volts)	+12V
Output Current (Amps)	16A(+12V)
Max Power (Watt)	–40°C to 65°C 200W
Output Voltage (Volts)	+5VSB
Output Current (Amps)	3A (+5VSB)
Efficiency	>87% @20% load, >87 @50% load, >87% @100% load
Ripple P-P (mV) (max.)	+12V:120, +5VSB:50
Total Regulation	±5%
GENERAL SPECIFICATIONS	
Hold-up Time (min.)	10mS@-48VDC
Over Voltage Protection	Latch off
Over Current & Short Circuit Protection	Auto Recovery
Over Temperature Protection	Auto Recovery
FAN Failure Protection	Auto Recovery
Hot Swap	Yes, 1+1 redundant
Load Sharing	Yes
Hi-pot	1400VDC
ENVIRONMENTAL SPECIFICATIONS	
Operating Temperature Range	–40°C to 65°C
Storage Temperature Range	–40°C to +70°C
Humidity, Non-Condensing	0 to 95% RH
EMI	Meets FCC/CISPR 22 Class A(under 6dB) Specification

Table 6-4 DC/DC Power Supply Specification

6.2.3 PSU LED Status Information

PSU LED behavior is shown as below in various conditions, detailed PSU status is stored in PSU EEPROM and can be accessed by BMC through ipmitool commands:

LED behavior for condition Power supply module1 + Power supply module2 (in normal operation), Power supply module2 LED will be solid GREEN in this case.

Power supply Module1 conditions	Module1 LED	Module2 LED
No power input to this PSU or power input Vin UVP triggered	1Hz Flashing Red	Green
Power input Vin valid, 5V standby Vout valid, P12V Vout is not enabled by system	1Hz Flashing Green	
Power input Vin valid, P12V & P5V_STB Vout valid, Power supply is in normal operation condition	Green	
Power supply is shut down due to Vin OVP, Vout OVP/UVP/OCP/SCP, OTP events or fan failure	Red	
Power supply is functional but warning events triggered: Vin UVW/OVW, Vout UVW/OVW/OCW/, OTW	Flashing 1sec Red and 1sec Green	

LED behavior for condition Power supply module1 + Power supply module2 (No power input), Power supply module2 LED will be 1Hz flash RED or off in this case.

Power supply Module1 conditions	Module1 LED	Module2 LED
No power input to all PSUs (Module1 & Module2)	Off	Off
Power input Vin UVP triggered	1Hz Flashing Red	1Hz Flashing Red
Power input Vin valid, 5V standby Vout valid, P12V Vout is not enabled by system	1Hz Flashing Green	
Power supply is shut down due to Vin OVP, Vout OVP/UVP/OCP/SCP, OTP events or fan failure	Red	
Power supply is functional but warning events triggered: Vin UVW/OVW, Vout UVW/OVW/OCW/, OTW	Flashing 1sec Red and 1sec Green	

Notes:
OVP: Over Voltage Protection
UVP: Under Voltage Protection
OCP: Over Current Protection
OTP: Over Temperature Protection
SCP: Short Circuit Protection
Fan failure: RPM<800 when DC power input is valid for this PSU.
OVW: Over Voltage Warning
UVW: Under Voltage Warning
OCW: Over Voltage Warning
OTW: Over Temperature Warning

Table 6-5 LED Status Information of PSU

7 Software Support

The S9500-22XST supports a base software package composed of the following components:

BIOS
The S9500-22XST Supports AMI AptioV BIOS with the x86 CPU module

BMC
The S9500-22XST Supports AMI MegaRAC SP-X BMC firmware for Aspeed AST2400 platform.

ONIE
See http://onie.org/ for the latest supported version

8 Compliance

Environmental	
Operating temperature	-40~65°C
Storage temperature	-40~70°C (–40°F to 158°F)
Operating relative humidity	5%-95% RH (non-condensing)
Storage relative humidity	5%-55% RH (non-condensing)
Dimensions (height x width x depth)	440.0 mm (W) x 302.0 mm (D) x 43.5 mm (H)
Weight	6.6kg

Regulatory Compliances	
Safety	UL 62368-1 IEC/EN 60950-1 IEC/EN 62368-1 BSMI CNS 14336-1
EMC	FCC Part 15, Subpart B, Class A EN55032, Class A EN 300 386 EN 55024 EN 301 489-1 EN 301 489-19 EN 303413 BSMI (CNS 13438), Class A

9 Appendix A – Requirements for IC Approval

Requirements	Details	Link to Section
Contribution License Agreement	OCP CLA, OCPHL Permissive	Section 1
Are all contributors listed in Section 1: License?	Yes	Section 1
Did All the Contributors sign the appropriate license for this spec? Final Spec Agreement/HW License?	Yes	Section 1
Which 3 of the 4 OCP Tenets are supported by this Spec?	Openness Efficiency Impact Scale	UfiSpace IC Presentation (Tenants on slide 12)
Is there a Supplier(s) that is building a product based on this Spec? (Supplier must be an OCP Solution Provider)	Yes	UfiSpace (OCP Solution Providers Directory)
Will Supplier(s) have the product available for GENERAL AVAILABILITY within 120 days?	Yes	Appendix B

10 Appendix B – UfiSpace – OCP Supplier Information

Table of supplier information for the S9500-22XST Disaggregated Cell Site Gateway Routers

Supplier Information	
Company	Ufi Space Co. Ltd.
Contact Info	sales@ufispace.com
Product Name	Disaggregated Cell Site Gateway Router
Product SKU#	S9500-22XST
Link to Product Landing Page	S9500-22XST

Summary of supplier requirements

Requirements	Details	Link to Section
Which Product recognition?	OCP Accepted™	Pending Approval
If OCP Accepted™, who provided the Design Package?	UfiSpace	Pending Approval
2021 Supplier Requirements for your product(s)		Pending Approval