EDGECORE Networks Corporation

Edgecore AS7926-80X

Switch Specification

Revision 1.0

OPEN

Compute Project

Revision History

Revision	Date	Author	Description
1.0	7/29/2019	Jeff Catlin	Initial Release

Contents

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	AS7926-40/80X
CPU sub-system	CPU: Intel Xeon D1519 1.5G DDR SDRAM: 8GB x 2 2133MHz with ECC (SO-DIMM) DDR4 SPI Flash (Boot): 16MB x 2 mSATA: 128GB MLC TPM: SLB 9665XT2.0 FW5.63 INFINEON
Management	UART RS232 console port (RJ45), Out-band Management Ethernet port (RJ45), 2xSFP+
MAC	Broadcom BCM88690
Ethernet Ports	40/80 x 100G QSFP28
BMC	AST2400 (optional)
Gearbox	Broadcom BCM 81724
Power Supply	1600W PSU Acbel FSJ001-610G
Cooling	4/8 fan-tray modules with 60mm x60mm x 76mm 12V fans, hot-swappable

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Scope

This document outlines the technical specifications for the Edgecore AS7926-80K Open Aggregation Router Platform submitted to the Open Compute Foundation.

Overview

This document describes the technical specifications of the AS7926-80K Open Aggregation Router designed by Edgecore Networks Corporation. The AS7926-80X is a cost optimized design focused on the aggregation of 100G connections. The AS7926-80K is an eighty port 100G switch composed of a main PCB , a matching mezzanine PCB, and CPU module.

The AS7926-80K Aggregation Router is based upon Broadcom's StrataDNX silicon namely the BCM 88690 (AKA Jericho2) and the BCM16K (AKA OP2).

The BCM 88690 silicon is geared toward next generation carrier aggregation deployments supporting advanced features such as

- 8GB Deep packet buffering
- Support for native 400G Ethernet interfaces
- Off Chip expandability of databases and statistical gathering
- Over 60K wire rate queues
- Over 190K meters

The BCM16K is included in the AS7926-40/80K designs and provides the off-chip database expandability and statistical gathering for the BCM 88690 silicon. The BCM16K provides massive expandability of IPv4/V6 routing tables, ACL tables, and enhanced statistical gathering capabilities.

The AS7926-80K designs utilize Broadcom's BCM 81724 gearbox silicon to maximize the 100G port density of the native PAM4 50G serdes contained in the BCM88690.

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The AS7926-80X supports traditional features found in switches such as:

- Redundant field replaceable power supply and fan units
- Support for "Front to Back" air flow direction
- Supports a modular CPU card that allows flexibility in the CPU and/or memory configurations that can be offered.
- Support for AC or DC power supply units

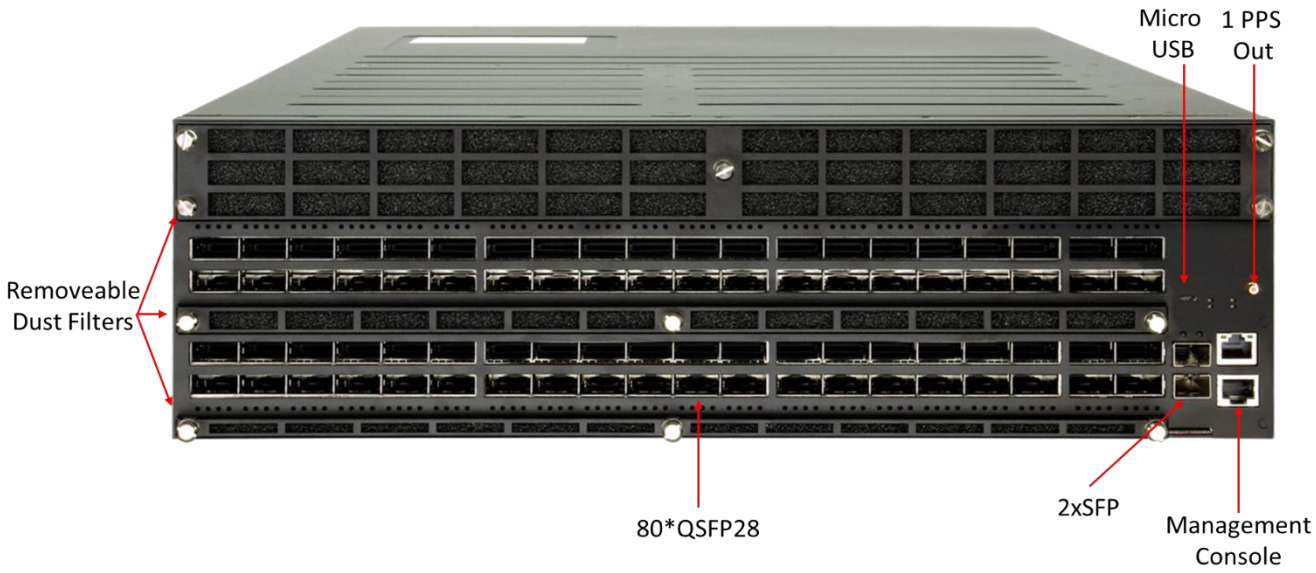
Physical Overview

Front View

Rear View

Front View Detail

Front Panel Ports

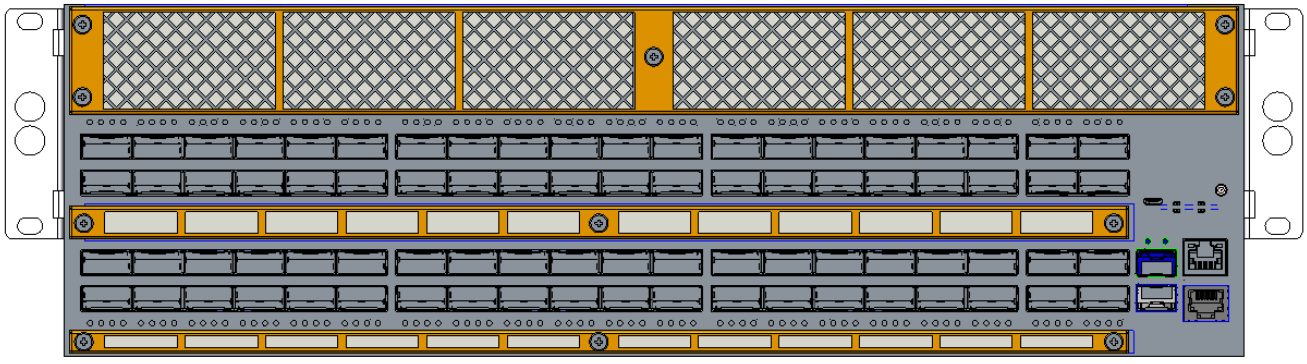


- Micro USB port console port
  - Used for storage and file transfer
- RJ45 Console Port
  - Used for RS232 type management
- RJ45 10/100/1000 Ethernet management port
  - Connected directly to the system CPU
- 2x10G SFP+ ports
  - Connected directly to the system CPU
- 1PPS output port

1. Hardware Architecture

1.1. Overview

Front Panel:



Rear Panel:

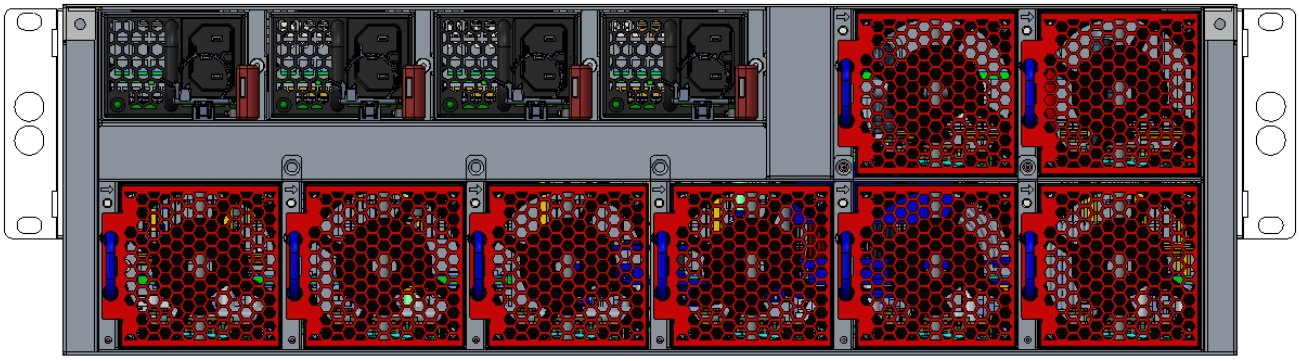


Table 1. System Overview

	ASF7680BBX-0418-EC
MAC	Broadcom BCM88690, 1 pcs, 4.8Tb/s Integrated Packet Processor, Traffic Manager, and Fabric Interface Single-Chip Device
TCAM	Broadcom BCM16K knowledge-Based Processor
PHY	Broadcom BCM81724 8x56 Gb/s PAM-4 to 16x25 Gb/s NRZ Reverse Gearbox
CPLD	ALTERA ALTERA 5M1270 ZF256C5N (2 pcs, BGA256 package)
PCB	24-Layers, TUC TU933+ for Mainboard 12-Layers, TUC TU872LK for CPU module 4-Layers, TG-150 for Fan board 22-Layers, TG-150 for PDU board
Power Supply	12V from PSU * 4.
Cooling	8 fan-tray modules with 8 pcs of 12V fans, hot-swappable
Dimension	PCB: 450 mm (L: Depth) x 432mm (W: Width) x 3.18 mm (H: Height)
Ethernet Ports	80x QSFP28
OOBF Ports	2x SFP+
Console Port	1x RJ-45
Ethernet Mgmt Port	1x RJ-45
USB Port	1x micro USB 2.0 type B
1PPS Port	1x SMB male connecter

1.2. Block Diagram

The high-level block diagram shown as below

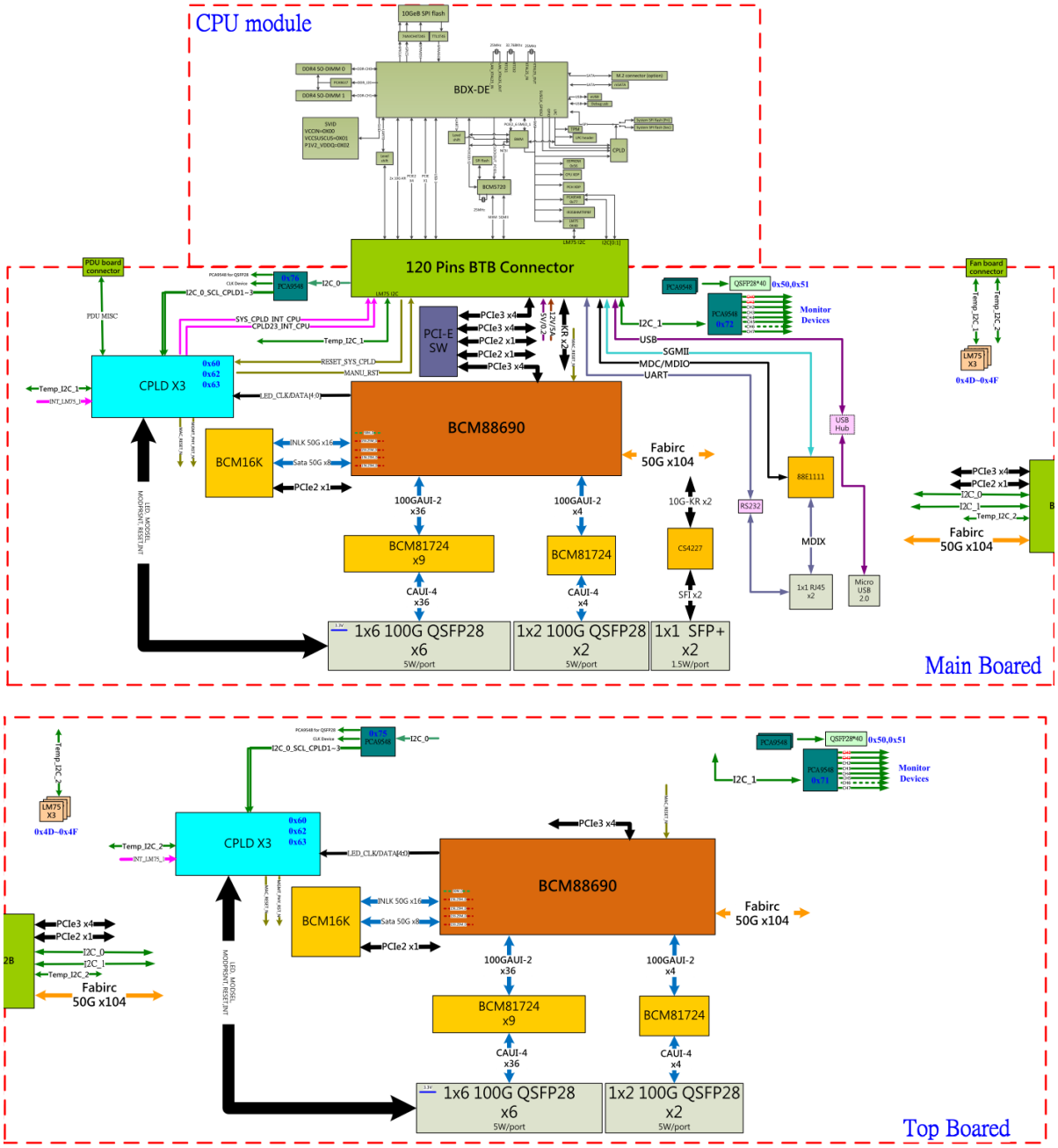


Figure 1. Block Diagram

1.2.1. Clock Tree

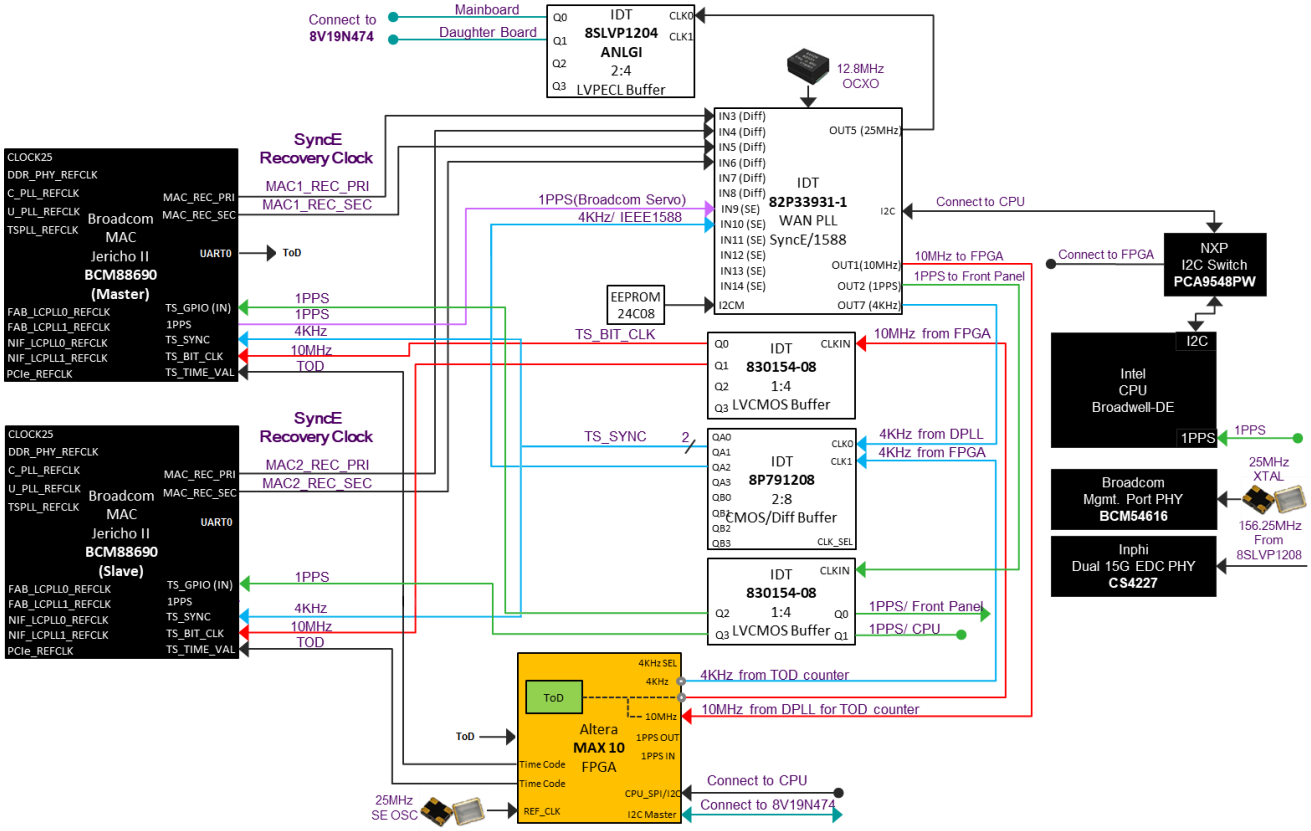


Figure 2. Bottom Main Board WANPLL Clock Tree

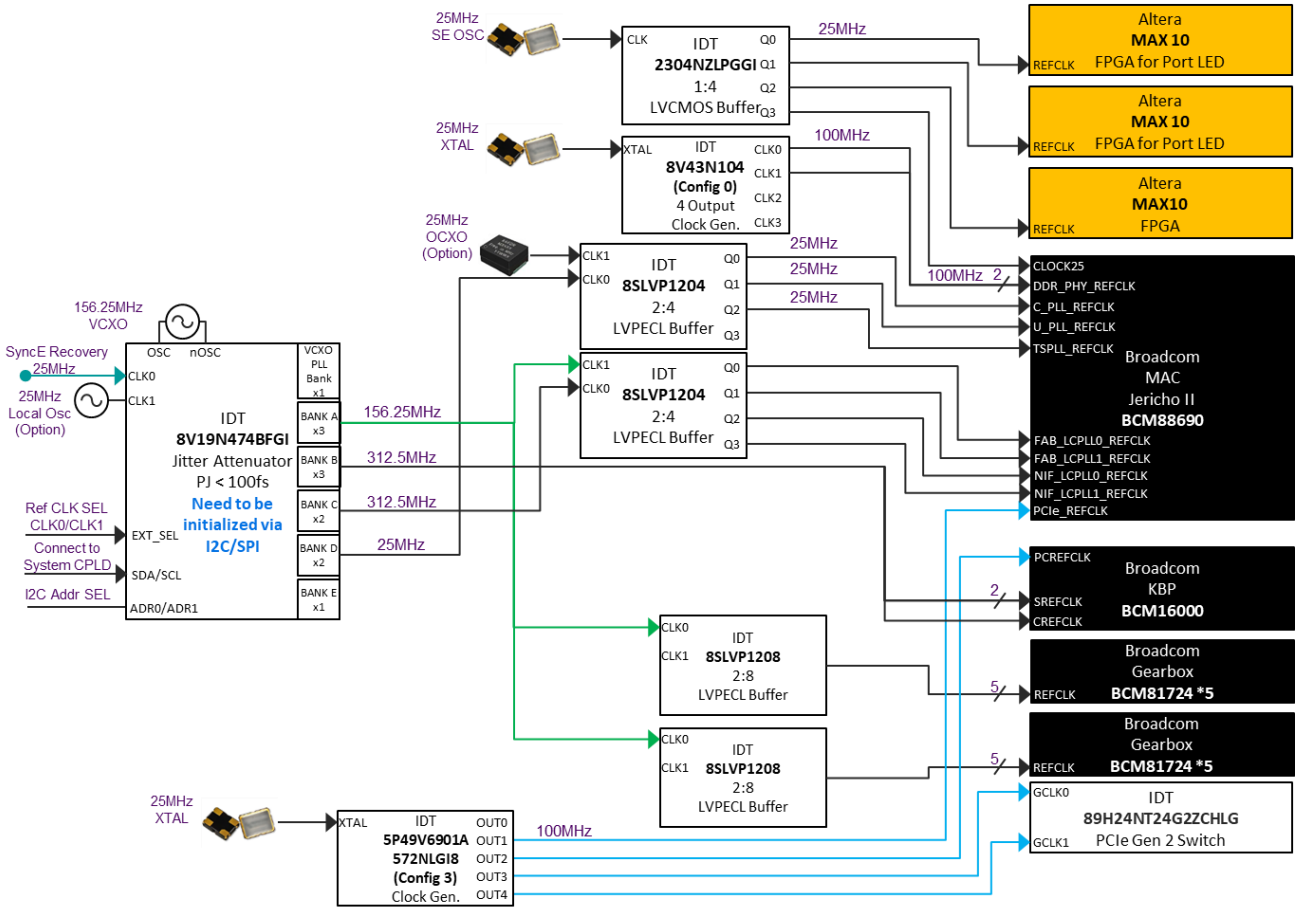


Figure 3. TOP/BOTTOM Mainboard Clock Tree

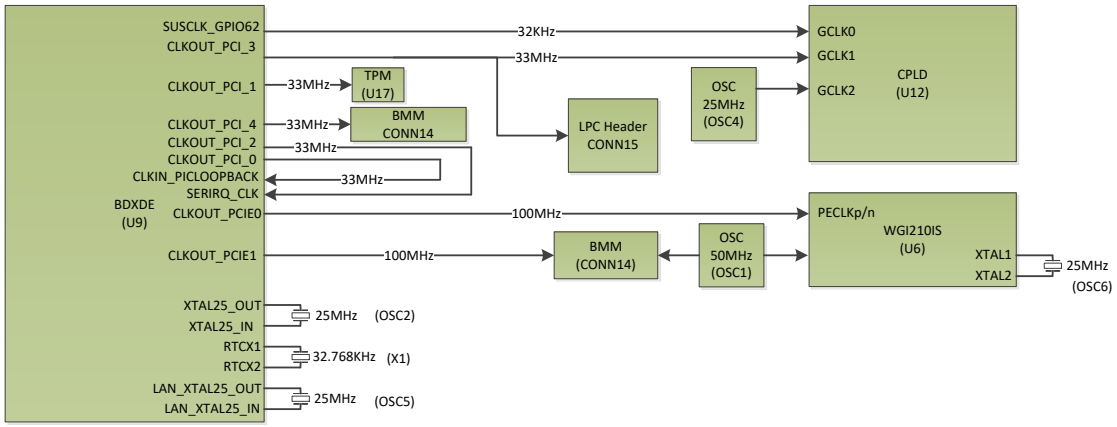


Figure 4. CPU Module Clock Tree

1.2.2. Power Tree

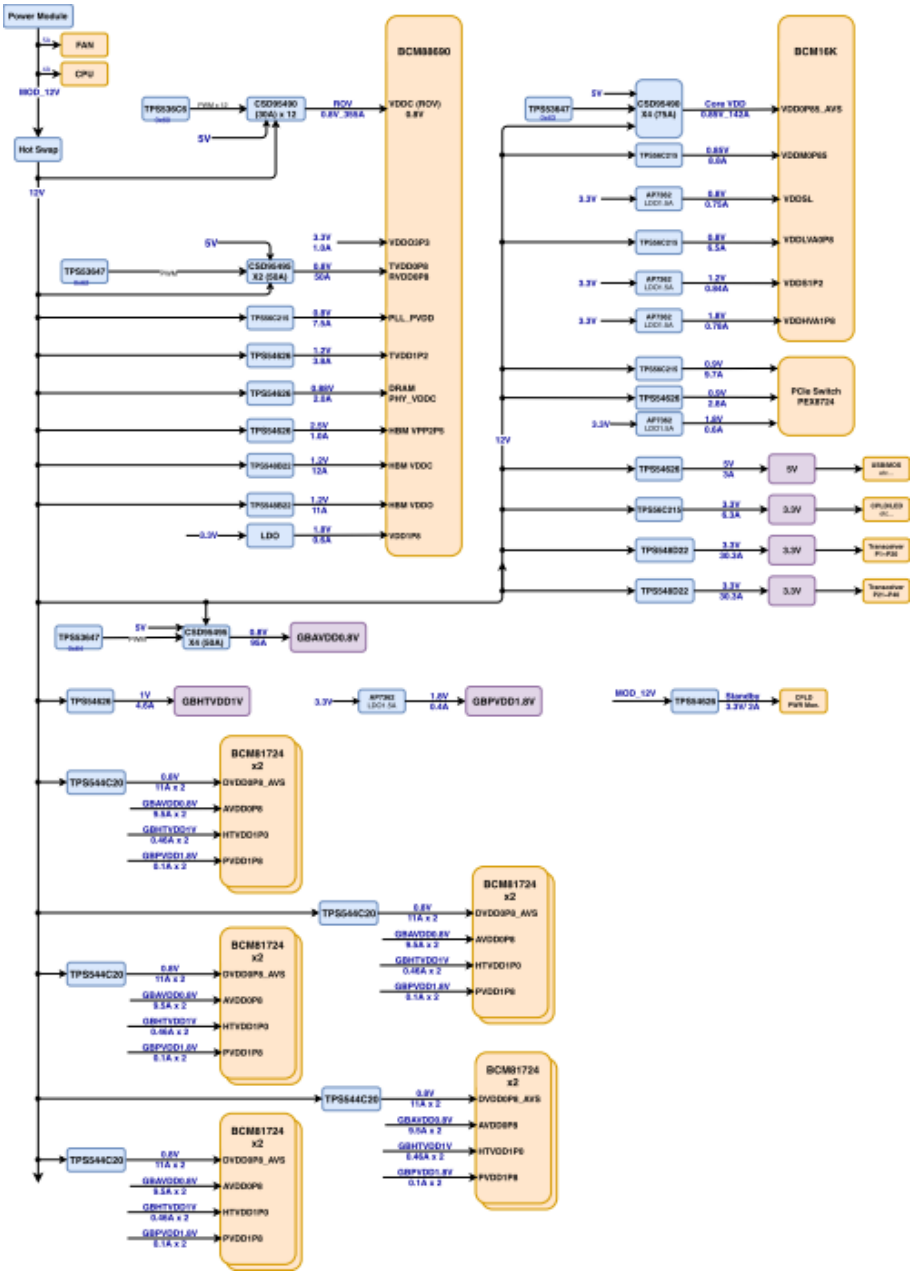


Figure 5. Main Board Power Tree

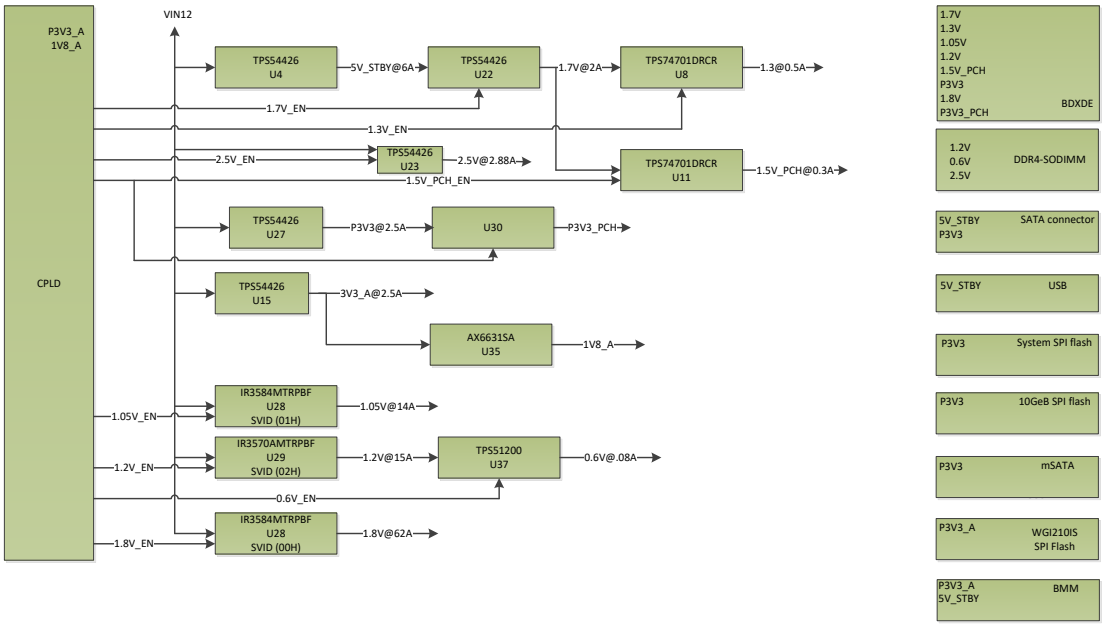


Figure 6. CPU module Power Tree

1.2.3. Main Board Reset Tree

The reset system will follow as below.

1. The CPU Module and Main Board will be power on. In addition, the reset monitor IC will check DC power voltage if reach the threshold.
2. The monitor IC will send **UCD_CPLD_PON_RST_L** signal to CPLD if all power is OK.
3. CPLD pass the **Manu_RST** signal to CPU Module, and hold the all reset signals of LC's device
4. When the reset process of CPU completes, the CPLD on Main Board will receive the **RESET_SYS_CPLD** signal from CPU Module.
5. When the system running, the Main Board CPLD has different register for every device's rest signal. CPU can reset Main Board device separately via Main Board CPLD1 register.

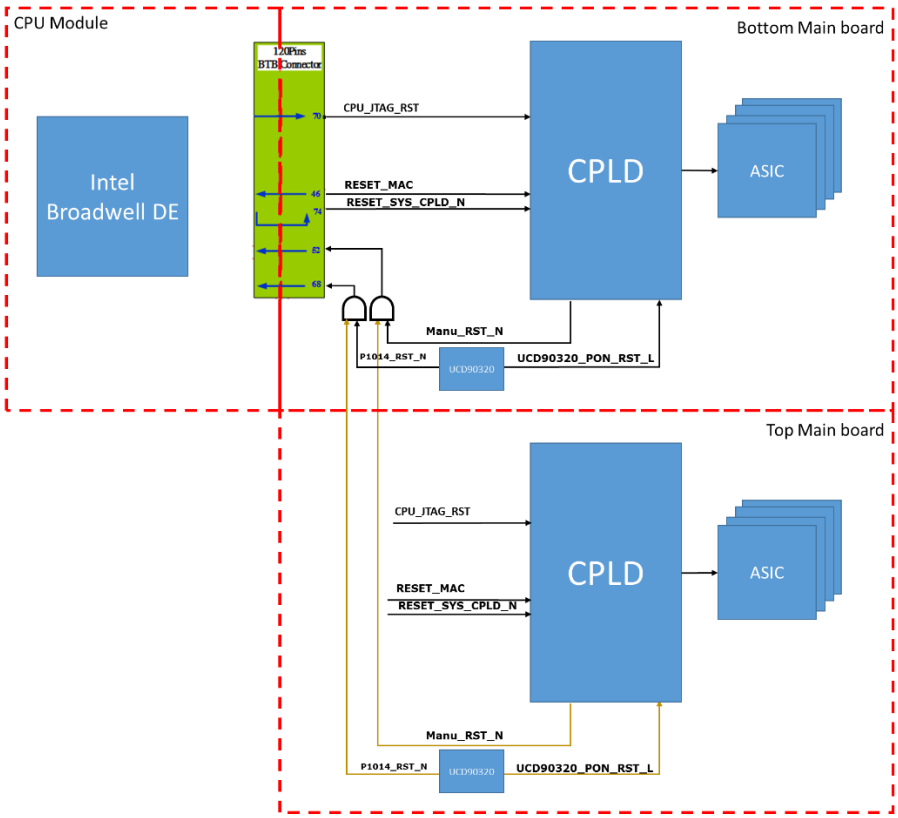


Figure 7. Reset Tree

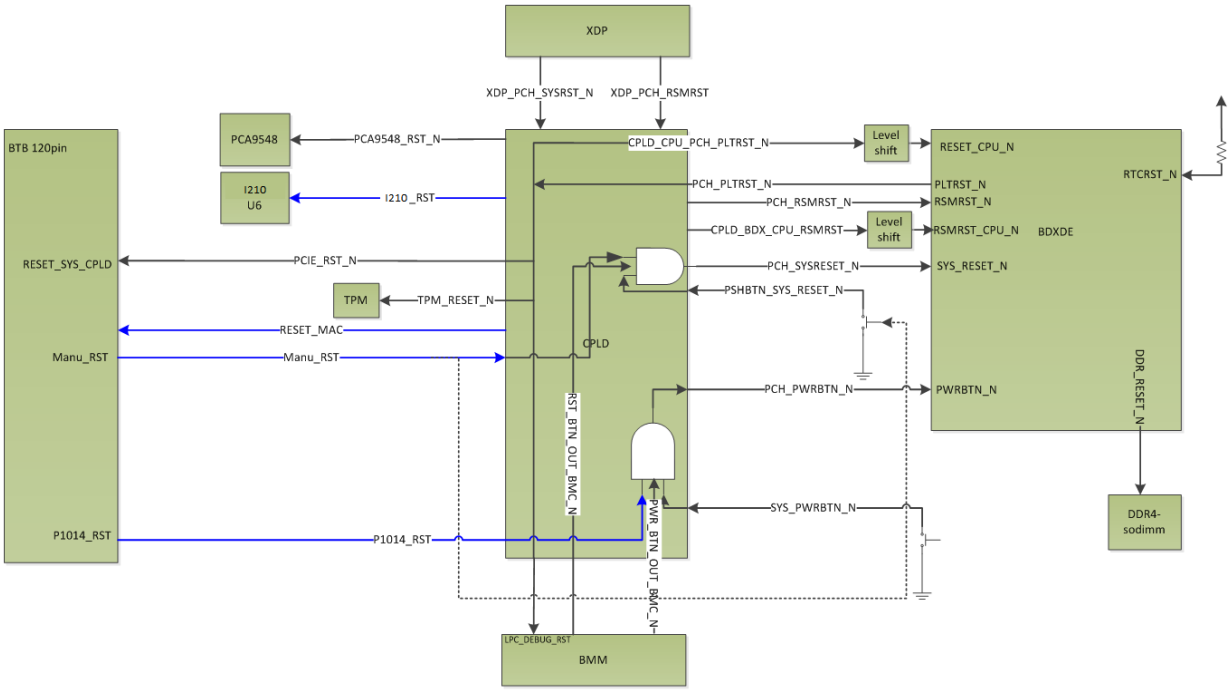


Figure 8. CPU Module Reset Tree

1.2.4. Power up/down Sequence

There are three chips need to concern about power up/down sequence in this system. One is MAC (BCM88690), another is OP2 (BCM16K) and the other one is Gearbox (BCM81724).

For additional information refer to the appropriate Broadcom datasheets

BCM88690:

Figure 9. MAC Power Sequence

For specific information refer to the appropriate Broadcom datasheets

BCM16K:

Figure 10. OP2 Power Sequence

For specific information refer to the appropriate Broadcom datasheets

BCM81724:

Figure 11. BCM88775 Power Sequence

For specific information refer to the appropriate Broadcom datasheets

1.2.5. ROV & AVS Adjustment

MAC (BCM88690), OP2 (BCM16K) and Gearbox (BCM81724) Core Voltage need to keep adjust as different application loading to optimize performance and power consumption. OP2 and Gearbox can auto adjust their Core Voltage (AVS) via Peripheral circuit and SDK, but Core Voltage of MAC need to adjust via NOS Driver.

To control the MAC Core Voltage, the NOS need to get recommend voltage value of MAC via SDK or CPLD. To get recommend voltage value from CPLD, read ROV value from Register 0x52[2:0] of CPLD1 and check the mapping with recommend voltage. Please check Register 0x52 of CPLD1 in Main board CPLD spec for detail

After get recommend voltage, NOS need to set the output voltage of J2 ROV regulator to meet recommend voltage. To do it, use I2C interface to access J2 ROV regulator. The regulator support PMbus so can use it to adjust the output voltage to meet recommend voltage.

Table 2. MAC ROV Table

For specific information refer to the appropriate Broadcom datasheets

1.3. PCI-E Architecture

Jericho2 and OP2 need to use PCI-E to do initialization and configuration. Jericho2 PCI-E interface is Gen3 x4 and OP2 is Gen2 x1. But CPU module only provide one Gen3 x4 PCI-E interface so need to have a PCI-E switch (PEX8724) to bridge all Jericho2 and to CPU.

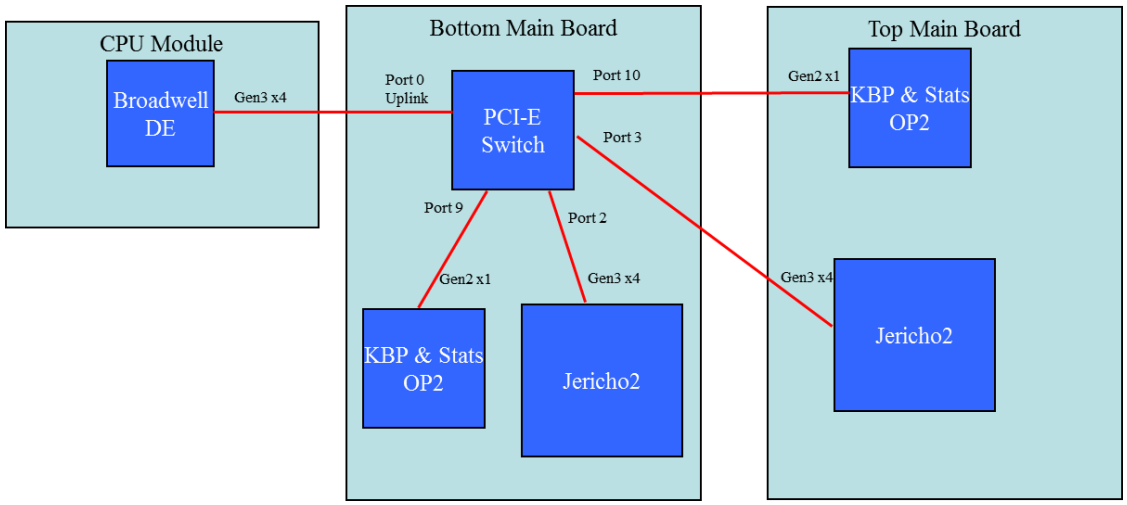


Figure 12. PCI-E Architecture

1.4. MIIM Architecture

To do initiation and configuration of Gearbox (BCM81724), S/W need to use the MIIM interface of Jericho2 to do it. Jericho 2 have six MIIM interfaces MIIM[6:0]. MIIM0 reserved for OP2. MIIM1 connect to Gearbox 1 and 2, MIIM2 connect to Gearbox 3 and 4,…, MIIM5 connect to Gearbox 9 and 10.

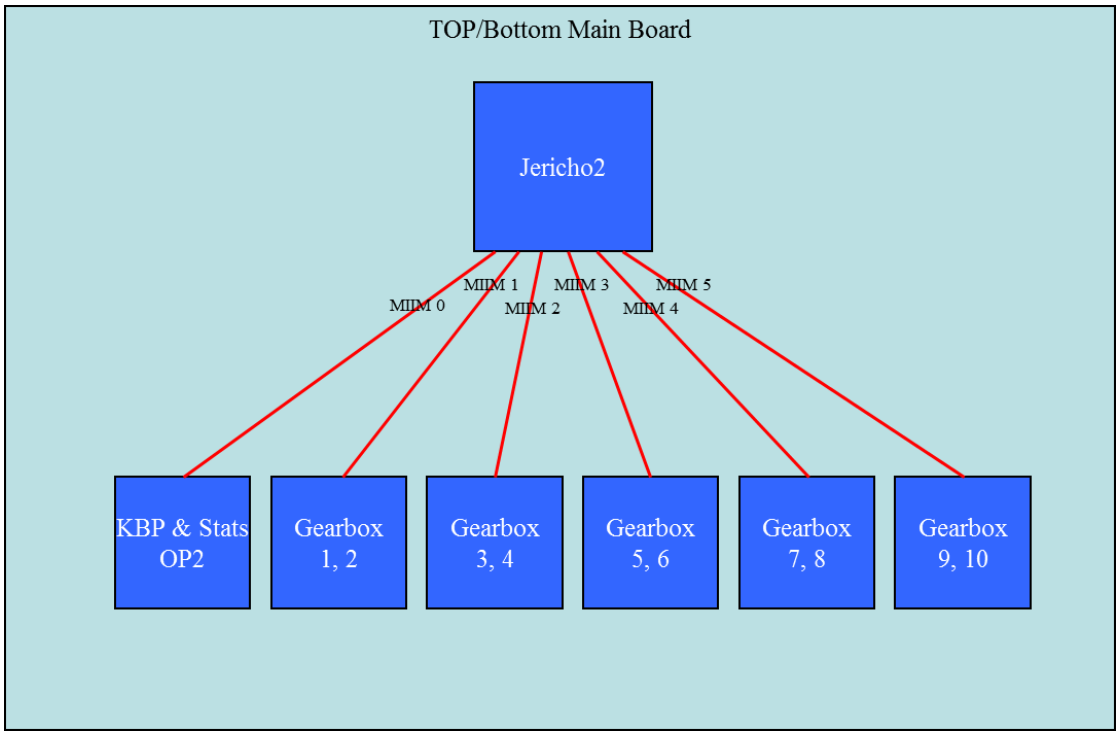


Figure 13. MIIM Architecture

1.5. JTAG Architecture

The JTAG interface can use to upgrade the CPLD firmware. To upgrade the CPLD of CPU module and switch JTAG interface to Main Board, please check detail in chapter 3.11.3.

To upgrade the CPLD of Main board, the JTAG interface switch to Bottom Main Board when SW1_Select set to “0” and switch to Top Main Board when SW1_Select set to “1”. The control the SW1_Select, please check detail of Register 0x61 of CPLD1 in Main Board CPLD specification.

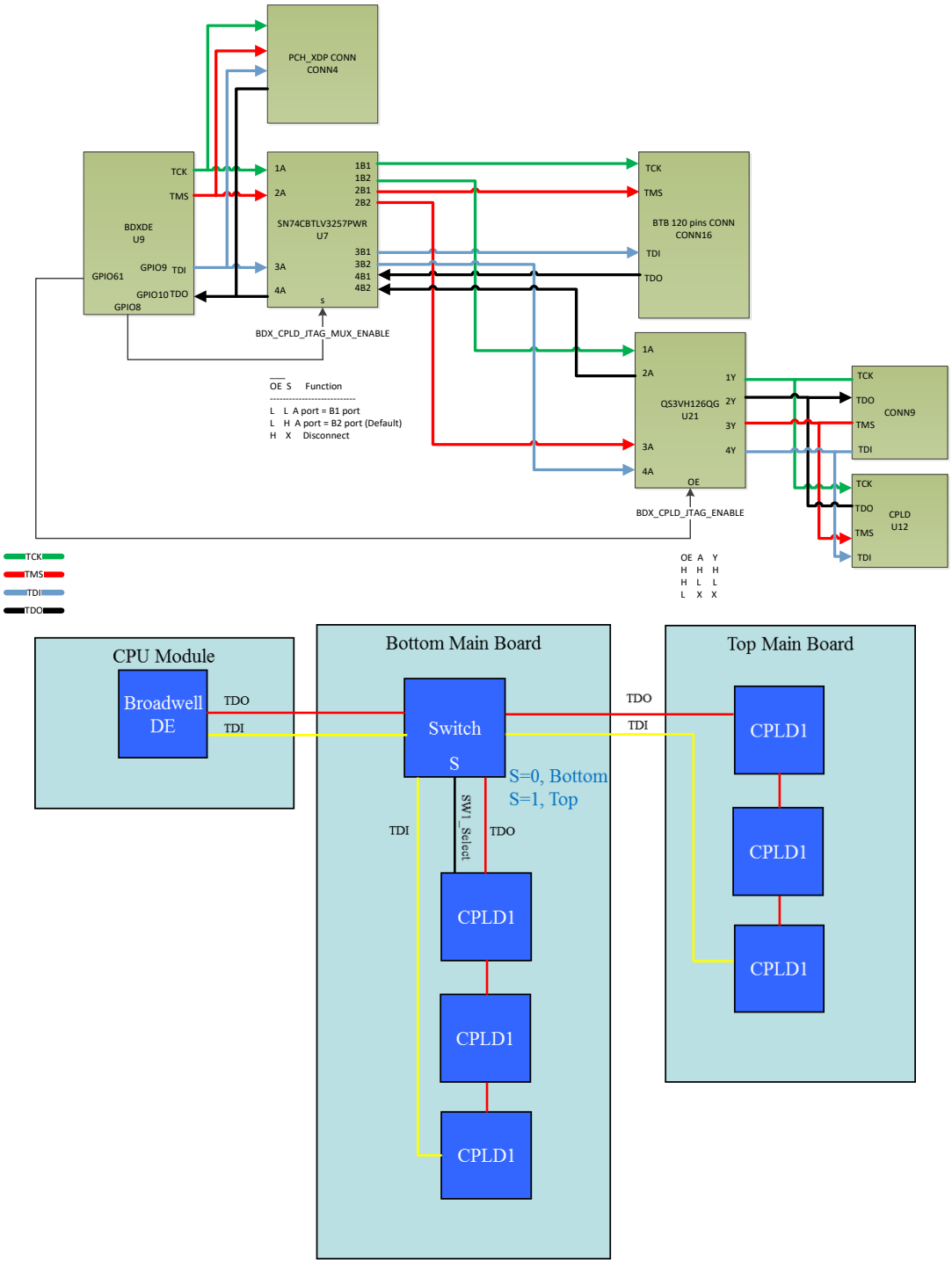


Figure 14. JTAG Architecture

1.6. I2C/SMBus Architecture

The SMbus from BDX-DE can access the CPU board and main board device via SMBUS.

The LM75 (0x4B) is accessed by the CPLD on line card.

The I2C information from DDR SPD EEPROM needed to read via another SMbus only used for DDR SPD.

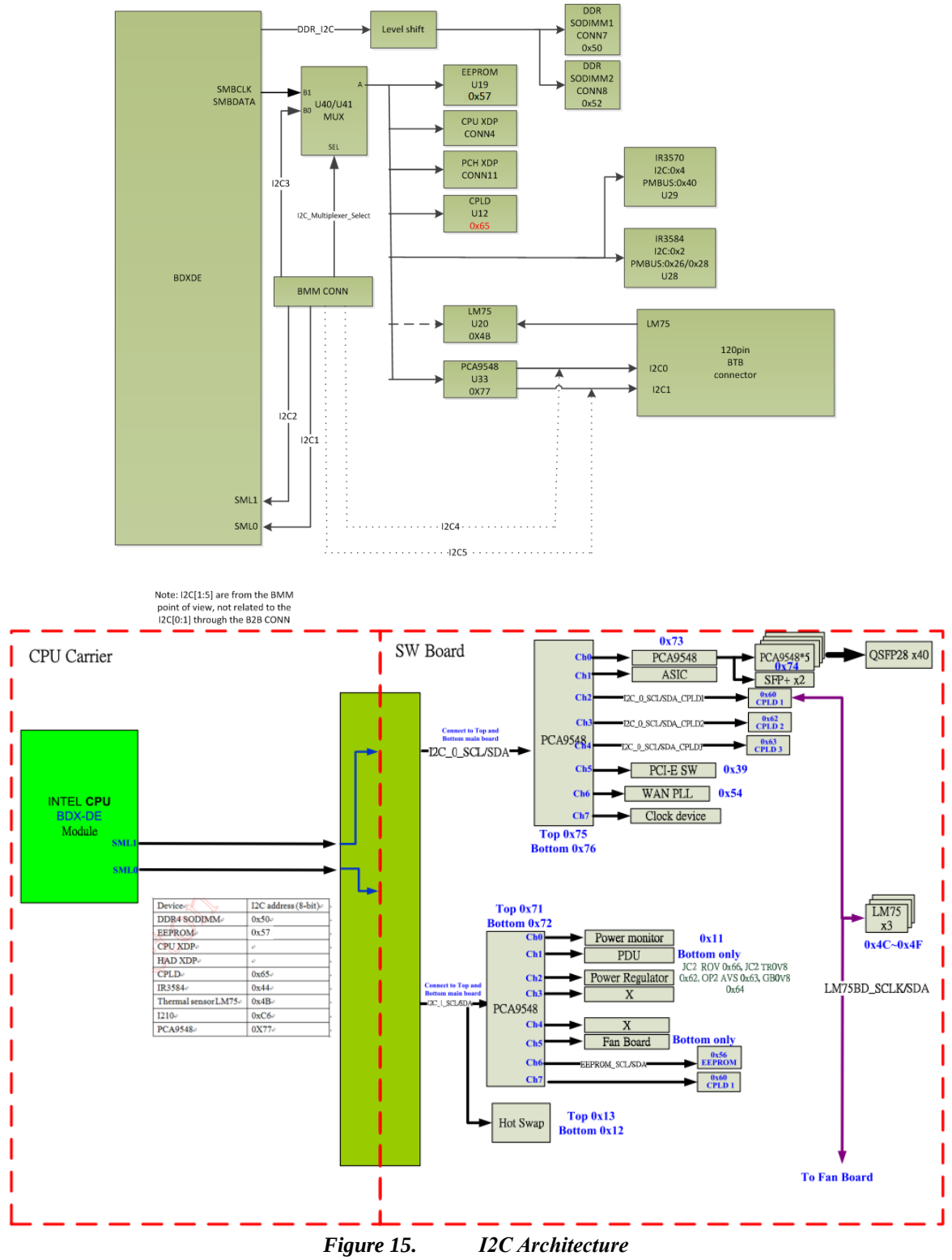


Figure 15. I2C Architecture

CPU	BTB connecter	Device	Port	Device	Port	Device	Port	Description
Link	I2C_0 (J5/L5)	Top: PCA9548 0x75 Bottom: PCA95480 x76	ch0	PCA9548 0x73	ch0	PCA9548 0x74	ch0~ ch7	QSFP_P1~ QSFP_P8
					ch1	PCA9548 0x74	ch0~ ch7	QSFP_P9~ QSFP_P16
					ch2	PCA9548 0x74	ch0~ ch7	QSFP_P17~ QSFP_P24
					ch3	PCA9548 0x74	ch0~ ch7	QSFP_P25~ QSFP_P32
					ch4	PCA9548 0x74	ch0~ ch7	QSFP_P33~ QSFP_P40
					ch5	SFP+ OOBF 0		Bottom Only
					ch6	SFP+ OOBF 1		Bottom Only
					ch7	CS4227 0x5F		Bottom Only
			ch1	BCM88690				Reserve
				USB hub 0x50				Reserve
			ch2	CPLD_1 0x60				
			ch3	CPLD_2 0x62				
			ch4	CPLD_3 0x63				
			ch5	PCIe switch 0x39				PEX8724 Bottom Only
			ch6	WANPLL 0x54				82P33931 Bottom Only
			ch7	Jitter Attenuator 0x6C				Reserve
	I2C_1 (c5/f5)	Top: PCA9548 0x71	ch0	Power monitor 0x11				UCD90320
			ch1	PDU Board				Bottom Only

		Bottom: PCA95480 x72	ch2	Power Regulator J2 ROV: 0x66 J2 TR0V8: 0x62 OP2 AVS: 0x63 GB0V8: 0x64				
			ch3	NA				
			ch4	NA				
			ch5	Fan Board				Bottom Only
			ch6	EEPROM 0x56				
			ch7	CPLD1 0x60				
		Hot swap	0x12					Bottom board
		Hot swap	0x13					Top board

Table 3. I2C/SMBus Table

1.7. NIF/Fabric Port Mapping

Below are the port mapping between MAC and front port number

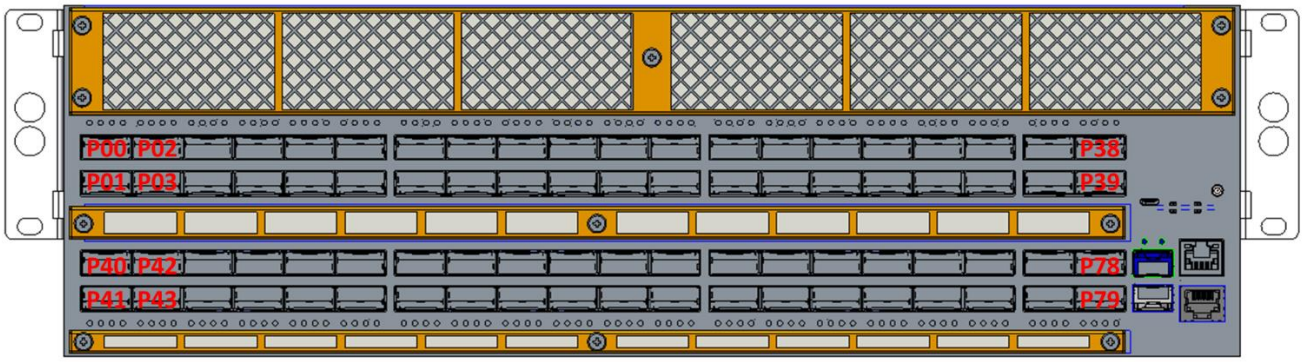


Figure 16. Front Port Mapping

Table 4. Top/Bottom MAC port configuration

MAC Lane Mapping			P/N Swap	Gear Box		Top/Bottom Front Port
Port	TX/RX	Lane		Host side	Device	
PM50-0 100GAUI-2	TX	NIF_TX_04	No	HRX_0	1	00/40
		NIF_TX_05	Yes	HRX_1		
		NIF_TX_06	No	HRX_2		01/41
		NIF_TX_07	Yes	HRX_3		
		NIF_TX_02	Yes	HRX_4		02/42
		NIF_TX_03	No	HRX_5		
		NIF_TX_01	No	HRX_6		03/43
		NIF_TX_00	No	HRX_7		
	RX	NIF_RX_03	No	HTX_0		00/40
		NIF_RX_02	Yes	HTX_1		
		NIF_RX_06	No	HTX_2		01/41
		NIF_RX_01	No	HTX_3		
		NIF_RX_00	Yes	HTX_4		02/42
		NIF_RX_04	No	HTX_5		
		NIF_RX_07	No	HTX_6		03/43
		NIF_RX_05	Yes	HTX_7		
PM50-1 100GAUI-2	TX	NIF_TX_08	Yes	HRX_0	2	04/44
		NIF_TX_11	No	HRX_1		
		NIF_TX_09	No	HRX_2		05/45
		NIF_TX_10	Yes	HRX_3		
		NIF_TX_12	No	HRX_4		06/46
		NIF_TX_13	Yes	HRX_5		
		NIF_TX_14	No	HRX_6		07/47
		NIF_TX_15	No	HRX_7		
	RX	NIF_RX_09	No	HTX_0		04/44
		NIF_RX_11	No	HTX_1		
		NIF_RX_08	Yes	HTX_2		05/45

MAC Lane Mapping			P/N Swap	Gear Box		Top/Bottom Front Port
Port	TX/RX	Lane		Host side	Device	
		NIF_RX_10	Yes	HTX_3		
		NIF_RX_14	Yes	HTX_4		06/46
		NIF_RX_15	No	HTX_5		
		NIF_RX_12	Yes	HTX_6		07/47
		NIF_RX_13	Yes	HTX_7		
PM50-2 100GAUI-2	TX	NIF_TX_19	Yes	HRX_0	3	08/48
		NIF_TX_16	No	HRX_1		
		NIF_TX_17	Yes	HRX_2		09/49
		NIF_TX_18	No	HRX_3		
		NIF_TX_20	Yes	HRX_4		10/50
		NIF_TX_21	No	HRX_5		
		NIF_TX_22	Yes	HRX_6		11/51
		NIF_TX_23	Yes	HRX_7		
	RX	NIF_RX_19	No	HTX_0		08/48
		NIF_RX_18	Yes	HTX_1		
		NIF_RX_17	No	HTX_2		09/49
		NIF_RX_20	No	HTX_3		
		NIF_RX_16	Yes	HTX_4		10/50
		NIF_RX_22	Yes	HTX_5		
		NIF_RX_21	No	HTX_6		11/51
		NIF_RX_23	Yes	HTX_7		
PM50-3 100GAUI-2	TX	NIF_TX_27	Yes	HRX_0	4	12/52
		NIF_TX_24	No	HRX_1		
		NIF_TX_25	Yes	HRX_2		13/53
		NIF_TX_26	No	HRX_3		
		NIF_TX_28	Yes	HRX_4		14/54
		NIF_TX_29	No	HRX_5		
		NIF_TX_30	Yes	HRX_6		15/55
		NIF_TX_31	Yes	HRX_7		
	RX	NIF_RX_27	No	HTX_0		12/52
		NIF_RX_25	No	HTX_1		
		NIF_RX_26	Yes	HTX_2		13/53
		NIF_RX_28	Yes	HTX_3		
		NIF_RX_24	No	HTX_4		14/54
		NIF_RX_29	No	HTX_5		
		NIF_RX_30	Yes	HTX_6		15/55
		NIF_RX_31	Yes	HTX_7		
PM50-4 100GAUI-2	TX	NIF_TX_35	Yes	HRX_0	5	16/56
		NIF_TX_32	No	HRX_1		
		NIF_TX_34	No	HRX_2		17/57
		NIF_TX_33	Yes	HRX_3		
		NIF_TX_36	Yes	HRX_4		18/58
		NIF_TX_37	No	HRX_5		

MAC Lane Mapping			P/N Swap	Gear Box		Top/Bottom Front Port
Port	TX/RX	Lane		Host side	Device	
		NIF_TX_38	Yes	HRX_6		19/59
		NIF_TX_39	Yes	HRX_7		
	RX	NIF_RX_35	No	HTX_0		16/56
		NIF_RX_33	No	HTX_1		
		NIF_RX_32	No	HTX_2		17/57
		NIF_RX_34	Yes	HTX_3		
		NIF_RX_36	Yes	HTX_4		18/58
		NIF_RX_37	No	HTX_5		
		NIF_RX_38	Yes	HTX_6		19/59
		NIF_RX_39	Yes	HTX_7		
PM50-5 100GAUI-2	TX	NIF_TX_43	Yes	HRX_0	6	20/60
		NIF_TX_40	No	HRX_1		
		NIF_TX_42	No	HRX_2		21/61
		NIF_TX_41	Yes	HRX_3		
		NIF_TX_44	Yes	HRX_4		22/62
		NIF_TX_45	No	HRX_5		
		NIF_TX_46	Yes	HRX_6		23/63
		NIF_TX_47	Yes	HRX_7		
	RX	NIF_RX_43	No	HTX_0		20/60
		NIF_RX_42	Yes	HTX_1		
		NIF_RX_41	No	HTX_2		21/61
		NIF_RX_40	Yes	HTX_3		
		NIF_RX_47	No	HTX_4		22/62
		NIF_RX_44	Yes	HTX_5		
		NIF_RX_45	No	HTX_6		23/63
		NIF_RX_46	No	HTX_7		
PM50-6 100GAUI-2	TX	NIF_TX_95	No	HRX_0	7	24/64
		NIF_TX_94	Yes	HRX_1		
		NIF_TX_93	No	HRX_2		25/65
		NIF_TX_92	Yes	HRX_3		
		NIF_TX_89	Yes	HRX_4		26/66
		NIF_TX_90	No	HRX_5		
		NIF_TX_88	No	HRX_6		27/67
		NIF_TX_91	No	HRX_7		
	RX	NIF_RX_92	No	HTX_0		24/64
		NIF_RX_93	No	HTX_1		
		NIF_RX_95	Yes	HTX_2		25/65
		NIF_RX_88	No	HTX_3		
		NIF_RX_94	Yes	HTX_4		26/66
		NIF_RX_89	Yes	HTX_5		
		NIF_RX_90	No	HTX_6		27/67
		NIF_RX_91	No	HTX_7		
PM50-7	TX	NIF_TX_87	No	HRX_0	8	28/68

MAC Lane Mapping			P/N Swap	Gear Box		Top/Bottom Front Port
Port	TX/RX	Lane		Host side	Device	
100GAUI-2		NIF_TX_86	Yes	HRX_1		
		NIF_TX_85	No	HRX_2		29/69
		NIF_TX_84	Yes	HRX_3		
		NIF_TX_81	Yes	HRX_4		30/70
		NIF_TX_82	No	HRX_5		
		NIF_TX_85	No	HRX_6		31/71
		NIF_TX_83	No	HRX_7		
	RX	NIF_RX_85	No	HTX_0		28/68
		NIF_RX_86	No	HTX_1		
		NIF_RX_87	Yes	HTX_2		29/69
		NIF_RX_84	No	HTX_3		
		NIF_RX_81	Yes	HTX_4		30/70
		NIF_RX_80	No	HTX_5		
		NIF_RX_82	No	HTX_6		31/71
		NIF_RX_83	Yes	HTX_7		
PM50-8 100GAUI-2	TX	NIF_TX_79	No	HRX_0	9	32/72
		NIF_TX_78	Yes	HRX_1		
		NIF_TX_77	No	HRX_2		33/73
		NIF_TX_76	Yes	HRX_3		
		NIF_TX_74	No	HRX_4		34/74
		NIF_TX_73	Yes	HRX_5		
		NIF_TX_75	Yes	HRX_6		35/75
		NIF_TX_72	Yes	HRX_7		
	RX	NIF_RX_77	No	HTX_0		32/72
		NIF_RX_79	No	HTX_1		
		NIF_RX_76	Yes	HTX_2		33/73
		NIF_RX_78	Yes	HTX_3		
		NIF_RX_72	No	HTX_4		34/74
		NIF_RX_73	Yes	HTX_5		
		NIF_RX_74	No	HTX_6		35/75
		NIF_RX_75	Yes	HTX_7		
PM50-9 100GAUI-2	TX	NIF_TX_70	Yes	HRX_0	10	36/76
		NIF_TX_71	No	HRX_1		
		NIF_TX_68	Yes	HRX_2		37/77
		NIF_TX_69	No	HRX_3		
		NIF_TX_66	No	HRX_4		38/78
		NIF_TX_65	Yes	HRX_5		
		NIF_TX_67	Yes	HRX_6		39/79
		NIF_TX_64	Yes	HRX_7		
	RX	NIF_RX_71	Yes	HTX_0		36/76
		NIF_RX_70	No	HTX_1		
		NIF_RX_69	Yes	HTX_2		37/77
		NIF_RX_64	Yes	HTX_3		

MAC Lane Mapping			P/N Swap	Gear Box		Top/Bottom Front Port
Port	TX/RX	Lane		Host side	Device	
		NIF_RX_68	No	HTX_4		38/78
		NIF_RX_65	No	HTX_5		
		NIF_RX_66	Yes	HTX_6		39/79
		NIF_RX_67	Yes	HTX_7		

For the Gear Box BCM81724, below table show the SerDes mapping and the working mode.

Operating Mode (Front-Panel Ports)	Logical Function (Per Port)	Host-Side SerDes Mode Per Port	FEC on Host ASIC	Line-Side SerDes Mode Per Port	FEC Required for Line Side	FEC Function Inside PHY

For additional information refer to Broadcom BCM81724 datasheet

Table 5. MAC to KBP OP2 lane mapping

MAC Lane Mapping		P/N Swap	KBP Lane Mapping
TX/RX	Lane		Core
TX	FAB_TX_004	Yes	RXDATA_0
	FAB_TX_005	Yes	RXDATA_1
	FAB_TX_006	Yes	RXDATA_2
	FAB_TX_007	Yes	RXDATA_3
	FAB_TX_002	No	RXDATA_4
	FAB_TX_003	Yes	RXDATA_5
	FAB_TX_000	No	RXDATA_6
	FAB_TX_001	No	RXDATA_7
RX	FAB_RX_000	No	TXDATA_0
	FAB_RX_001	Yes	TXDATA_1
	FAB_RX_006	Yes	TXDATA_2
	FAB_RX_007	Yes	TXDATA_3
	FAB_RX_004	No	TXDATA_4
	FAB_RX_005	No	TXDATA_5
	FAB_RX_003	Yes	TXDATA_6
	FAB_RX_002	Yes	TXDATA_7
TX	NIF_TX_48	Yes	RXDATA_16
	NIF_TX_49	Yes	RXDATA_17
	NIF_TX_50	Yes	RXDATA_18
	NIF_TX_51	Yes	RXDATA_19
	NIF_TX_52	No	RXDATA_20
	NIF_TX_53	No	RXDATA_21
	NIF_TX_54	Yes	RXDATA_22
	NIF_TX_55	Yes	RXDATA_23
RX	NIF_RX_49	Yes	TXDATA_16

MAC Lane Mapping		P/N Swap	KBP Lane Mapping
TX/RX	Lane		Core
	NIF_RX_48	Yes	TXDATA_17
	NIF_RX_50	No	TXDATA_18
	NIF_RX_51	No	TXDATA_19
	NIF_RX_52	Yes	TXDATA_20
	NIF_RX_53	Yes	TXDATA_21
	NIF_RX_54	Yes	TXDATA_22
	NIF_RX_55	Yes	TXDATA_23
			KBP Static
TX	NIF_TX_63	Yes	RXDATA_32
	NIF_TX_62	Yes	RXDATA_33
	NIF_TX_60	No	RXDATA_34
	NIF_TX_61	No	RXDATA_35
	NIF_TX_59	Yes	RXDATA_40
	NIF_TX_56	Yes	RXDATA_41
	NIF_TX_57	Yes	RXDATA_42
	NIF_TX_58	Yes	RXDATA_43

For the Fabric interface, two Jericho2 used it to connect each other. So only need to swap TX signals to map RX signals. Both Jericho2 of Top/Bottom main board need to do the same swap as following table.

Table 6. Fabric interface lane mapping

Fabric Lane	Mapped RX Lane	Mapped TX Lane	TX P/N Swap
8	FAB_RX_008	FAB_TX_008	Yes
9	FAB_RX_009	FAB_TX_011	Yes
10	FAB_RX_010	FAB_TX_009	No
11	FAB_RX_011	FAB_TX_010	No
12	FAB_RX_012	FAB_TX_014	Yes
13	FAB_RX_013	FAB_TX_015	Yes
14	FAB_RX_014	FAB_TX_012	Yes
15	FAB_RX_015	FAB_TX_013	Yes
16	FAB_RX_016	FAB_TX_016	No
17	FAB_RX_017	FAB_TX_019	No
18	FAB_RX_018	FAB_TX_017	No
19	FAB_RX_019	FAB_TX_018	No
20	FAB_RX_020	FAB_TX_021	Yes
21	FAB_RX_021	FAB_TX_023	Yes
22	FAB_RX_022	FAB_TX_020	No
23	FAB_RX_023	FAB_TX_022	No
24	FAB_RX_024	FAB_TX_026	Yes
25	FAB_RX_025	FAB_TX_027	Yes
26	FAB_RX_026	FAB_TX_025	No
27	FAB_RX_027	FAB_TX_024	Yes

28	FAB_RX_028	FAB_TX_029	Yes
29	FAB_RX_029	FAB_TX_031	No
30	FAB_RX_030	FAB_TX_028	Yes
31	FAB_RX_031	FAB_TX_030	No
32	FAB_RX_032	FAB_TX_034	Yes
33	FAB_RX_033	FAB_TX_032	No
34	FAB_RX_034	FAB_TX_033	No
35	FAB_RX_035	FAB_TX_035	Yes
36	FAB_RX_036	FAB_TX_036	Yes
37	FAB_RX_037	FAB_TX_039	Yes
38	FAB_RX_038	FAB_TX_037	No
39	FAB_RX_039	FAB_TX_038	No
40	FAB_RX_040	FAB_TX_043	No
41	FAB_RX_041	FAB_TX_040	No
42	FAB_RX_042	FAB_TX_042	Yes
43	FAB_RX_043	FAB_TX_041	No
44	FAB_RX_044	FAB_TX_045	Yes
45	FAB_RX_045	FAB_TX_047	No
46	FAB_RX_046	FAB_TX_044	No
47	FAB_RX_047	FAB_TX_046	Yes
48	FAB_RX_048	FAB_TX_051	Yes
49	FAB_RX_049	FAB_TX_050	No
50	FAB_RX_050	FAB_TX_049	No
51	FAB_RX_051	FAB_TX_048	No
52	FAB_RX_052	FAB_TX_055	No
53	FAB_RX_053	FAB_TX_054	Yes
54	FAB_RX_054	FAB_TX_052	No
55	FAB_RX_055	FAB_TX_053	No
56	FAB_RX_056	FAB_TX_058	No
57	FAB_RX_057	FAB_TX_057	No
58	FAB_RX_058	FAB_TX_056	Yes
59	FAB_RX_059	FAB_TX_059	Yes
60	FAB_RX_060	FAB_TX_063	Yes
61	FAB_RX_061	FAB_TX_062	Yes
62	FAB_RX_062	FAB_TX_061	Yes
63	FAB_RX_063	FAB_TX_060	No
64	FAB_RX_064	FAB_TX_065	No
65	FAB_RX_065	FAB_TX_066	No
66	FAB_RX_066	FAB_TX_064	Yes
67	FAB_RX_067	FAB_TX_067	Yes
68	FAB_RX_068	FAB_TX_068	Yes
69	FAB_RX_069	FAB_TX_069	Yes
70	FAB_RX_070	FAB_TX_070	Yes
71	FAB_RX_071	FAB_TX_071	Yes
72	FAB_RX_072	FAB_TX_074	Yes

73	FAB_RX_073	FAB_TX_073	Yes
74	FAB_RX_074	FAB_TX_072	Yes
75	FAB_RX_075	FAB_TX_075	Yes
76	FAB_RX_076	FAB_TX_078	Yes
77	FAB_RX_077	FAB_TX_076	No
78	FAB_RX_078	FAB_TX_077	No
79	FAB_RX_079	FAB_TX_079	Yes
80	FAB_RX_080	FAB_TX_081	No
81	FAB_RX_081	FAB_TX_083	No
82	FAB_RX_082	FAB_TX_080	Yes
83	FAB_RX_083	FAB_TX_082	Yes
84	FAB_RX_084	FAB_TX_084	No
85	FAB_RX_085	FAB_TX_085	No
86	FAB_RX_086	FAB_TX_086	No
87	FAB_RX_087	FAB_TX_087	No
88	FAB_RX_088	FAB_TX_090	Yes
89	FAB_RX_089	FAB_TX_088	No
90	FAB_RX_090	FAB_TX_091	No
91	FAB_RX_091	FAB_TX_089	Yes
92	FAB_RX_092	FAB_TX_094	No
93	FAB_RX_093	FAB_TX_092	Yes
94	FAB_RX_094	FAB_TX_093	Yes
95	FAB_RX_095	FAB_TX_095	Yes
96	FAB_RX_096	FAB_TX_096	No
97	FAB_RX_097	FAB_TX_099	No
98	FAB_RX_098	FAB_TX_097	Yes
99	FAB_RX_099	FAB_TX_098	No
100	FAB_RX_100	FAB_TX_100	No
101	FAB_RX_101	FAB_TX_101	No
102	FAB_RX_102	FAB_TX_102	No
103	FAB_RX_103	FAB_TX_103	No
104	FAB_RX_104	FAB_TX_105	No
105	FAB_RX_105	FAB_TX_104	Yes
106	FAB_RX_106	FAB_TX_106	No
107	FAB_RX_107	FAB_TX_107	No
108	FAB_RX_108	FAB_TX_108	No
109	FAB_RX_109	FAB_TX_111	Yes
110	FAB_RX_110	FAB_TX_110	Yes
111	FAB_RX_111	FAB_TX_119	No

LED Indicator

The unit has 4 status LEDs and 162 port LEDs. The 4 status LEDs are for SYSTEM, PSU, FAN, and Diag. The 162 port LED are for 80 NIF ports and 2 OOBF ports.

1.7.1. Status LED

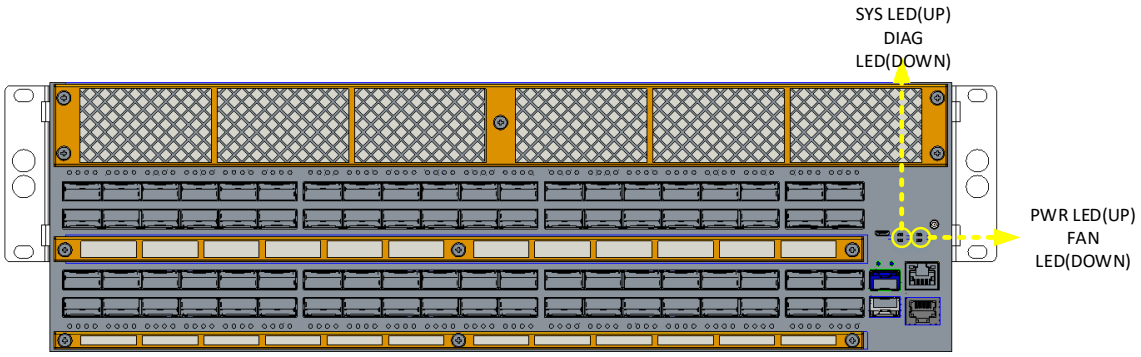


Figure 17. Front panel of 3U Chassis

There are four LED to indication System Status. They are SYSTEM/LOC, PSU, FAN, and Diag. Each LED is tri-color LED so can display many different colors. To control these four LED, Register 0x30 & 0x31 of CPLD3 on bottom Main board used to set what color shall be light for them.

Following table is just an example about how to define Status LED. S/W developer can define it as different requirement and use Register 0x30 & 0x31 of CPLD3 on bottom Main board to implement it. Please check detail in Main board CPLD Spec.

Table 7. Status LED Definition

OPERATING CONDITION	LED SIGNALING
PWR	
All PSU present and work	Solid Green
One PSU did not present or work	Solid Yellow (R+G)
More than one PSU did not present or work	Solid Red
DIAG	
Diagnostic Passed	Solid Green
Diagnostic Error/Failure/Fault	Solid Red
Diagnostic is in progress	Blinking Green
Location Indicated	Solid Blue
Fan	
All FAN module present and work	Solid Green
One FAN module did not present or work	Solid Yellow (R+G)
More than one FAN module did not present or work	Solid Red
SYSTEM/LOC	
Normal Operation	Solid Green
Error/Failure/Bad	Solid Red,
Location Indicated	Blink Green
Not Present	Off

1.7.2. Management Port LED

The management port has two LEDs. One is Link LED on top left side of RJ-45 port and the other is Activity LED on top right of RJ-45 port.

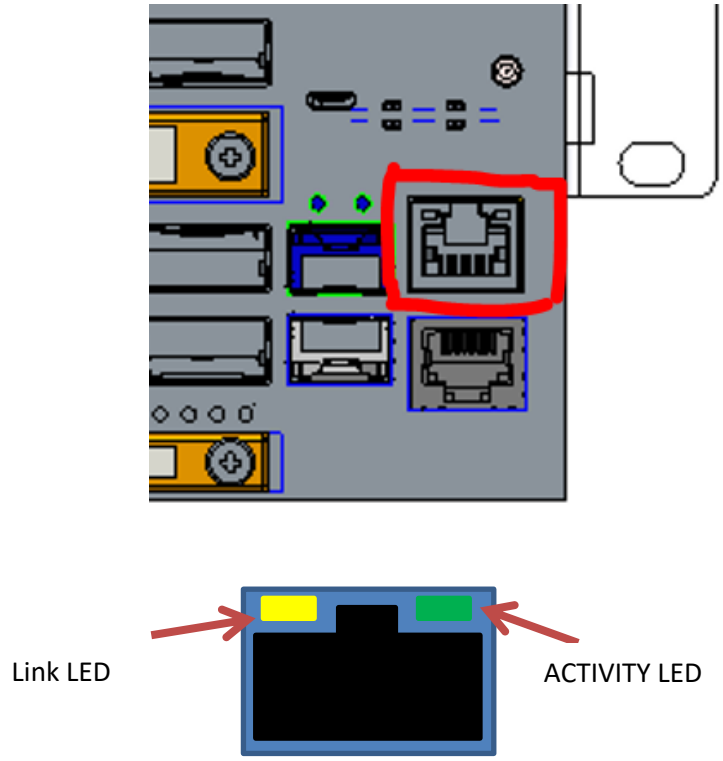


Figure 18. Management Port LED

Table 8. Management Port LED Definition

OPERATING CONDITION	LED SIGNALING
Link LED:	
Port Link up	Solid Yellow
Port link down	off
ACTIVITY LED:	
Power has traffic active	Blink green
Power did not have traffic active	off

1.7.3. NIF Port LED

BCM88690 has two-wire (clock and data) LED interface is to control system LEDs. Both signals are held low during periods of inactivity. A single LED refresh cycle consists of clocking out a programmable number of LED data bits. The LED data signal is pulsed high at the start of each LED refresh cycle, this selection define the Led stream by Figure 13.

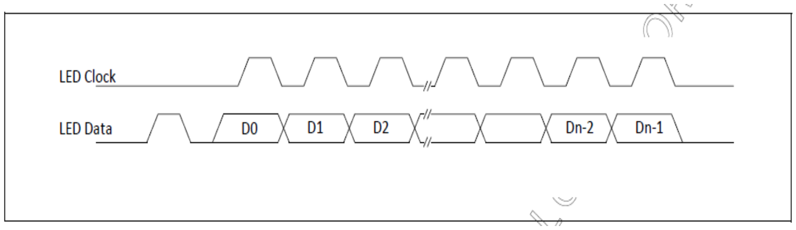


Figure 19. Led Refresh cycle

There are 160 RGB LEDs for 40 ports, and one port is with 2 RGB LEDs. The first LED indicates configuration of the QSF28 port. The Line Card supports 100G/40G and 2x50G breakout modes. Each supported configuration is shown by a different color. The LED CPLDs drive the R/G/B LEDs by de-coding the MAC's LED buses.

To control Port LED, CPLD2 of top board handle the decoding of P00 to P19 and CPLD3 handle the decoding of P20 to P39. CPLD2 of Bottom board handle the decoding of P40 to P59 and CPLD3 handle the decoding of P60 to P79. Each Jericho2 of Top/Bottom board use LED0 bus to connect CPLD2 and LED2 bus to connect CPLD3. Both Jericho2 shall use the stream format showed as below to control related port LEDs.

LED0 Output Order→→→→→→→→→→→→→→→→→→→→→→→→→→→→→

Port	00	01	02	03	04	05	06	07
PM	0	0	0	0	1	1	1	1
SDR NO.	00:01	02:03	04:05	06:07	08:09	10:11	12:13	14:15

→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→

Port	08	09	10	11	12	13	14	15
PM	2	2	2	2	3	3	3	3
SDR NO.	16:17	18:19	20:21	22:23	24:25	26:27	28:29	30:31

→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→

Port	16	17	18	19
PM	4	4	4	4
SDR NO.	32:33	34:35	36:37	38:39

LED2 Output Order→→→→→→→→→→→→→→→→→→→→→→→→→→→→→

Port	20	21	22	23	24	25	26	27
PM	5	5	5	5	11	11	11	11
SDR NO.	40:41	42:43	44:45	46:47	88:89	90:91	92:93	94:95

→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→

Port	28	29	30	31	32	33	34	35
PM	10	10	10	10	9	9	9	9
SDR NO.	80:81	82:83	84:85	86:87	72:73	74:75	76:77	78:79

→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→

Port	36	37	38	39
PM	8	8	8	8
SDR NO.	64:65	66:67	68:69	70:71

Bit Output Order→→→→→→→→→→→→→→→→→→→→→→→→→→→→→→

Port x	Speed (LED0)			Link/Act (LED1)		
Bit	1	2	3	4	5	6

Color	R	G	B	R	G	B

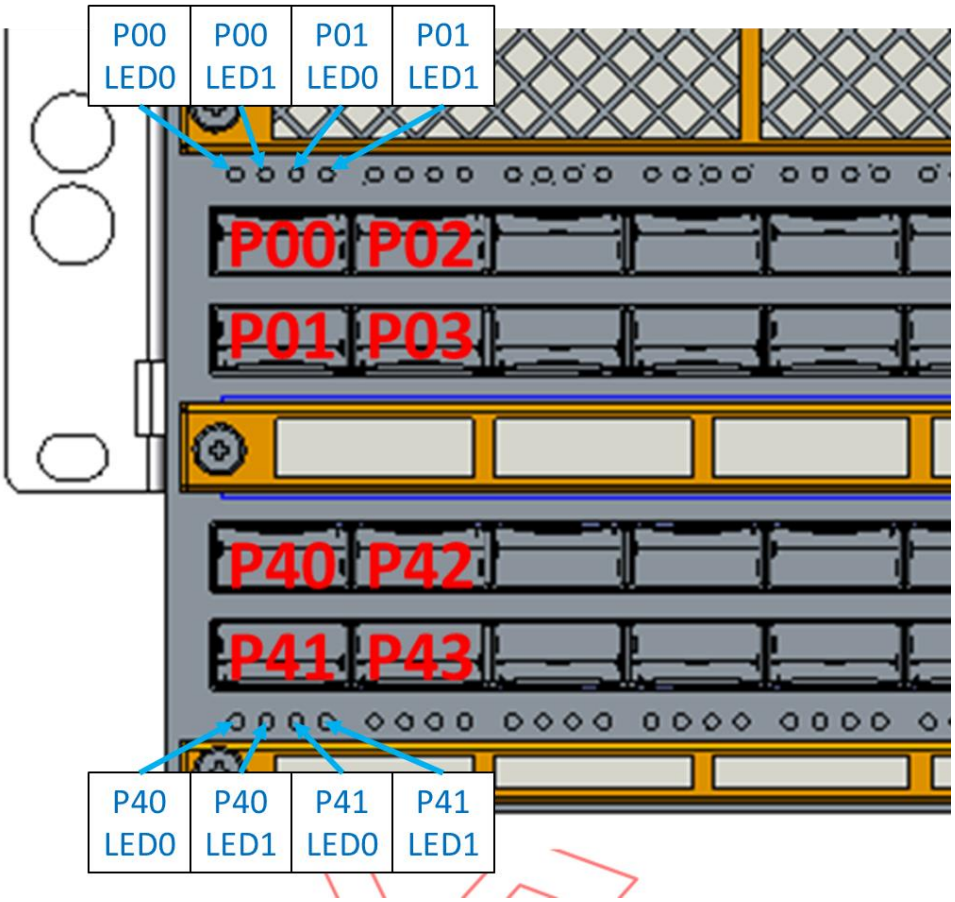


Figure 20. Port Led

Table 9. NIF Port LED definition

OPERATING CONDITION	LED SIGNALING
CONFIGURATION: LED 0	
100G (4 x 25G)	Solid Blue (B)
40G (4 x 10G)	Solid Yellow (R+G)
2 x 50G (2 x 25G)	Solid Cyan (B+G)
All lanes link down	off
LINK/ACTIVITY: LED 1	
All of the configured Ports are linked	Solid Green; blink if activity
Any of configured Ports are NOT linked	Solid Yellow; blink if activity
All ports link down	off

1.7.4. OOBF Port LED

The OOBF port has two LEDs. One is Link LED on top left side of RJ-45 port and the other is

Activity LED on top right of RJ-45 port.

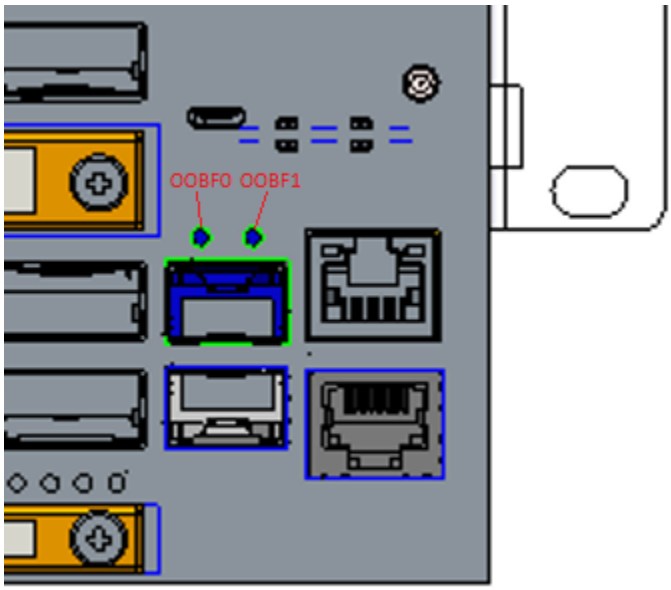


Figure 21. OOBF Port LED

Table 10. OOBF Port LED Definition

OPERATING CONDITION	LED SIGNALING
Port Link up	Solid green
Power has traffic active	Blink green
Port link down	off

2. CPU Sub-system

2.1. Feature

- 2 DDR4 channels, 1DPC with DDR4 2133 ECC SODIMM.
- Memory speed: DDR4 2133, up to 2400.
- PCI Express Lanes :
  - 24 Gen3, 1x16 and 1x8, 6 controllers x4 granularity (Uncore)
  - 8 Gen2, 2x4, 8 controllers x1 granularity (Integrated PCH logic)
- Integrated 10GbE Controller contains two independent 10GbE MACs that support an XGMII interface link to the either KX4 or KR PHY device interfaces.
  - KX4 PHY supports
    - XAUI for XGMII extension
    - 10GBASE-KX4 for gigabit backplane applications.
    - 2500BASE-KX for gigabit backplane applications.
    - 1000BASE-KX for gigabit backplane applications.
  - KR PHY supports
    - 10GBASE-KR for gigabit backplane application

- 1000BASE-KX for gigabit backplane application.
- 10GBASE SFP+ through a XFI compatible interface
- 10GBASE-T through a XFI compatible interface

- Integrated PCH logic
  - PCI Express Base specification, revision 2.0 support for up to eight ports with transfers up to 5GT/s
  - ACPI power management logic support revision 4.0a
  - Enhanced DMA controller, interrupt controller, and timer function.
  - Integrated Serial ATA host controllers with independent DMA operation on up to six ports.
  - xHCI USB controller provides support for up to 4 USB ports, of which four can be configured as SuperSpeed USB 3.0 ports.
  - One legacy EHCI USB controller provides a USB debug port.
  - Integrated 10/100/1000 Gigabit Ethernet MAC witch system defense.
  - System Management Bus (SMBus) specification, version 2.0 with additional support for I2C devices
  - Supports intel Virtualization Technology for Directed I/O (Intel VT-d)
  - Supports intel Trusted Execution Technology (Intel TXT)
  - Integrated clock controller
  - Low Pin Count (LPC) interface
  - Firmware Hub (FWH) interface support
  - Serial Peripheral Interface (SPI) support
  - JTAG Boundary scan support.

2.2. Configuration

2.2.1. Power-On Reset

The cores and uncore support the following reset types. Note PWRGOOD_CPU is driven by the PCH.

Cold reset is the first time when the platform asserts PWRGOOD_CPU and asserts RESET_CPU_N to the uncore. The platform has to wait for the Base Clock (BCLK) and the power to be stable before asserting PWRGOOD_CPU. This results in reset of all the states in the processor, including the sticky state that is preserved on the other resets. PLLs come up, I/O (DMI2, uncore PCI Express, and DDR) links undergo initialization and calibration. Components in fixed and variable power planes are brought up. Ring, router, SAD, and various lookup tables in the core/Cbo are initialized. Once the uncore initialization has completed, then the power is enabled to the cores and cores are brought out of reset. BIOS is fetched from the PCH.

Warm reset is typically a platform wide event and is indicated by assertion and deassertion of the RESET_CPU_N signal on the socket while PWRGOOD_CPU remains asserted. This reset preserves the error log state and machine check bank states for use by platform debug. The warm reset preserves the error log state and machine check bank states for use by platform for post error event analysis. To maintain the DDR memory attached to the processor self refresh and sticky registers remain valid through out a warm reset, the "Reset_warn" message must complete by the processor. The "Reset_warn" is a message that gets issued from the PCH to all sockets prior to warm reset. BIOS will need to program the FlexRatioMSR/CSR in each socket and invoke the Warm Reset to the platform.

The reset flow is divided into the following 5 phases.

- **Phase 0**: Expectations from the platform (before assertion of PWRGOOD_CPU)
  - Initially PWRGOOD_CPU signal is deasserted and RESET_CPU_N is asserted to the socket. PWRGOOD_CPU cannot deassert until RESET_CPU_N is asserted.
  - PWRGOOD_CPU must be asserted no sooner than 2 ms after the IVR Vccin supply has fully ramped-up.
  - Vccioin may be brought up before Vccin for IVR is brought up if not at the same time. Vccioin is intended to source the PECI IO.
  - The PWRGOOD_CPU and RESET_CPU_N signals have "clean" edges.
  - The reference clock (BCLK) is stable.
  - All external power rails have ramped as follows: Vccin, Vccioin, VCCD are up and stable at their nominal values
  - Assert PWRGOOD_CPU (RESET_CPU_N still asserted) only after 2 msec of Vccin, Vccioin and VCCD at tolerance.
  - After the power rails are up and stable for 2 msec and reference clocks are stable, platform asserts PWRGOOD_CPU and continues to assert RESET_CPU_N signal to the socket.
  - PWRGOOD_CPU remains asserted as long as Vccin, Vccioin and VCCD remain stable.
  - No power sequencing between Vccin and VCCD is required.

- **Phase 1**: PCU bring-up
  - Phase 1a: Activity Leading to PCU Start-up
    - Assertion of PWRGOOD_CPU (the trigger to move from the end Phase 0 to the start of Phase 1a).
    - Processor starts a timer (using BCLK) for determinism interval.
    - The PECI and SVID interfaces are held in reset until IVR asserts its power good signal.
    - The PCU PLL is enabled.
  - Phase 1b: Pcode Controlled Preparing for Broad uncore Bring-Up
    - Starting at the sub-phase, all steps should be synchronous.
    - PCU micro controller comes out of reset to start reset pcode execution. This is the planned "re-entry" point for Warm Reset processing.
    - Early reset pcode determines that it is at the start of Phase 1b.
    - Pcode brings the rest of the PCU hardware out of reset.
    - Pcode determines the boot config.
    - Pcode issues SVID command to ramp Vccin to 1.8V for cold reset.
    - Pcode reads and compares Vccin MBVR ICCMAX limit (reg 21h) vs its own supported ICCMAX limit:
      - If VR's ICCMAX ≥ supported ICCMAX then bootup continues.
      - If VR's ICCMAX < supported ICCMAX then bootup halts and system shuts down. MSR 411h IA32_MC4_STATUS logs Error code 0x1e - MCA_VR_ICC_MAX_LESS_THAN_FUSED_ICC_MAX in field MSEC_FW.
    - Pcode sequences uncore non-boot IVRs to ramp up.
    - Pcode signals uncore power good to IIO, IMC.
    - Delivery of the uncore power good signals defines the transition from the end of phase 1b to the beginning of phase 1c.

- Phase 1c: PLL locking and IO Calibration
  - Pcode initiates thermal sensors.
  - Pcode locks PLLs in the following order: IIO, and IMC.
  - Pcode instructs the ring PLLs to start locking.
  - RESET_CPU_N signal is deasserted.
  - De-assertion of RESET_CPU_N signal will bring PCU out of reset and signifies the transition from the end of Phase 1c to the beginning of Phase 2.

- **Phase 2**: Uncore initialization and core bring up
  - The starting assumptions are:
    - All IVRs except core IVRs have ramped-up and are stable.
    - All PLLs except core PLLs have locked.
    - Phase 2 is entered as a result of de-assertion of external pin RESET_CPU_N.
    - Boot mode related straps have been sampled and are available.
    - Some IO link calibration have started and may or may not have completed by the start of this phase.
  - In this phase
    - PCU comes out of reset again and again determines the reset type.
    - Reset is deasserted to the ring units (HA, Cbo, IIO).
    - Reset is de-asserted to System Agents (IMC, IIO).
    - Pcode initializes the ring stops
    - Pcode performs boot mode processing based on straps. Set the advertised firmware, IO, and Intel TXT agent bits appropriately.
    - Pcode services DMI2 handshake protocol. If DMI2 links are used in DMI2 mode, pcode checks if the links have trained to L0. If it's the legacy socket, and if DMI2 links does not reach L0 within 3-4 ms, pcode executes error flow.
    - Pcode determines number of cores, slices and st/mt-threading for the core. In this step pcode also takes into account number of BIOS-disabled cores. Pcode determines whether BIST should be executed. BIST is executed if BIST Strap is set or requested.
    - Pcode programs the logical ids and switches from physical to logical mode.
    - LLC reset and configuration.
    - If it's not service processor boot mode, pcode waits for links to get to parameter exchange.
    - Pcode releases links to get to Normal operation (i.e. L0)
    - Pcode sets core Cstate to C1

- **Phase 3**: Reset execution (from core reset to fetch boot vector)
  - The starting assumptions are:
    - Before this phase starts, following information is provided to the core: APIC-ID, whether it's the BSP, SMT enable/disable, reset type (cold, warm, C6 exit).
    - Uncore necessary to the get to the BIOS and Intel TXT Address space is fully initialized.
  - In this phase:
    - Initialize core's internal structures, arrays, microarchitectural and architectural state.

- Execute MLC BIST if BIST enabled.
- Initialize uncore.
- Read LLC BIST results from the uncore and report it in the EAX register.
- Report LLC and MLC BIST results.
- The core and thread selected as package BSP fetches BIOS or goes to “Wait-for-SIPI” state
- The end assumption is there is at least one thread that was designated as package BSP.

➢ **Phase 4**: BIOS execution

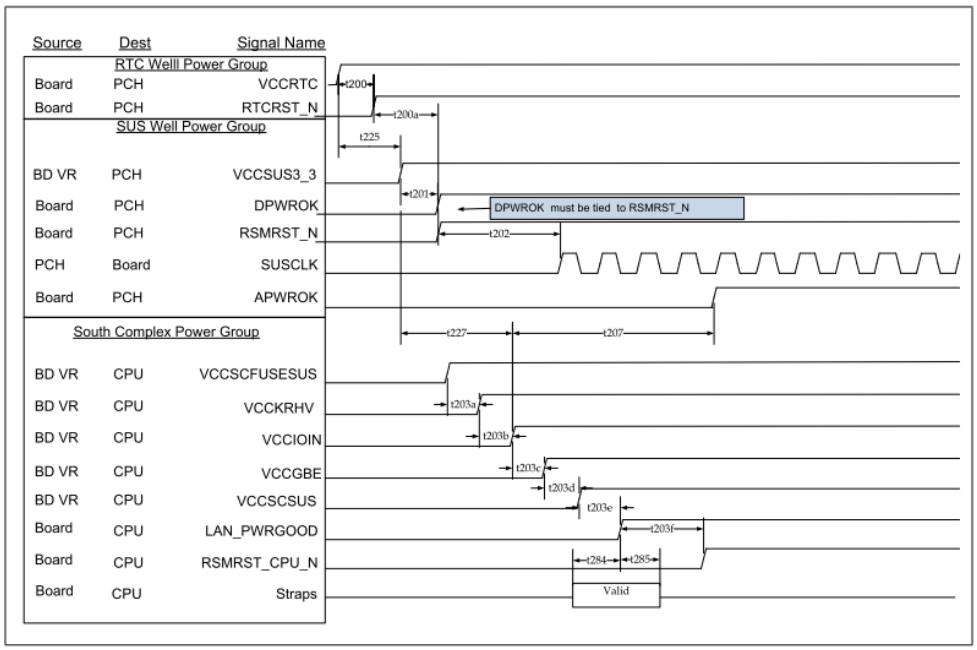


Figure 22. Power Sequencing Diagram G3 with RTC loss to S5

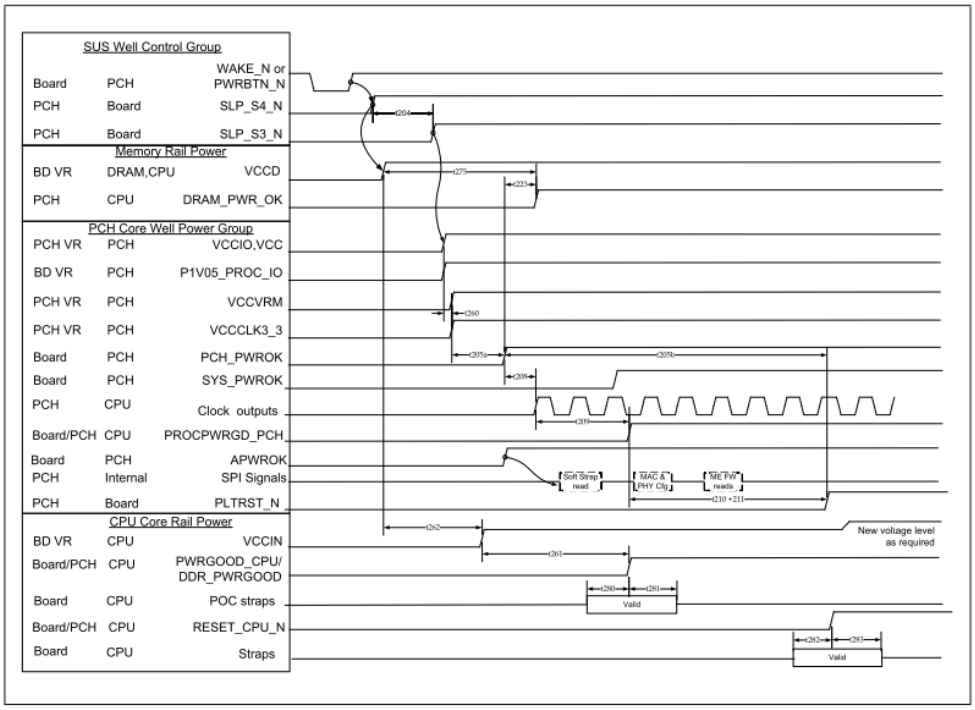


Figure 23. Power Sequencing Diagram S5 to S0

- BIOS has two flash memories (Flash 1/U1 and Flash 2/U31) to boot up from, the boot up sequence is same as phase 4.
- The relation of reset sequence and power on sequence:
  This relation can be described from different boot status.
  - Cold boot: When turning on the system after it has been powered off, the power on and reset sequence will be restarted.
  - Warm boot: When restarting the system without interrupting power, the power on sequence do not restart. Reset sequence differs from power on sequence.

2.2.2. PCH Strap pin definition

Table 11. PCH Strap definitions

Strap pin	Description	Default Value/Setting
SATA1GP/ GPIO19	This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 Reserved 1 1 SPI (default) 0 0 LPC	1

GPIO51	This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.	1
SATA3GP /GPIO37	0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).	0
MFG_MODE_STRAP	0 = Enable security measures defined in the Flash Descriptor. 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.	0
INTVRMEN	0 = DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source (should be connected to an external VRM). It should not pull the strap low. 1 = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left as No Connect.	1
GPIO62 / SUSCLK	0 = Disable PLL On-Die voltage regulator. 1 = Enable PLL On-Die voltage regulator.	1
DSWODVREN	0 = Disable Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This mode is only supported for testing environments. 1 = Enable DSW 3.3 V-to-1.05 V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards.	1
SPKR	0 = Disable “No Reboot” mode. 1 = Enable “No Reboot” mode (integrated PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.	
SATA2GP/GPIO36	0 = SoC RX is terminated to VSS. Grangeville platform only supports SoC Rx terminated to VSS. 1 = SoC RX is terminated to VCC/2.	0
GPIO33	0 = SoC TX is terminated to VSS. Grangeville platform only supports SoC Tx terminated to VSS 1 = SoC TX is terminated to VCC/2.	0
GPIO53	0 = SoC is in AC-coupling mode. Grangeville platform only supports AC-coupling mode. 1 = SoC is in DC-coupling mode.	0
GPIO55	0 = Enable “Top Swap” mode. This inverts an address on access to SPI and firmware hub, so the	1

	processor believes its fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64 KB blocks in the FWH or the appropriate address lines (A16, A17, A18, A19, or A20) as selected in Top-Swap Block size soft strap (handled through FITc. 1 = Disable “Top Swap” mode.	
GPIO8	This pin must not be driven low until after rising edge of RSMRST_N.	1
GPIO44	This pin must not be driven low until after rising edge of RSMRST_N.	1
GPIO46	This pin must not be driven low until after rising edge of RSMRST_N.	1
BIST_ENABLE	Build-in Self Test (BIST) enable strap: 0 = BIST Disable 1 = BIST Enable	0
BMCINIT	Integrated Service Processor Boot Mode Selection: 0 = Integrated Service Processor Boot Mode Disabled. 1 = Integrated Service Processor Boot Mode Enable	1
TXT_PLTEN	0 = The platform is not Intel TXT enabled. 1 = Default. The platform is Intel TXT enabled.	0
TXT_AGENT	0 = Default. The SoC is not the Intel TXT Agent. 1 = The SoC is the Intel TXT Agent.	0
SAFE_MODE_BOOT	0 = Safe Mode Boot Disabled 1 = Safe Mode Boot Enabled	1
DEBUG_EN_N	0 = Debug Mode 1 = Normal Mode	XDP_PRESENT_N
DDR3_4_STRAP	Select between DDR4 and DDR3 0 = DDR3, it requires <1K ohm pull down in order to out drive the internal pull up. 1= DDR4 (Default)	1
PECI0 ; PECI1 ; PECI2	In micro-server design space, there will be multiple sockets that share a PECI bus. However these sockets are effectively independent agents. The PECI IDs are used as straps to identify which socket is which in order for PECI bus to work.	000
LAN_MDIO_DIR_CTL_0; LAN_MDIO_DIR_CTL_1	00 = Both LAN ports are disabled. Note: In this mode manageability is not functional and must not be enabled in NVM control word 1. 01 = Port 1 is disabled. Port 0 is enabled.	11

	10 = Reserved 11 = Both Port 0 and 1 are enabled. Recommend 5.1K ohm pull up to VCCIOIN or 5.1K ohm pull down to GND.	
RSVD12_AJ67	This pin should have a 5.1K ohm pull down to GND.	0
RSVD11_AG67	This pin should have a 5.1K ohm pull down to GND.	0
RSVD10_AN78	This pin should have a 5.1K ohm pull down to GND.	0
RSVD09_AC64	This pin should have a 5.1K ohm pull down to GND.	0
SERIRQ_DIR	Recommend 5.1k ohm pull up to VCCIOIN.	1
UART_TXD[0]	Recommend 5.1k ohm pull down to GND.	0
UART_TXD[1]	Controls the security attributes on the NVM - for pre-production usage only. 0 = Disable NVM Security (Default) 1 = Security Enabled Recommend 5.1K ohm pull down to GND.	0
LAN_NCSI_RXD0	Recommend 5.1K ohm pull up to VCCIOIN.	1
LAN_NCSI_RXD1	Enable/Disable manageability traffic: 0 = LAN available in S5 for WoL (Default) 1 = LAN not available in S5. Manageability is disabled. Recommend 5.1K ohm pull down to GND.	0
LAN_NCSI_ARB_OUT	Selects SVID VR Operating Mode 1 - VCCSCSUS, P1V05_PCH, VCCGBE, VCCIOIN are combined into one SVID controlled supply. 0 - Separate SVID controllers (default).	1
RSVD84	49.9Ω 1% to GND	0
RSVD93	1k - 5.1kΩ to GND	0
RSVD94	1k - 5.1kΩ to GND	0
RSVD00	1k - 5.1kΩ to VCC3_3	1
RSVD18	1k - 5.1kΩ to GND	0
RSVD16	1k - 5.1kΩ to GND	0
RSVD17	1k - 5.1kΩ to GND	0
RSVD21	1k - 5.1kΩ to GND	0
NCTF/TP	1k - 5.1kΩ to VCC3_3	1

2.3. Memory Mapping

Broadwell-DE SoC contains registers that are located in the processor I/O space and memory space and sets of PCI configuration registers that are located in PCI configuration space. This chapter describes Broadwell-DE SoC I/O and memory maps at the register-set level. Register access is also described.

Table 12. PCI devices and functions

Bus:Device:Function	Function Description
Bus0:Device31:Function0	LPC controller
Bus0:Device31:Function2	SATA controller #1
Bus0:Device31:Function3	SMBus controller
Bus0:Device31:Function5	SATA controller#2
Bus0:Device31:Function6	Thermal subsystem
Bus0:Device29:Function0	USB EHCI controller#1
Bus0:Device28:Function0	PCI-e port1
Bus0:Device28:Function1	PCI-e port2
Bus0:Device28:Function2	PCI-e port3
Bus0:Device28:Function3	PCI-e port4
Bus0:Device28:Function4	PCI-e port5
Bus0:Device28:Function5	PCI-e port6
Bus0:Device28:Function6	PCI-e port7
Bus0:Device28:Function7	PCI-e port8
Bus0:Device25:Function0	Gigabit Ethernet controller
Bus0:Device22:Function0	Intel management engine interface#1
Bus0:Device22:Function1	Intel management engine interface#2
Bus0:Device22:Function2	IDE-R
Bus0:Device22:Function3	KT
Bus0:Device20:Function0	xHCI controller

Table 13. Fixed I/O ranges decoded by Broadwell-DE

I/O Address	Read Target	Write Target	Internal Unit
00h-08h	DMA controller	DMA controller	DMA
09h-0Eh	reserved	DMA controller	DMA
0Fh	DMA controller	DMA controller	DMA
10h-18h	DMA controller	DMA controller	DMA
19h-1Eh	reserved	DMA controller	DMA
1Fh	DMA controller	DMA controller	DMA
20h-21h	Interrupt controller	Interrupt controller	interrupt
24h-25h	Interrupt controller	Interrupt controller	interrupt
28h-29h	Interrupt controller	Interrupt controller	interrupt
2Ch-2Dh	Interrupt controller	Interrupt controller	interrupt
2Eh-2Fh	LPC SIO	LPC SIO	Forwarded to LPC
30h-31h	Interrupt controller	Interrupt controller	interrupt
34h-35h	Interrupt controller	Interrupt controller	interrupt
38h-39h	Interrupt controller	Interrupt controller	interrupt
3Ch-3Dh	Interrupt controller	Interrupt controller	interrupt
40h-42h	Timer/Counter	Timer/Counter	PIT
43h	reserved	Timer/Counter	PIT
4Eh-4Fh	LPC SIO	LPC SIO	Forwarded to LPC
50h-52h	Timer/Counter	Timer/Counter	PIT
53h	reserved	Timer/Counter	PIT
60h	microcontroller	microcontroller	Forwarded to LPC

61h	NMI controller	NMI controller	Processor I/F
62h	microcontroller	microcontroller	Forwarded to LPC
64h	microcontroller	microcontroller	Forwarded to LPC
66h	microcontroller	microcontroller	Forwarded to LPC
70h	reserved	NMI and RTC controller	RTC
71h	RTC controller	RTC controller	RTC
72h	RTC controller	NMI and RTC controller	RTC
73h	RTC controller	RTC controller	RTC
74h	RTC controller	NMI and RTC controller	RTC
75h	RTC controller	RTC controller	RTC
76h	RTC controller	NMI and RTC controller	RTC
77h	RTC controller	RTC controller	RTC
80h	DMA controller, LPC, PCI or PCIe	DMA controller, LPC, PCI or PCIe	DMA
81h-83h	DMA controller	DMA controller	DMA
84h-86h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
87h	DMA controller	DMA controller	DMA
88h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
89h-8Bh	DMA controller	DMA controller	DMA
8Ch-8Eh	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
8Fh	DMA controller	DMA controller	DMA
90h-91h	DMA controller	DMA controller	DMA
92h	Reset generator	Reset generator	Processor I/F
93h-9Fh	DMA controller	DMA controller	DMA
A0h-A1h	Interrupt controller	Interrupt controller	interrupt
A4h-A5h	Interrupt controller	Interrupt controller	interrupt
A8h-A9h	Interrupt controller	Interrupt controller	interrupt
ACh-ADh	Interrupt controller	Interrupt controller	interrupt
B0h-B1h	Interrupt controller	Interrupt controller	interrupt
B2h-B3h	Power management	Power management	Power management
B4h-B5h	Interrupt controller	Interrupt controller	interrupt
B8h-B9h	Interrupt controller	Interrupt controller	interrupt
BCh-BDh	Interrupt controller	Interrupt controller	interrupt
C0h-D1h	DMA controller	DMA controller	DMA
D2h-DDh	reserved	DMA controller	DMA
DEh-DFh	DMA controller	DMA controller	DMA
F0h	Ferr#/interrupt controller	Ferr#/interrupt controller	Processor I/F
170h-177h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
1F0h-1F7h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
200h-207h	Gameport low	Gameport low	Forwarded to LPC

208h-20Fh	Gameport high	Gameport high	Forwarded to LPC
376h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
3F6h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
4D0h-4D1h	Interrupt controller	Interrupt controller	interrupt
CF9h	Reset generator	Reset generator	Processor I/F

Table 14. Variable I/O decode ranges

Range name	Mappable	Size (bytes)	Target
ACPI	Anywhere in 64KB I/O space	64	Power management
IDE bus master	Anywhere in 64KB I/O space	1. 16 or 32 2. 16	1. SATA host controller #1, #2 2. IDE-R
Native IDE command	Anywhere in 64KB I/O space	8	1. SATA host controller #1, #2 2. IDE-R
Native IDE control	Anywhere in 64KB I/O space	4	1. SATA host controller #1, #2 2. IDE-R
SATA index/data pair	Anywhere in 64KB I/O space	16	1. SATA host controller #1, #2 2. IDE-R
SMBus	Anywhere in 64KB I/O space	32	SMB unit
TCO	96 bytes above ACPI base	32	TCO unit
GPIO	Anywhere in 64KB I/O space	128	GPIO unit
Parallel port	3 ranges in 64KB I/O space	8	LPC peripheral
Serial port 1	8 ranges in 64KB I/O space	8	LPC peripheral
Serial port 2	8 ranges in 64KB I/O space	8	LPC peripheral
Floppy disk controller	2 ranges in 64KB I/O space	8	LPC peripheral
LAN	Anywhere in 64KB I/O space	32	LAN unit
LPC generic 1	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 2	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 3	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 4	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
I/O trapping ranges	Anywhere in 64KB I/O space	1 to 256	Trap on backbone
PCI bridge	Anywhere in 64KB I/O space	I/O base/limit	PCI bridge
PCI-E root ports	Anywhere in 64KB I/O space	I/O base/limit	PCI-E root ports 1-8
KT	Anywhere in 64KB I/O space	8	KT

Table 15. Memory decode ranges from processor perspective

Memory range	target	Dependency/comments
0000 0000h-000D FFFFh 0010 0000h-TOM	Main memory	TOM registers in host controller
000E 0000h-000E FFFFh	LPC or SPI	Bit 6 in BIOS decode enable register is set
000F 0000h-000F FFFFh	LPC or SPI	Bit 7 in BIOS decode enable register is set
FEC_ _000h-FEC_ _040h	IOx APCI inside broadwell-de SoC	_ _ is controlled using APIC range select (ASEL) field and APIC enable (AEN) bit.
FEC1 0000h-FEC1 7FFFh	PCI-E port 1	PCI-E root port 1 I/OxAPIC enable (PAE) set
FEC1 8000h-FEC1 FFFFh	PCI-E port 2	PCI-E root port 2 I/OxAPIC enable (PAE) set
FEC2 0000h-FEC2 7FFFh	PCI-E port 3	PCI-E root port 3 I/OxAPIC enable (PAE) set
FEC2 8000h-FEC2 FFFFh	PCI-E port 4	PCI-E root port 4 I/OxAPIC enable (PAE) set
FEC3 0000h-FEC3 7FFFh	PCI-E port 5	PCI-E root port 5 I/OxAPIC enable (PAE) set
FEC3 8000h-FEC3 FFFFh	PCI-E port 6	PCI-E root port 6 I/OxAPIC enable (PAE) set
FEC4 0000h-FEC4 7FFFh	PCI-E port 7	PCI-E root port 7 I/OxAPIC enable (PAE) set
FEC4 8000h-FEC4 FFFFh	PCI-E port 8	PCI-E root port 8 I/OxAPIC enable (PAE) set
FFC0 0000h-FFC7 FFFFh FF80 0000h- FF87 FFFFh	LPC or SPI (or PCI)	Bit 8 in BIOS decode enable register is set
FFC8 0000h-FFCF FFFFh FF88 0000h- FF8F FFFFh	LPC or SPI (or PCI)	Bit 9 in BIOS decode enable register is set
FFD0 0000h-FFD7 FFFFh FF90 0000h- FF97 FFFFh	LPC or SPI (or PCI)	Bit 10 in BIOS decode enable register is set
FFD8 0000h-FFDF FFFFh FF98 0000h- FF9F FFFFh	LPC or SPI (or PCI)	Bit 11 in BIOS decode enable register is set
FFE0 0000h-FFE7 FFFFh FFA0 0000h- FFA7 FFFFh	LPC or SPI (or PCI)	Bit 12 in BIOS decode enable register is set
FFE8 0000h-FFEF FFFFh FFA8 0000h- FFAF FFFFh	LPC or SPI (or PCI)	Bit 13 in BIOS decode enable register is set
FFF0 0000h-FFF7 FFFFh FFB0 0000h-FFB7 FFFFh	LPC or SPI (or PCI)	Bit 14 in BIOS decode enable register is set
FFF8 0000h–FFFF FFFFh FFB8 0000h–FFBF FFFFh	LPC or SPI (or PCI)	Always enabled. The top two 64KB blocks of this range can be swapped.
FF70 0000h–FF7F FFFFh FF30 0000h–FF3F FFFFh	LPC or SPI (or PCI)	Bit 3 in BIOS Decode Enable register is set
FF60 0000h–FF6F FFFFh FF20 0000h–FF2F FFFFh	LPC or SPI (or PCI)	Bit 2 in BIOS Decode Enable register is set
FF50 0000h–FF5F FFFFh FF10 0000h–FF1F FFFFh	LPC or SPI (or PCI)	Bit 1 in BIOS Decode Enable register is set
FF40 0000h–FF4F FFFFh FF00 0000h–FF0F FFFFh	LPC or SPI (or PCI)	Bit 0 in BIOS Decode Enable register is set
128 KB anywhere in 4 GB range	Integrated LAN Controller	Enable using BAR in D25:F0 (Integrated LAN Controller MBARA)
4 KB anywhere in 4 GB range	Integrated LAN Controller	Enable using BAR in D25:F0 (Integrated LAN Controller MBARB)
1 KB anywhere in 4 GB range	USB EHCI Controller #1	Enable using standard PCI mechanism

		(D29:F0)
64 KB anywhere in 4 GB range	USB xHCI Controller	Enable using standard PCI mechanism (D20:F0)
FED0 X000h–FED0 X3FFh	High Precision Event Timers	BIOS determines “fixed” location which is one of four, 1-KB ranges where X (in the first column) is 0h, 1h, 2h, or 3h.
FED4 0000h–FED4 FFFFh	TPM on LPC	None
Memory Base/Limit anywhere in 4 GB range	PCI Bridge	Enable using standard PCI mechanism (D30:F0)
Prefetchable Memory Base/Limit anywhere in 64-bit address range	PCI Bridge	Enable using standard PCI mechanism (D30:F0)
64 KB anywhere in 4 GB range	LPC	LPC Generic Memory Range. Enable using setting bit[0] of the LPC Generic Memory Range register (D31:F0:offset 98h).
32 Bytes anywhere in 64-bit address range	SMBus	Enable using standard PCI mechanism (D31:F3)
2 KB anywhere above 64 KB to 4 GB range	SATA Host Controller #1	AHCI memory-mapped registers. Enable using standard PCI mechanism (D31:F2)
Memory Base/Limit anywhere in 4 GB range	PCI Express* Root Ports 1-8	Enable using standard PCI mechanism (D28: F 0-7)
Prefetchable Memory Base/Limit anywhere in 64-bit address range	PCI Express Root Ports 1-8	Enable using standard PCI mechanism (D28:F 0-7)
4 KB anywhere in 64-bit address range	Thermal Reporting	Enable using standard PCI mechanism (D31:F6 TBAR/ TBARH)
4 KB anywhere in 64-bit address range	Thermal Reporting	Enable using standard PCI mechanism (D31:F6 TBARB/TBARBH)
16 Bytes anywhere in 64-bit address range	Intel® MEI #1, #2	Enable using standard PCI mechanism (D22:F 1:0)
4 KB anywhere in 4 GB range	KT	Enable using standard PCI mechanism (D22:F3)
16 KB anywhere in 4 GB range	Root Complex Register Block (RCRB)	Enable using setting bit[0] of the Root Complex Base Address register (D31:F0:offset F0h).

2.4. RAM

The Intel Broadwell-DE CPU family can support memory DDR3 and DDR4 that need via strap pin DDR3_4_STRAP to configure which one be supported.

Currently the board supports two DDR4 SODIMM modules with ECC, so the DDR3_4_STRAP should be pull to high.

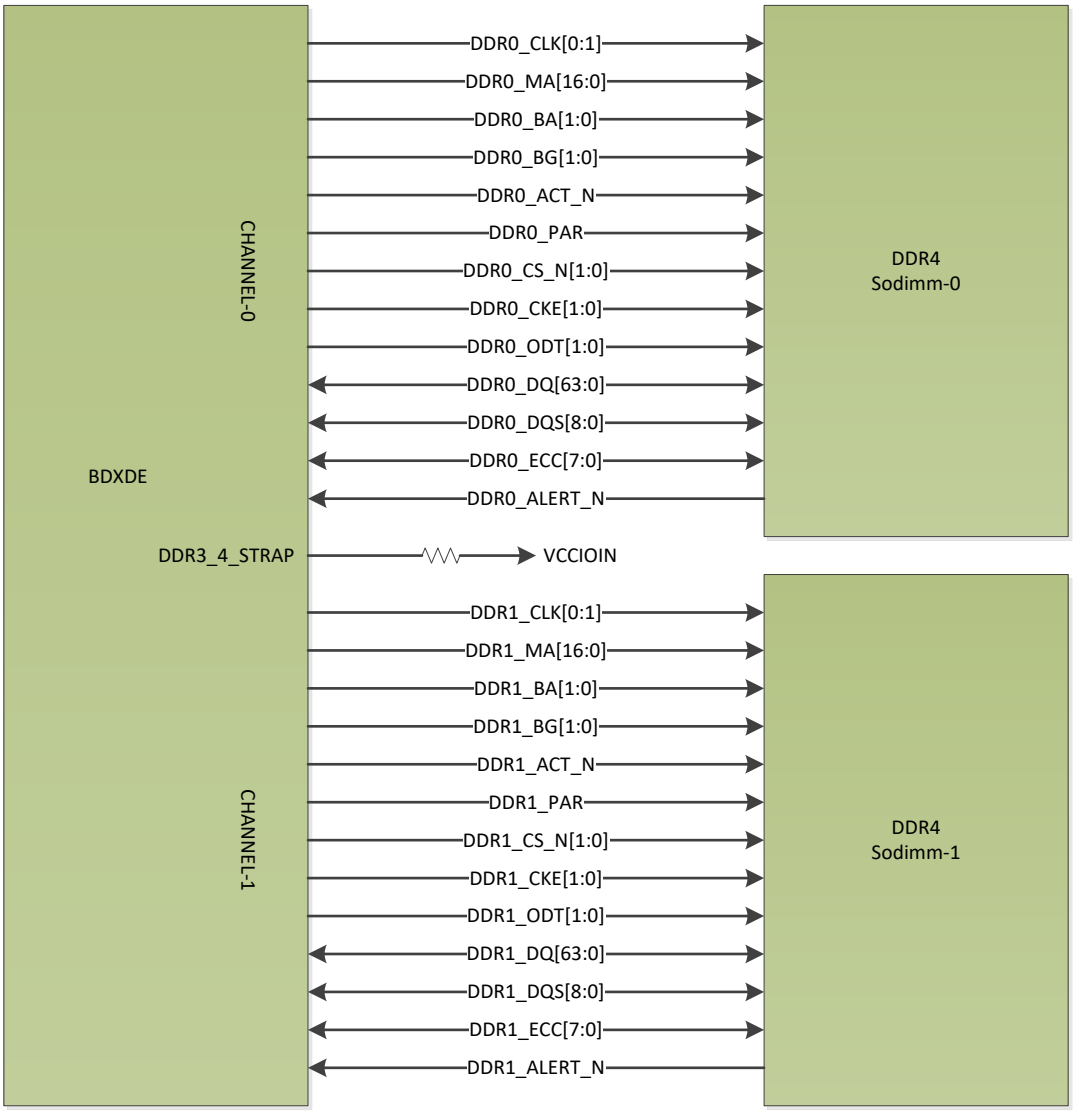


Figure 24. RAM Connection

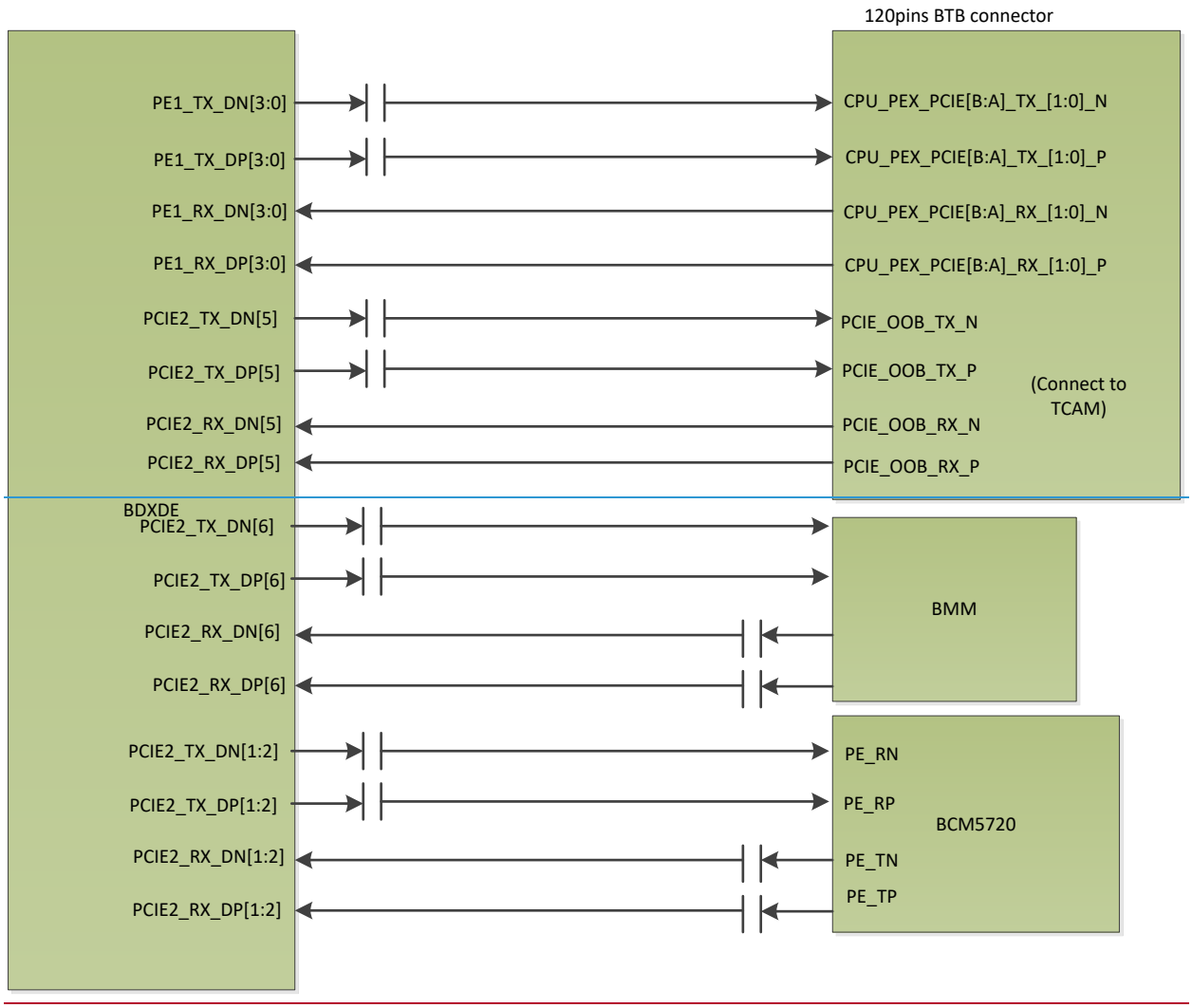
2.5. PCIe

The CPU board provides the x4 PCIE Gen3 and connect to the PCI-E Switch PEX8724.

There are other PCIE GEN2 that connect to BMC module.

The PCIE interface connected to Intel I210 is PCIE GEN2 x2.

The PCIE interface connected to BMC module is PCIE GEN2 x1.


120pins BTB connector
PE1_TX_DN[3:0]
PE1_TX_DP[3:0]
PE1_RX_DN[3:0]
PE1_RX_DP[3:0]
PCIE2_TX_DN[5]
PCIE2_TX_DP[5]
PCIE2_RX_DN[5]
PCIE2_RX_DP[5]
CPU_PEX_PCIE[B:A]_TX_[1:0]_N
CPU_PEX_PCIE[B:A]_TX_[1:0]_P
CPU_PEX_PCIE[B:A]_RX_[1:0]_N
CPU_PEX_PCIE[B:A]_RX_[1:0]_P
PCIE_OOB_TX_N
PCIE_OOB_TX_P
PCIE_OOB_RX_N
PCIE_OOB_RX_P
(Connect to TCAM)
BDXDE
PCIE2_TX_DN[6]
PCIE2_TX_DP[6]
PCIE2_RX_DN[6]
PCIE2_RX_DP[6]
BMM
PCIE2_TX_DN[1:2]
PCIE2_TX_DP[1:2]
PCIE2_RX_DN[1:2]
PCIE2_RX_DP[1:2]
PE_RN
PE_RP
PE_TN
PE_TP
BCM5720

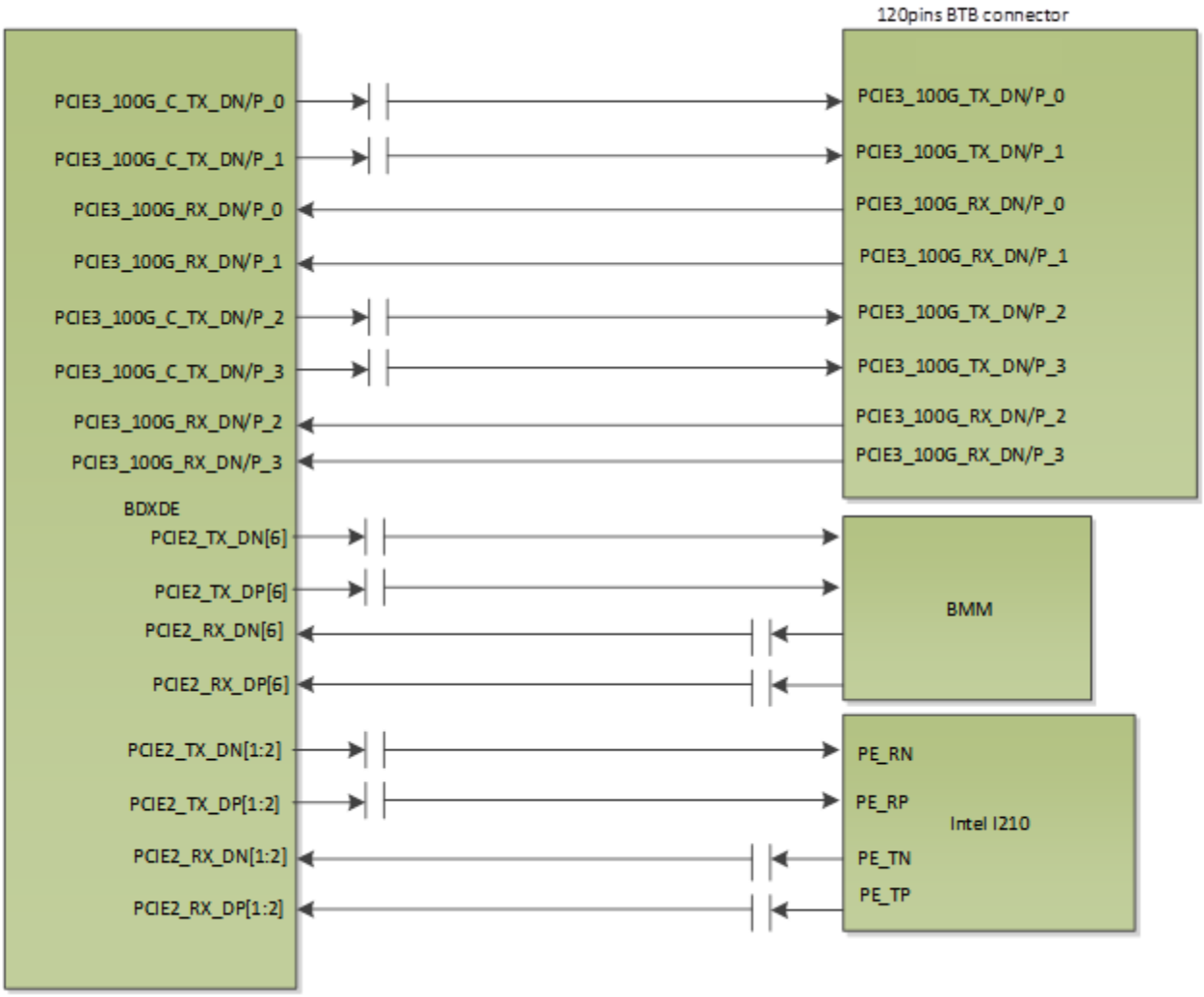


Figure 25. PCIe Topology

2.6. SMbus

The SMbus from Broadwell-DE can access the CPU board and main board device via SMBUS0.

The U40/U41 multiplexers are used to prevent multi-master issues on the SMBUS.

The BMC module could use the SMBUS when the I2C_multiplexer_select pin is driven from high to low.

In order to prevent the hang-up issue which occurred when the CPU is accessing the SMBUS and BMC module want to take the bus master (I2C_multiplexer_select would be driven low), if the BMC module is installed, BMC would be the master for all SMBUS, CPU would ask BMC for SMBUS information via LPC by IPMI.

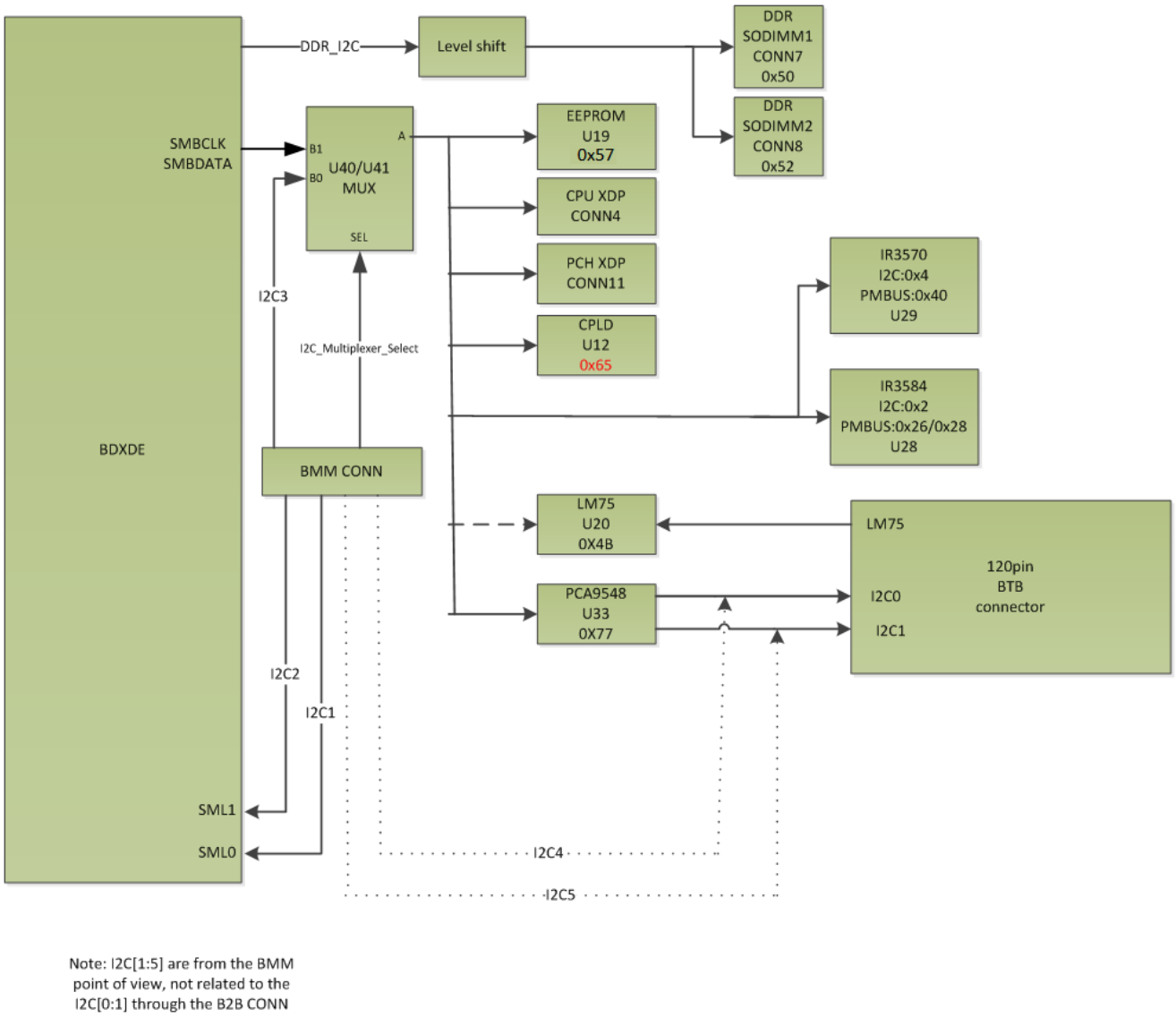


Figure 26. SMBUS Connection

Table 16. SMBus 0 Address Table

Device	I2C address	Note
DDR4 SODIMM 1	0x50	Need to be accessed by DDR_I2C interface
DDR4 SODIMM 2	0x52	Need to be accessed by DDR_I2C interface
LM75	0x4B	Need to be accessed by main board CPLD Not display at SMBus 0.
EEPROM	0x57	For R1 CPU board
IR3584 (I2C)	0x02	
IR3584 (PMBUS-Loop1)	0x26	

IR3584 (PMBus-Loop2)	0x28	
IR3570 (I2C)	0x4	
IR3570 (PMBus Loop1)	0x42	
PCA9548	0X77	

2.7. UART

There are two UART interfaces of Broadwell-DE CPU, UART0 and UART1.

UART0 is the main system console and connect to main board through 120pin connector and BMC via CPLD, the reason is to support the SOL function when BMC is present.

UART1 is the reserved UART interface and directly connect to BMC module.

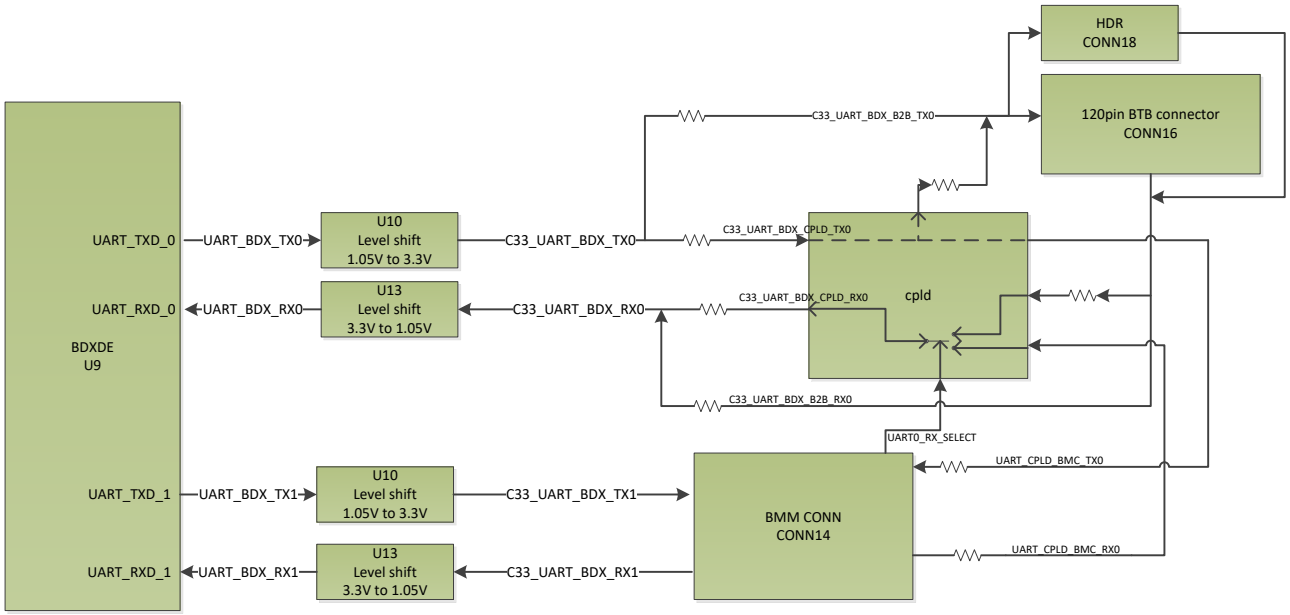


Figure 27. UART Connector

Table 17. CONN18 PIN ASSIGNMENT

Pin Number	Description
1	VCC
2	TX
3	RX
4	GND

2.8. USB

There are three USB 2.0 interfaces in the project.

- The USB-0 via the 120pins BTB connector to switch board is for chassis USB connector.
- The USB-1 is for debug function.
- The USB-3 is connected to BMC module for vMEDIA function.

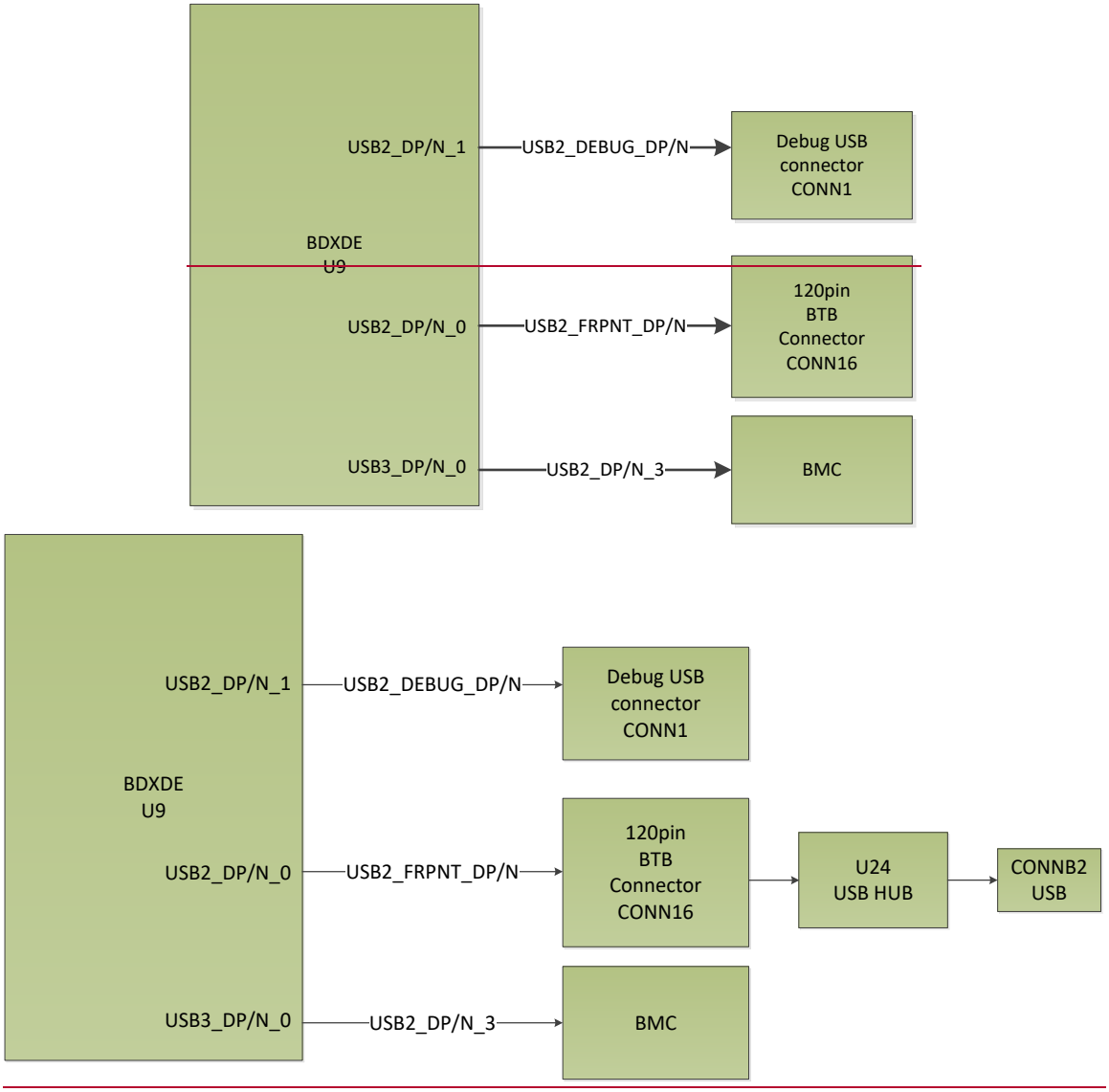


Figure 28. USB Connection

2.9. SATA

The CPU board supports 1 SATA SSD devices via SATA 3.0 interface.

- SATA 3.0 CH0 support mSATA SSD module.

The following table shows the mSATA dimension and size.

Table 18. SATA SSD Module Table

Type	Dimension	Capacity
mSATA SSD	50.8mm x 29.85mm x 4.0mm	16GB~512GB (default)

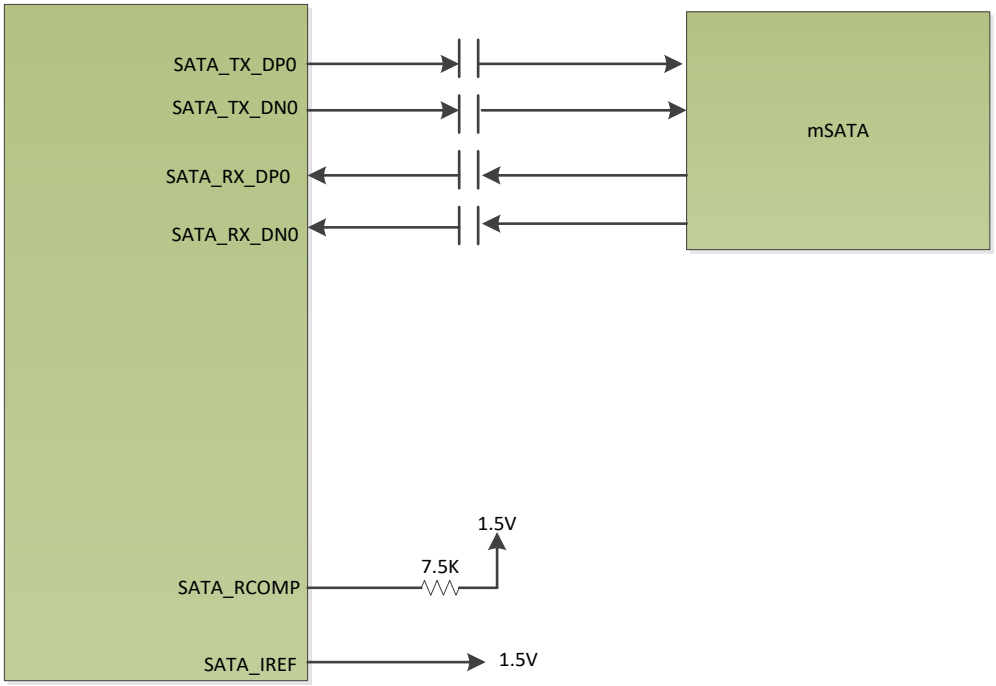


Figure 29. SATA Connection

2.10. GPIO

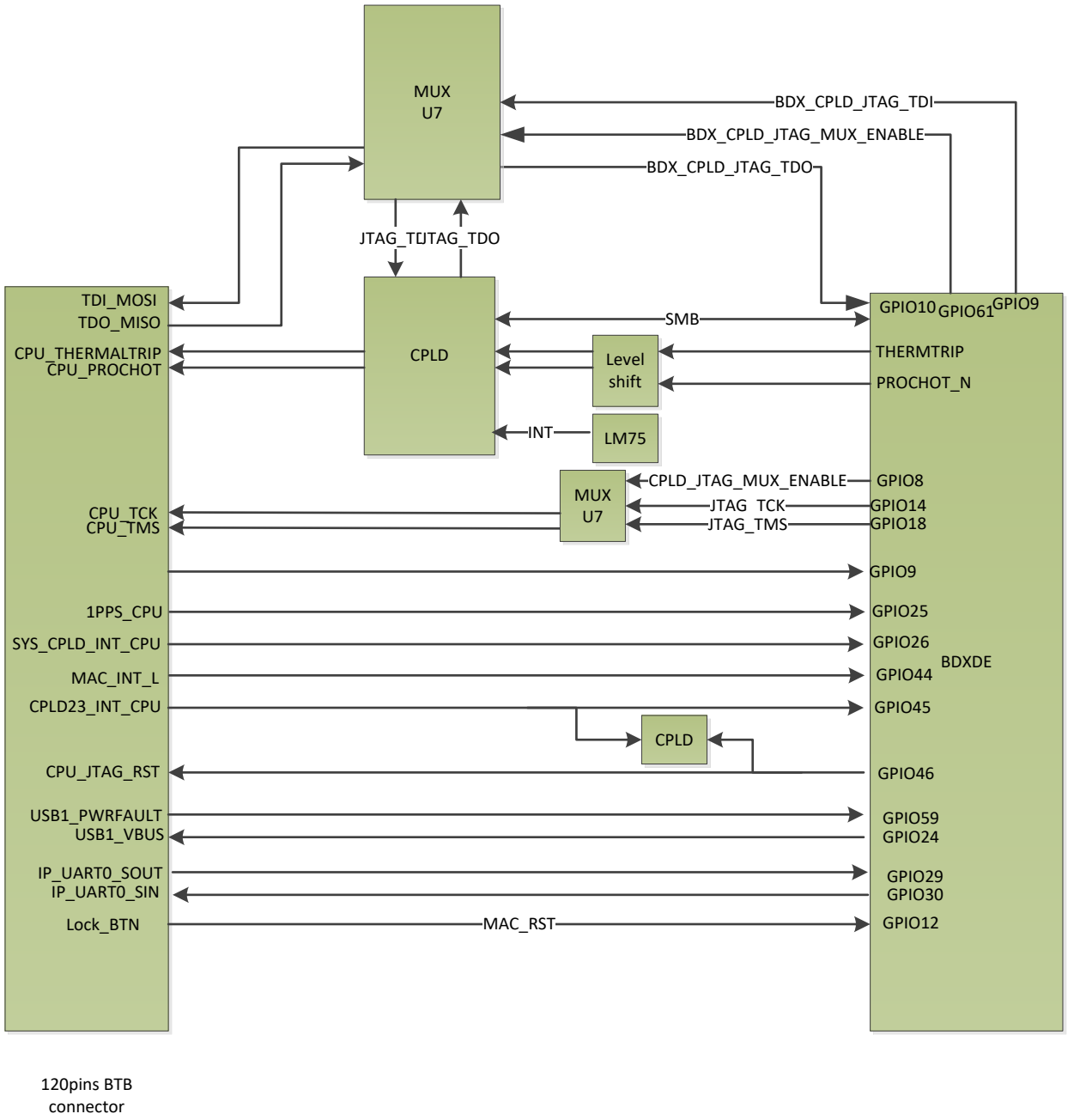


Figure 30. GPIO Connection

The following table is the GPIO function description of BDXDE CPU.

Table 19. GPIO table

Pin name	GPIO_USE_SEL 1: GPIO 0: Native	GPIO_IO_SEL 1: input 0: output	Function
GPIO0	0	X	BMBUSY#
GPIO1	1	0	Watch dog event clear indicator
GPIO2	0	X	NC
GPIO3	0	X	NC
GPIO4	1	1	CPU to PCH Throttle event interrupt
GPIO5	0	X	NC
GPIO6	1	0	JTAG enable, enable JTAG multiplexer to update CPLD code from CPU. 1: enable the JTAG multiplexer 0: disable the JTAG multiplexer
GPIO7	0	X	NC
GPIO8	1	0	JTAG Multiplexer select, which select the JTAG signals from CPU would go to CPLD or main board 1: to CPLD (default) 0: to Main board
GPIO9	1	0	XDP_NOA5_PCH/ BDX_CPLD_JTAG_TDI When configure to be BDX_CPLD_JTAG_TDI, which is CPU JTAG output
GPIO10	1	1	XDP_NOA6_PCH/ BDX_CPLD_JTAG_TDO When this pin configure to BDX_CPLD_JTAG_TDO , which is CPU JTAG input
GPIO11	0	X	SMBALERT#
GPIO12	1	0	Reset MAC, to do the sleep function.
GPIO14	1	0	XDP_NOA7_PCH/

			BDX_CPLD_JTAG_TCK
GPIO15	1	0	SOC_FPGA_CLK
GPIO16	1	0	FM_THROTTLE_PCH_N/ FM_THROTTLE_N
GPIO17	1	1	BMC present detect
GPIO18	1	0	XDP_NOA14_PCH/ BDX_CPLD_JTAG_TMS
GPIO19	1	BI-DIR	XDP_NOA9_PCH
GPIO20	1	0	FM_SMI_ACTIVE_PCH_N/ FM_SMI_ACTIVE_CPLD_N
GPIO21	1	BI-DIR	XDP_NOA8_PCH
GPIO22	1	0	SCLOCK
GPIO23	0	X	NC
GPIO24	0	0	NC
GPIO25	1	1	1PPS_CPU
GPIO26	1	1	SYS_CPLD_INT_CPU
GPIO27	1	1	SOC_FPGA_DIN
GPIO28	1	0	SOC_FPGA_DOUT
GPIO29	1	0	IP_UART0_SOUT
GPIO30	1	1	IP_UART0_SIN
GPIO31	1	1	SMB_PWR_ALERT
GPIO32	X	X	NC
GPIO33	X	X	NC
GPIO35	1	0	FM_NMI_EVENT_PCH_N/ FM_NMI_EVENT_CPLD_N
GPIO36	1	0	ADR_STATUS_RD
GPIO37	1	1	ADR_STATUS_CLR
GPIO38	0	0	SLOAD
GPIO39	0	0	SDATAOUT0
GPIO40	0	BI	XDP_NOA1_PCH
GPIO41	1	0	XDP_NOA2_PCH/ CPLD_CONFIG_CLK

GPIO42	1	BI	XDP_NOA3_PCH/ CPLD_CONFIG_DATA
GPIO43	1	0	XDP_NOA4_PCH / ADR_MCU_INIT
GPIO44	0	1	NC
GPIO45	1	1	CPLD23_INT_CPU
GPIO46	1	0	CPU_JTAG_RST
GPIO48	1	0	SDATAOUT1
GPIO49	1	0	FM_CPU_PROCHOT_PCH_N/ FM_PROCHOT_N
GPIO50	X	X	NC
GPIO51	1	1	4.7k pull to 3.3V
GPIO52	1	1	CPU_SV
GPIO53	1	1	1k pull to gnd
GPIO54	X	X	NC
GPIO55	1	1	FM_BIOS_RCRV_BOOT_N
GPIO57	1	1	FM_ME_RCRV_N
GPIO58	0	X	SML1_CLK
GPIO59	1	BI	XDP_NOA0_PCH
GPIO60	0	X	SML0ALERT#
GPIO61	X	X	NC
GPIO62	0	X	SUSCLK_33K
GPIO65	0	X	NC
GPIO67	0	X	NC
GPIO68	1	1	CPLD interrupt
GPIO69	0	X	NC
GPIO70	0	X	NC
GPIO71	0	X	NC
GPIO72	1	1	1K pull to 3.3V
GPIO74	0	X	SML1ALERT#/TEMP_ALERT#.
GPIO75	0	X	SML1DATA

2.11. CPLD

2.11.1. Power sequence

The most important function of the CPLD is to control the whole board power sequence based on the power sequence requirement of Intel Broadwell-DE.

CPLD would base on the power good signals from the VRs on the board and then drives the enable signals to enable the VRs.

The “PWROK” signals are used to indicate PCH and PCU of BDXDE that the related power are ok.

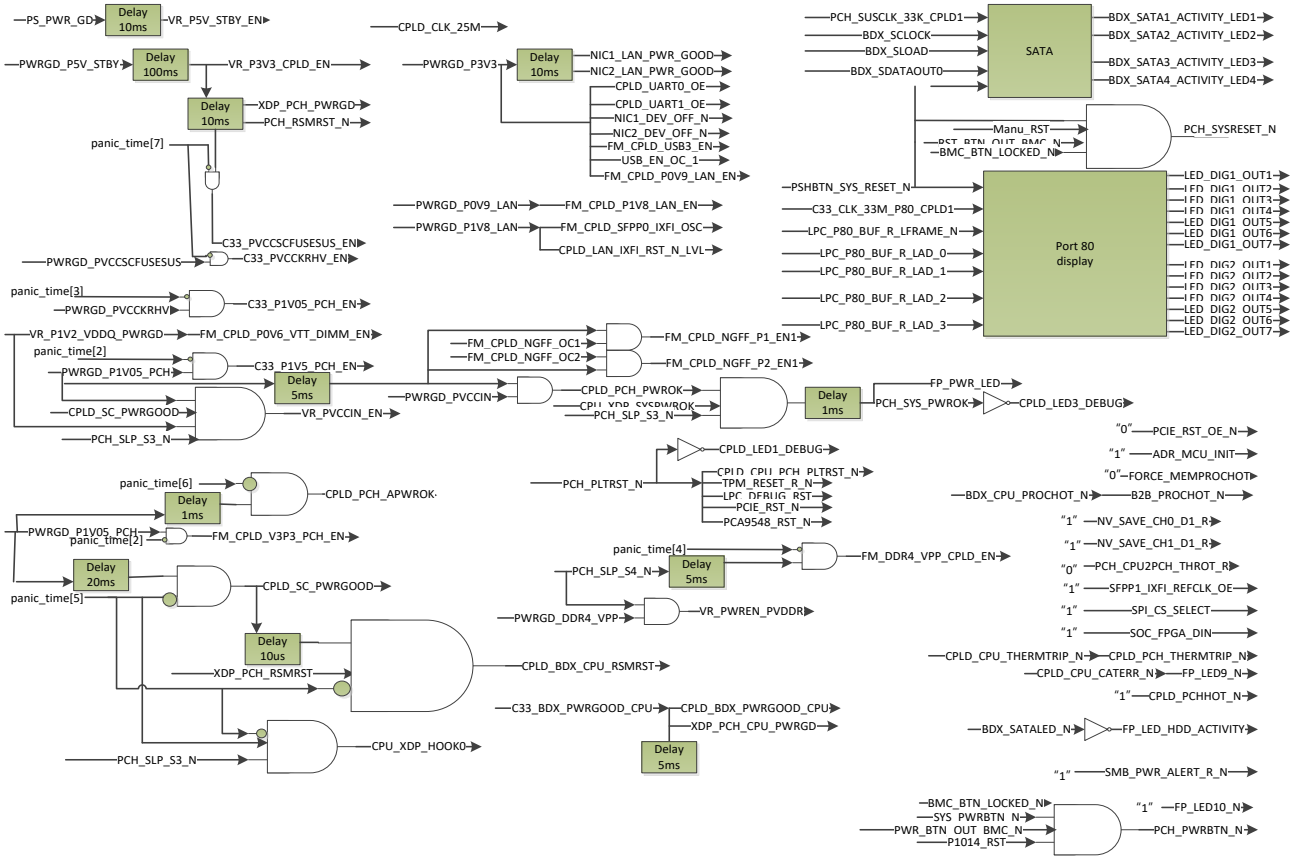


Figure 31. CPLD Block Diagram

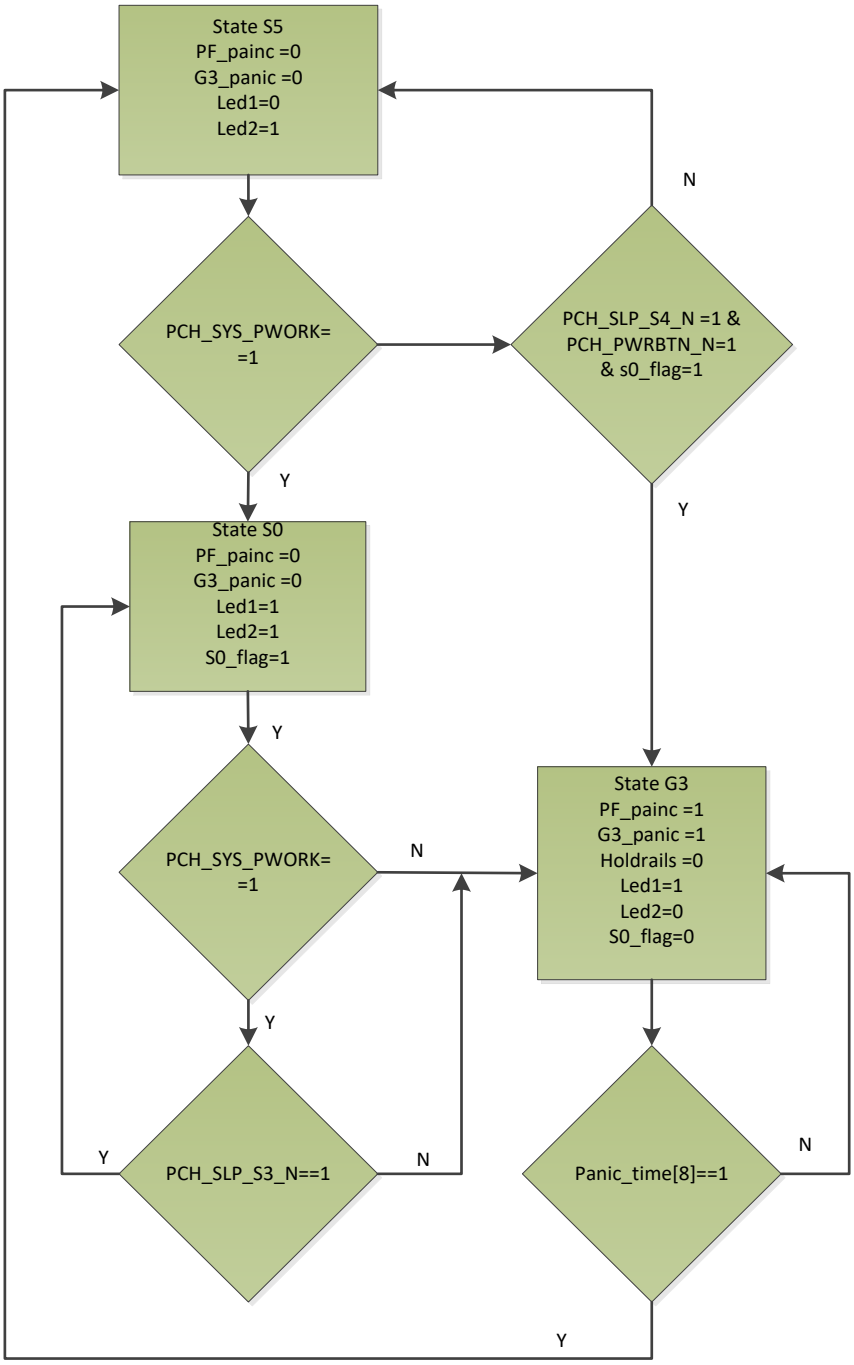


Figure 32. Power Sequence Flow Chat

2.11.2. Watch Dog

The watch dog block is used monitor that the system boot is successful or not. When CPU successful boot up and can go into OS, the CPU would drive "WATCHDOG_IND" to high

For watch dog enable and configuration, please check detail in CPU CPLD specification.

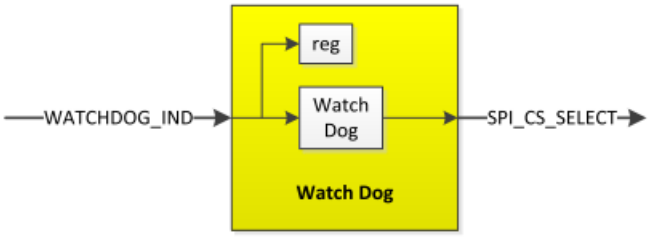


Figure 33. Watch Dog Block Diagram

2.11.3. JTAG

The JTAG interface of the CPU board is used to upgrade the CPLD via CPU in the whole chassis, including U12 on the CPU board, other CPLDs are on the main board and FAN board.

When the CPLD on the CPU board needs to be upgraded, the GPIO8 of Broadwell-DE needs to select to “1”, and the GPIO61 needs to select to “1”.

When the CPLD devices on the main board or FAN board need to be upgrade, GPIO8 of Broadwell-DE needs to select to “0”, and the GPIO61 needs to select to “0”.

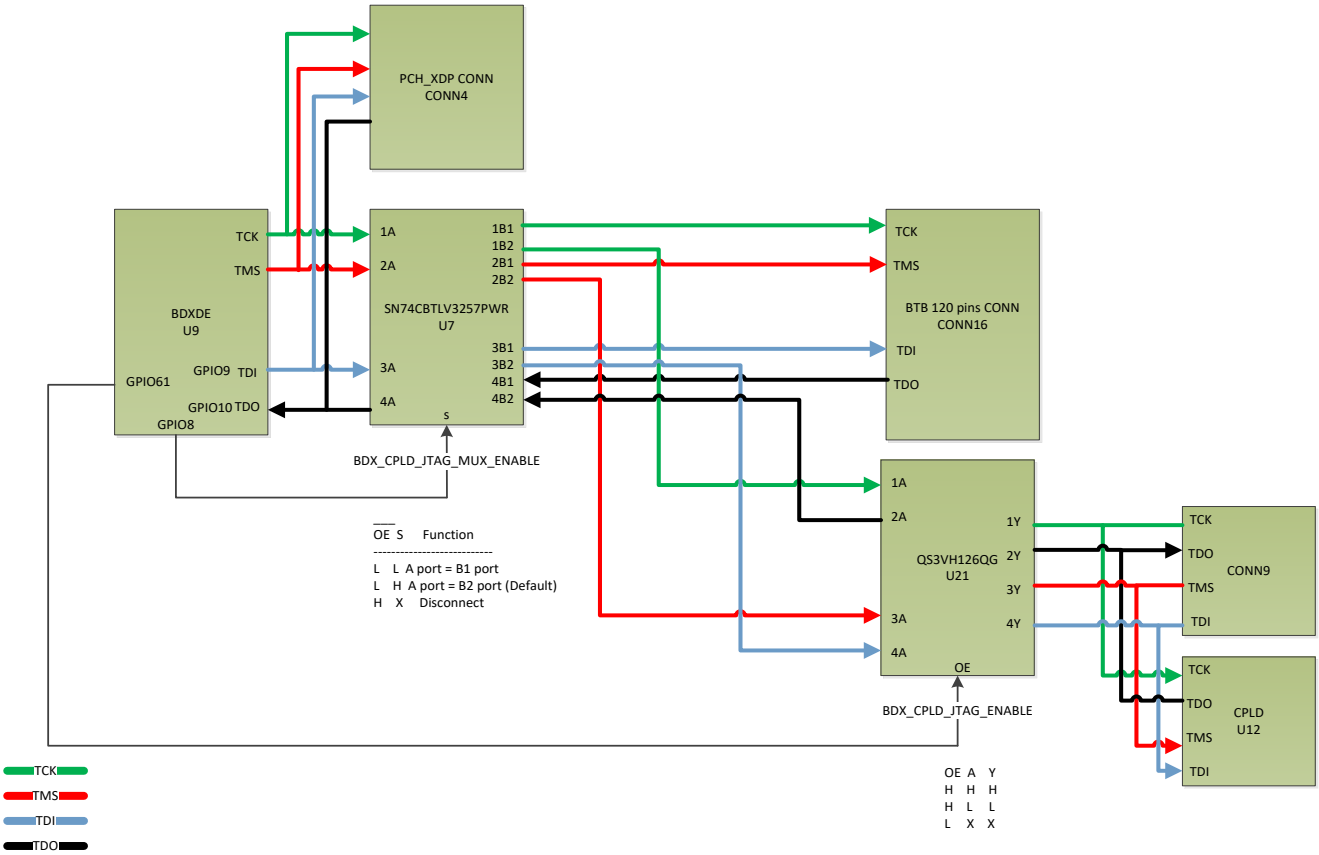


Figure 34. JTAG architecture

2.12. I210

The MAC sub-system is used for CPU to connect the management PHY (WGI210IS) on the main board, the Ethernet controller solution is Intel WGI210IS.

The I210 communicates CPU via PCIE GEN2 x1, and connect to the management port PHY MARVELL 88E1111 on the main board via SGMII interface.

The NCSI interface is used to connect the BMC module to support share NIC function.

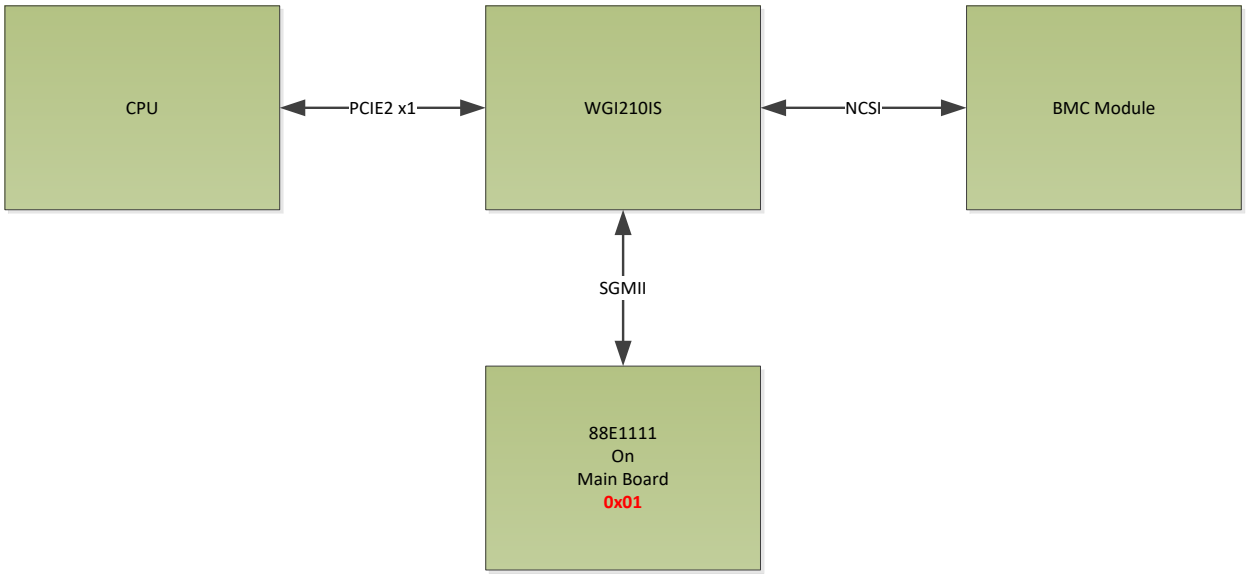


Figure 35. I210IS connection illustration

2.12.1. Feature

- Small package: 9 x 9 mm
- PCIe v2.1 (2.5 GT/s) x1, with Switching Voltage Regulator (iSVR)
- Integrated Non-Volatile Memory (iNVM)
- Platform Power Efficiency
  - IEEE 802.3az Energy Efficient Ethernet (EEE)
  - Proxy: ECMA-393 and Windows* logo for proxy offload
- Advanced Features:
  - 0 to 70 °C commercial temperature or -40 to 85 °C industrial temperature
  - Jumbo frames
  - Interrupt moderation, VLAN support, IP checksum offload
  - PCIe OBFF (Optimized Buffer Flush/Fill) for improved system power management
  - Four transmit and four receive queues
  - RSS and MSI-X to lower CPU utilization in multi-core systems
  - ECC – error correcting memory in packet buffers
  - Four Software Definable Pins (SDPs)
- Manageability:
  - NC-SI for greater bandwidth pass through
  - Flexible firmware architecture with secure Flash update
  - MCTP over PCIe
  - PXE and iSCSI boot

3. BMC Sub-system

The BMC is used for monitoring the system HW information including thermal, power, FAN and CPU status.

The BMC module would be installed in CONN14 on CPU board.

The following brief descriptions are for the interface between BMC module and CPU board in following sections.

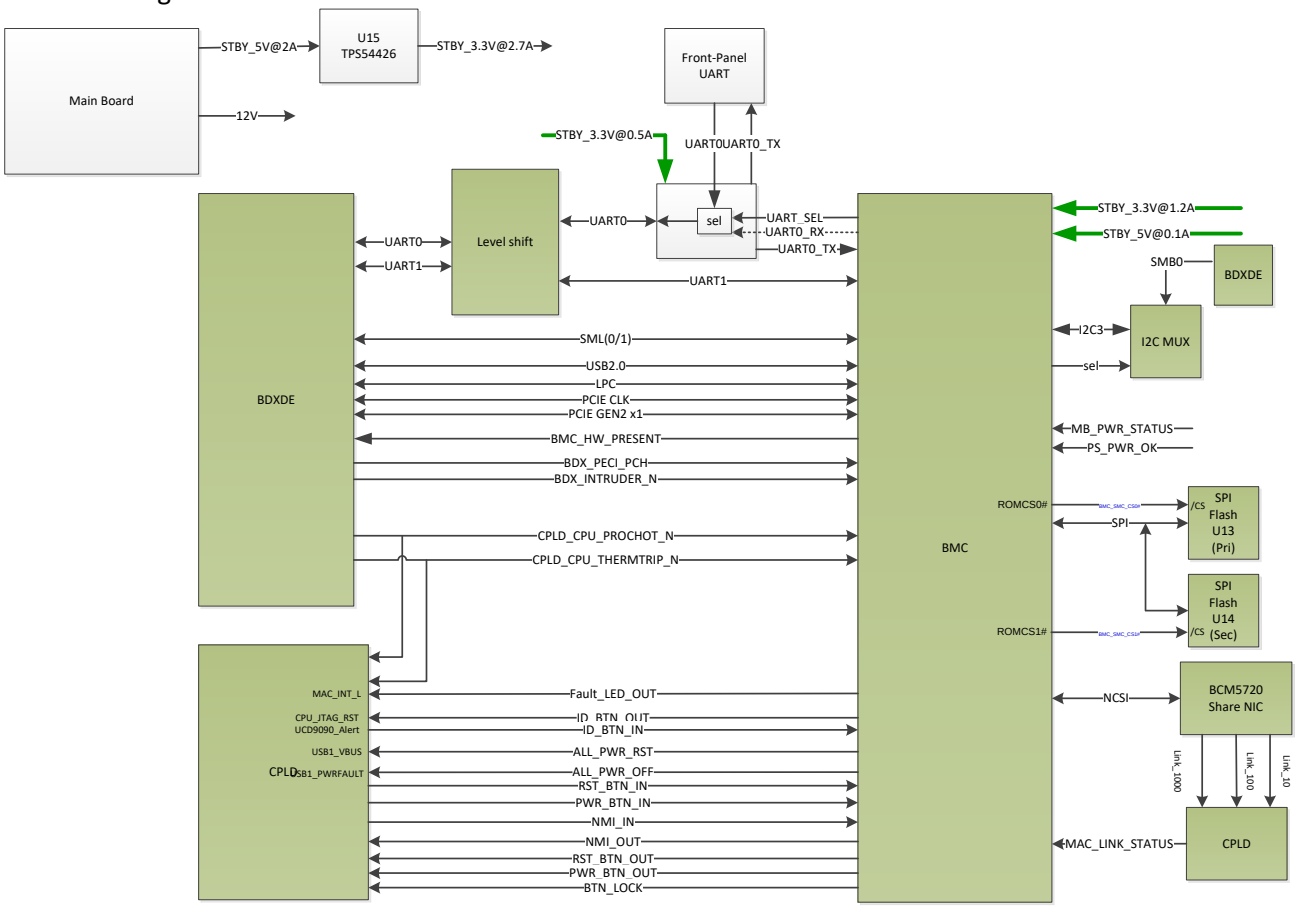


Figure 36. BMCM connection

3.1. LPC

The LPC interface is the main communication channel for CPU to get the whole system information from BMC via IPMI protocol, like SMBUS.

BMC would also listen the information from CPU via LPC, such as port 80 status and serial messages for SOL function.

3.2. SMBUS

In order to prevent the multi master hang-up issue, if BMC module is installed, the SMBUS host would change to BMC, not CPU.

When BMC is installed, the "I2C_Multiplexer_select" would be driven to low to let BMC be the only host on SMBUS.

CPU would change to via LPC to get the SMBUS information from BMC.

3.3. UART

The UART interface is used to achieve SOL function.

CPU UART0 is connected to BMC uart1 block, and is used for SOL.

If BMC want to send UART message to CPU via UART0 of CPU, "BMC_UART0_DIR_SEL" would be driven to "0" from "1".

4. Fan Sub-system

Fan tray

The AS7926-40/80K utilizes fan modules from Invni model # PF60761BX-Q120-S99. Information is provided below:

LED

A single LED is provided on each fan module to indicate status

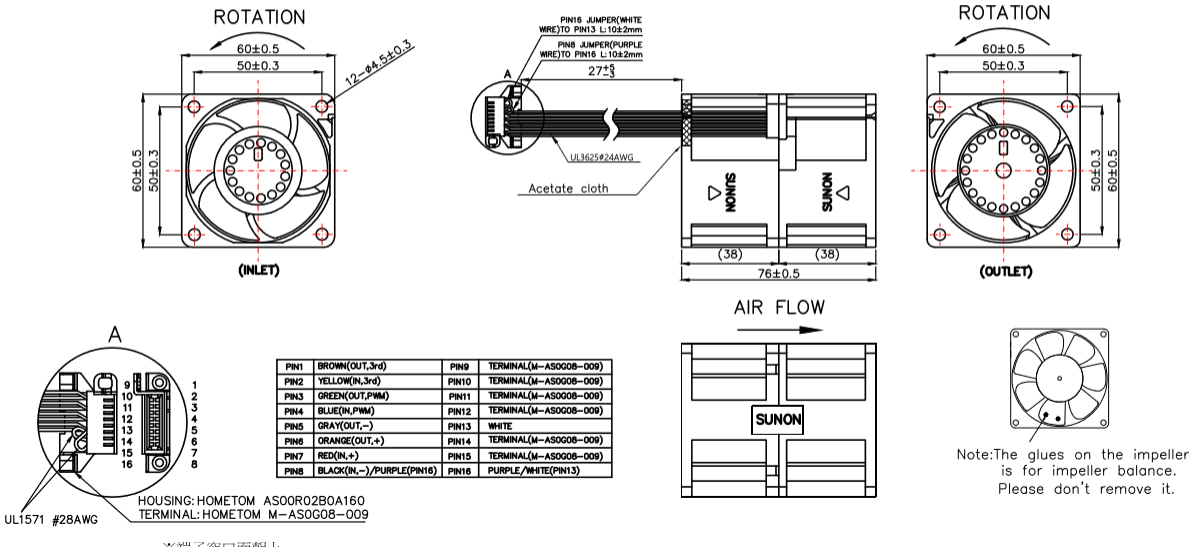
Green – Power functioning normally

Amber – Power fan fault

Off – No power

RATED SPEED	**20800/17900 RPM ± 10% at rated voltage**
AIR FLOW	**86.1 CFM**
STATIC PRESSURE	**5.55 Inch-H_2O**
ACOUSTIC NOISE	**72.8 dB(A)**

Screw Type (Pan head)	Torque	Screw Spec	
		Size	Standard
Machine screw	3~4 Kgf-cm	M4.0	JIS B1111-1974
Self-tapping screw	5~6 Kgf-cm	ϕ 5.0	JIS B1122 Type 2



PIN1	BROWN(OUT,3rd)	PIN9	TERMINAL(M-AS0G08-009)
PIN2	YELLOW(IN,3rd)	PIN10	TERMINAL(M-AS0G08-009)
PIN3	GREEN(OUT,PWM)	PIN11	TERMINAL(M-AS0G08-009)
PIN4	BLUE(IN,PWM)	PIN12	TERMINAL(M-AS0G08-009)
PIN5	GRAY(OUT,-)	PIN13	WHITE
PIN6	ORANGE(OUT,+)	PIN14	TERMINAL(M-AS0G08-009)
PIN7	RED(IN,+)	PIN15	TERMINAL(M-AS0G08-009)
PIN8	BLACK(IN,-)/PURPLE(PIN16)	PIN16	PURPLE/WHITE(PIN13)

4.1. Overview

The ASF7680BBX Fan Bottom Board provides 1 slave I2C channel for fan management and 2 Master I2C channels for temperature sensing. For the fan control, it can support two ways to control the fan modules, one way is the automatic sensing and adjusting, and the other way is manual controlling.

Table 20. Fan Board Top/Btm Overview

ASF7680BBX-0418-111ZZ	
PCB	4 Layers, TG-150 for Fan Top Board. 4 Layers, TG-150 for Fan Bottom Board.
Power Source	12V from PDU board.
Cooling	N/A
Dimension	422.69 mm (L: Depth) x 57.11 mm (W: Width) for Fan Board Btm. 150.0 mm (L: Depth) x 57.11 mm (W: Width) for Fan Board Top

4.2. Block Diagram

The ASF7680BBX Fan Board Bottom provides 1 slave I2C channel, which is connected to the Broadwell-DE module and 2 master I2C channels, which are connected to Main Board Top and Main Board Bottom. For the slave I2C channel, CPU can via this interface to get the status of the fan, and when the Fan CPLD is set to the manual mode, it can control the fan speed of the fan. For the master I2C channel, the Fan CPLD will automatically ready the temperature data of the thermal sensors on the Main Bottom Board and Main Top Board. When the temperature over the setting threshold, the Fan CPLD will speed up the fan speed to cool the system.

The Fan Top Board and Fan Bottom Board use 12VDC from the PDU Board which is delivered via

an internal power cable. The on-board DC/DC is used to generate 3.3V from 12VDC.

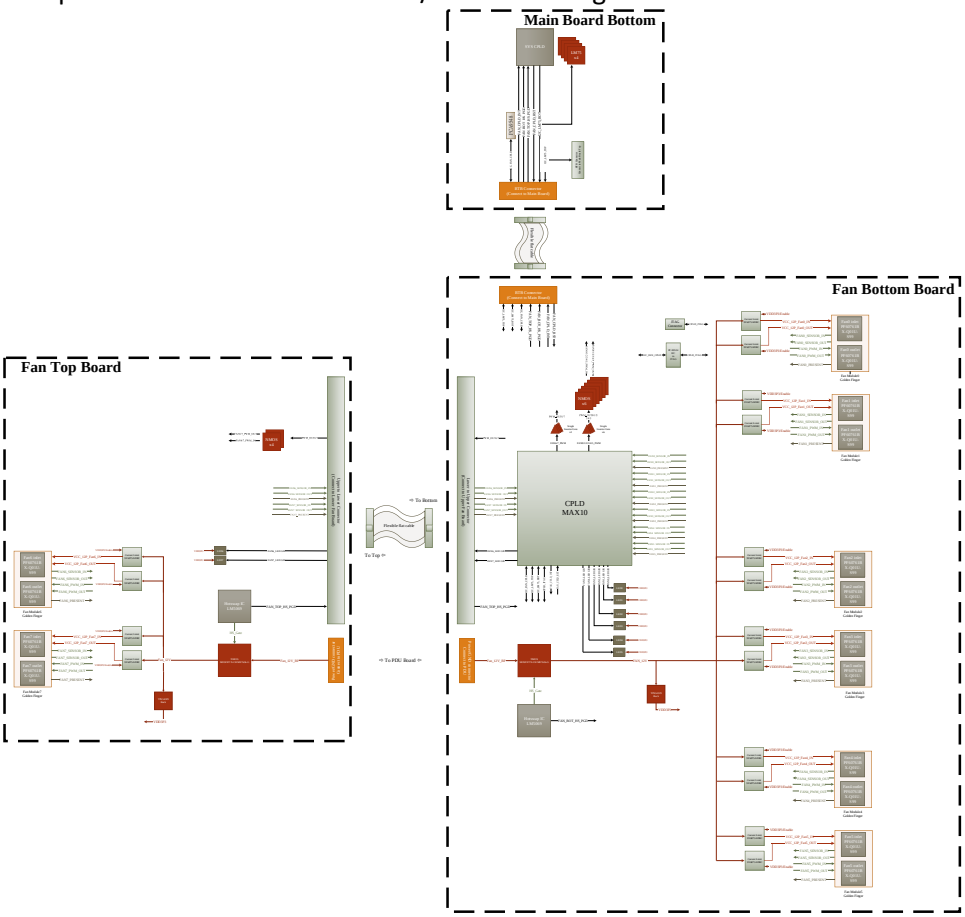


Figure 37. Block Diagram

4.2.1. Clock Tree

There is an Oscillator which provides 25MHz to the Fan CPLD.

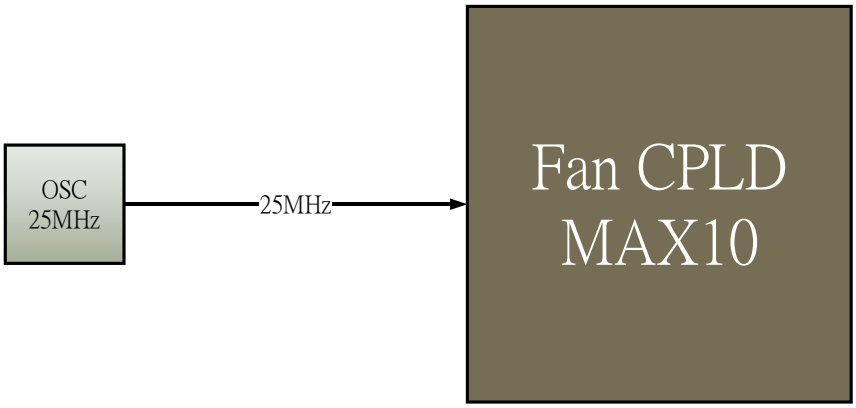


Figure 38. Fan Bottom Board clock Tree

4.2.2. Power Tree

The Fan Board Bottom/Top uses 12V to provide power for the fan modules, and it also converts

12V to 3.3V, which is the power source of the Fan CPLD and the others chips.

When the Fan Board Bottom/Top is powered up, its current will be monitored by the hot swap IC “LM5069”. If there is any over-current condition coming up, the LM5069 will turn off the MOS to prevent damage to the on-board chips.

The following is the power tree topology.

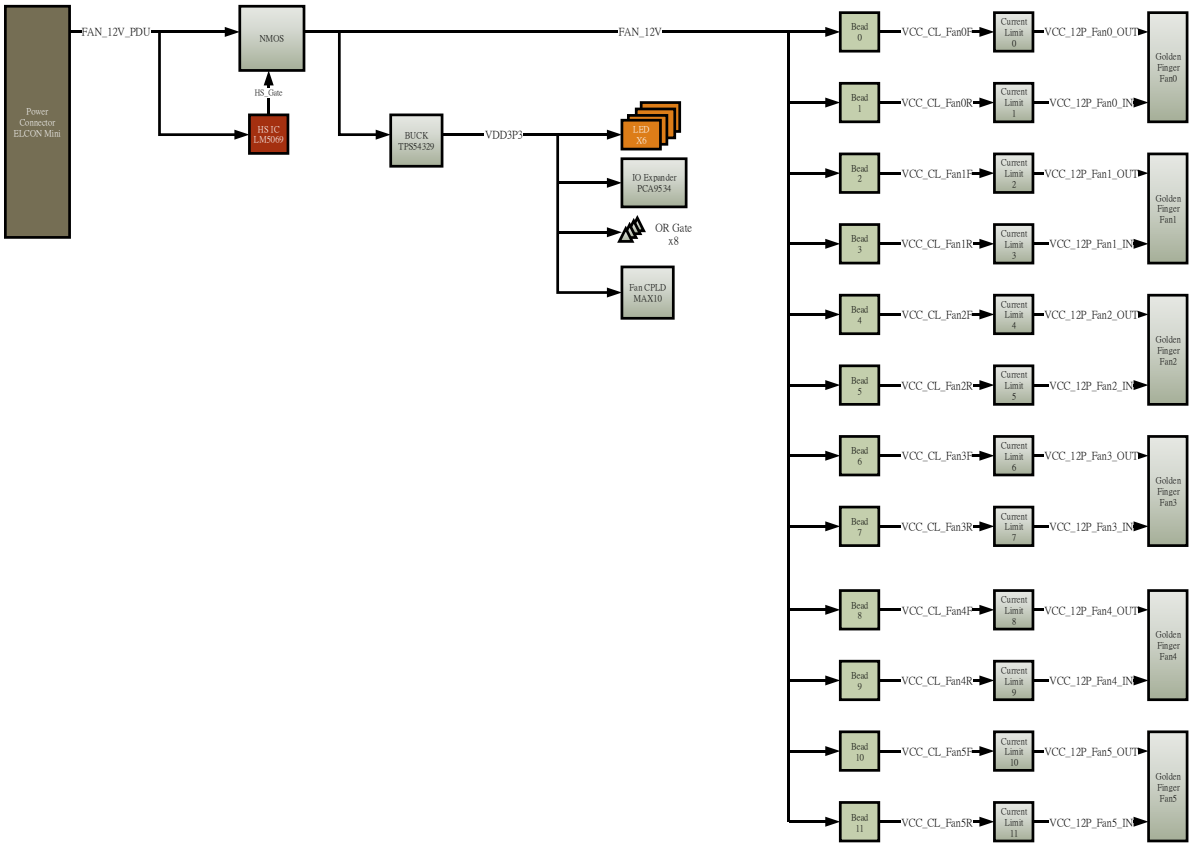


Figure 39. Fan Board Bottom Power Tree

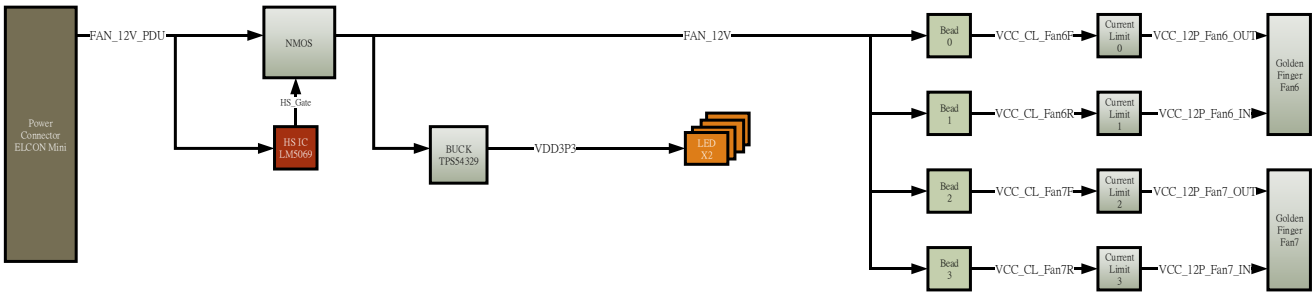


Figure 40. Fan Board Top Power Tree

4.2.3. Reset Tree

Resetting the Fan CPLD will follow as below.

1. Using the I2C to change bit 7 of the Reset Register (0x04) from high to low.
2. Using the system CPLD on the Main Board Bottom to reset the Fan CPLD.

The following is about the reset tree topology.

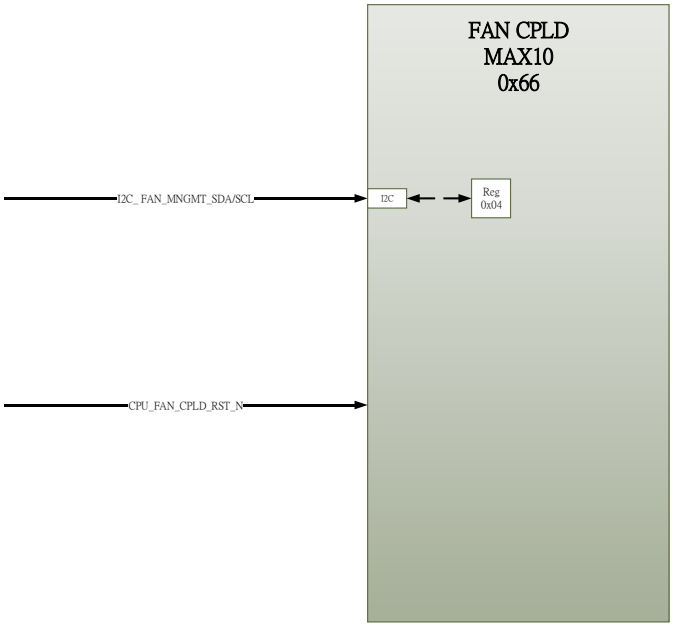


Figure 41. Reset Tree

4.2.4. Others

4.3. LED Indicator

The Fan Board Bottom/Top has 8 LEDs which indicates the present status of the fan modules. The 8 LEDs are next to the fan modules.

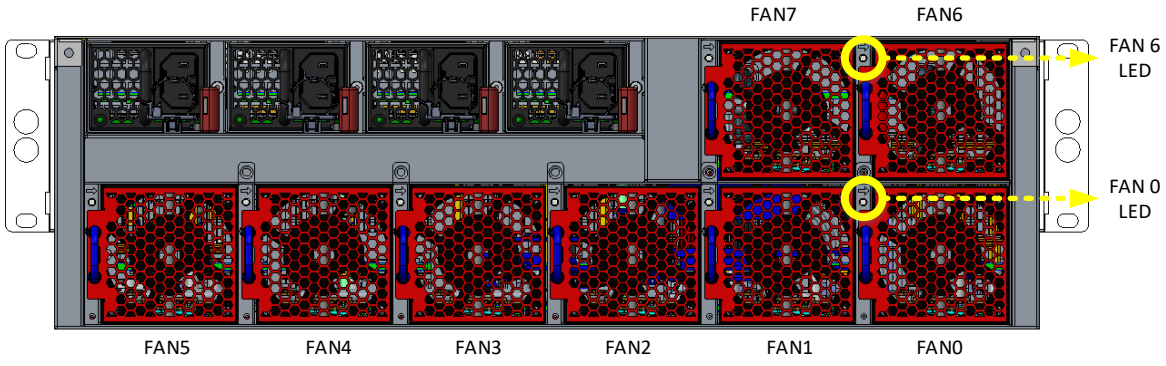


Figure 42. Rear panel of 3U Chassis

4.3.1. FAN BOARD BOTTOM/TOP LED

Table 21. Fan Board Bottom/Top LED Definition

OPERATING CONDITION	LED SIGNALING
Fan Module normal operation.	Solid Green
Fan Module did not present or fail	Solid Red

4.4. I2C ADDRESS TABLE

Table 22. I2C Address Table, Fan Board Bottom

Device	Address (HEX)
MAX10	0x66
PCA9534	0x27

4.5. Interrupt

When the Fan CPLD detects some errors during the system running, it will via the net "FAN_INT_L" to send the interrupt signal to the system CPLD of the Main Board Bottom, The interrupt connection are as below.

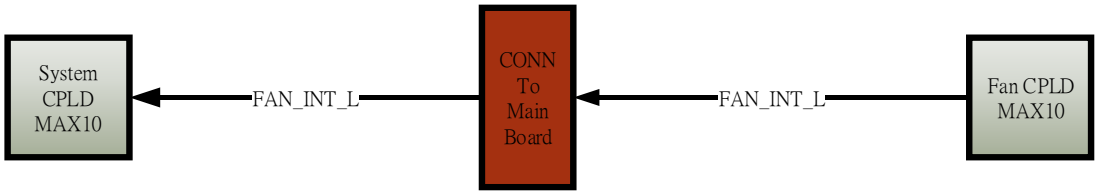


Figure 43. Interrupt Connection

4.6. JTAG

The Fan Board Bottom provides two ways of the JTAG download chain. One is using the test connector and GUI to do download, and the other one is using the PCA9534, which use the I2C interface to simulate the JTAG interface to program the Fan CPLD.

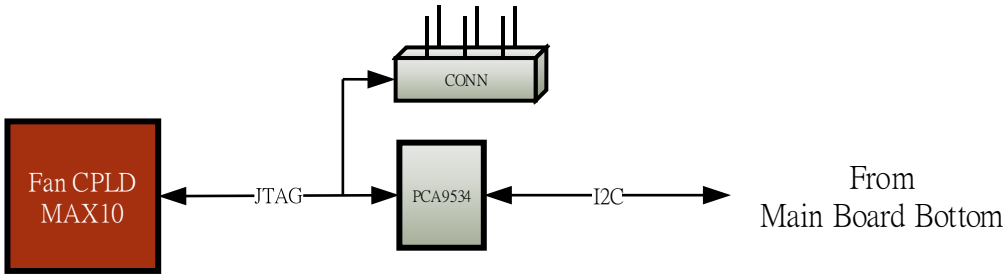


Figure 44. JTAG chain

4.7. Thermal system

4.7.1. Temperature sensor

There are nine temperature sensors on the Main Board Bottom, Main Board Top, and the CPU module. The Fan CPLD on the Fan Board Bottom can access the appropriate sensors, and got the temperature information via I2C interface. The sensors have the interrupt signal connection with the System CPLD for over-temp event application.

The temp sensor solutions are "LIN LM75BD 2.8-5.5V TEMP MINOTOR SO8 LT/LF NXP" and

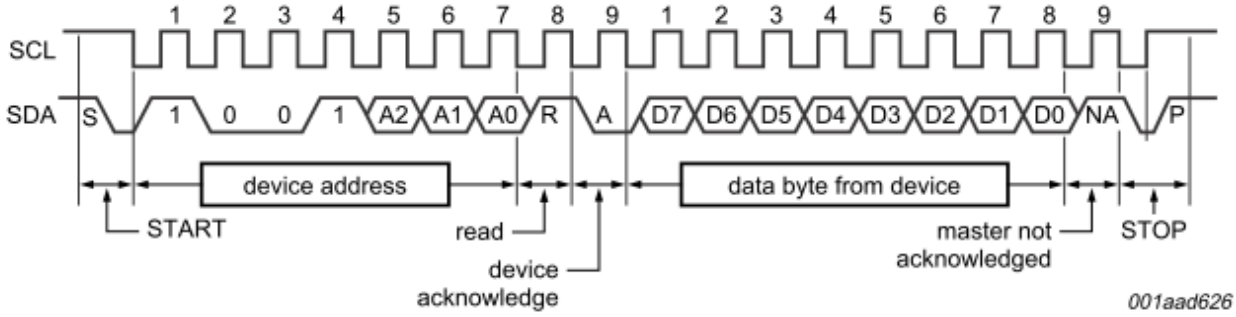
“TMP432ADGSR”.

The thermal alarm will be 70 degree at initial value and it is via thermal sensor’s interrupt to the CPU module. However, the temperature value that causes an interrupt will be optimized after thermal test result.

The Fan CPLD provides two I2C master interfaces and it connects to LM75s, TMP432, and the System CPLD of Main Board Bottom/Top and the CPU module. The Fan CPLD needs to get temperature information repetitive on every I2C master interface and put what it gets into the temperature registers. For the first I2C master channel, which connects to the Main Board Bottom, it connects four LM75s and one TMP432, and for the second I2C master channel, which connects to the Main Board Top, it connects three LM75s and one TMP432.

For the LM75, the I2C device addresses on the Main Board Bottom/Top are 0x4D, 0x4E, and 0x4F, and the I2C device address on the CPU module is 0x4B. For the TMP432, the I2C device address on the Main Board Bottom/Top is 0x4C.

To Read LM75, please follow the format showed as below.



To protect the system, system also need to alarm user if any thermal sensor over warning temp. The waring temp threshold showed as below

1. CPU module:

- LM75-4 (0x4B): > TBD

2. Main Board Bottom/Top:

- TMP432 (0x4C): > TBD,
- LM75-1 (0x4D): > TBD,
- LM75-2 (0x4E): > TBD,
- LM75-3 (0x4F): > TBD,

If the temp keeps go up after warning event, system shall turn off the system if any thermal sensor over damaged temp.

The damage temp threshold showed as below

1. CPU module:

- LM75-4 (0x4B): > TBD

2. Main Board Bottom/Top:

- TMP432 (0x4C): > TBD,
- LM75-1 (0x4D): > TBD,
- LM75-2 (0x4E): > TBD,
- LM75-3 (0x4F): > TBD,

4.8. CPLD

The Fan Board Bottom has one CPLD for LED decoding, reset control, power on control, and interrupt consolidation. Please check detail in Fan CPLD specification.

.

5. PDU Sub-system

The ASF7680BBX PDU board of the 3U chassis is the power source of the system, which connects four power supplies to provide the 12VDC for the whole system by using internal power cables. The status of the power supplies are monitored by the System CPLD on the Main Board Bottom. The CPU can use the I2C interface to control the power supplies by changing the bits of the registers.

Power Supply Modules

The AS7926-40/80X supports the power supply listed below:

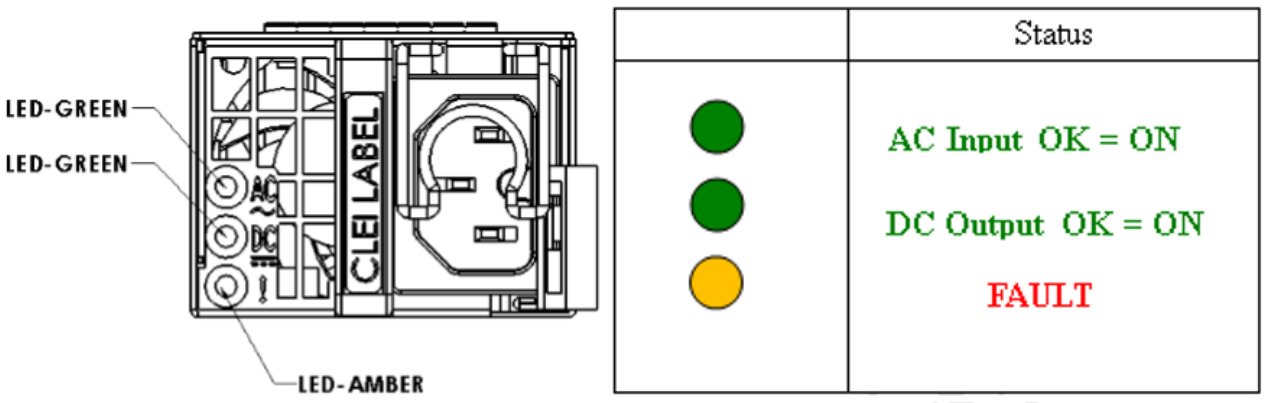
Vendor: MFG: Power-One. Agent: Belpower

Vendor P/N: PTT1600-12-054NAS445

Load range

Load Range				
Voltage	**Minimum Continuous**	**Maximum Continuous**	**OCP**	**Max. Power**
+5VSB	0A	3A	6A	1000W
+12V	1A	83.33A / 133.33A (L/H)	100A / 160A (L/H)	1600W

LEDs



5.1. PDU Board Block Diagram

The PDU Board connects four power supplies, which provides the 12VDC for the Main Board Bottom/Top and Fan Board Top/Bottom.

The system CPLD on the Main Board Bottom will record the status of these power supplies, and it can also turn on or turn off these power supplies by changing the bits of its own registers.

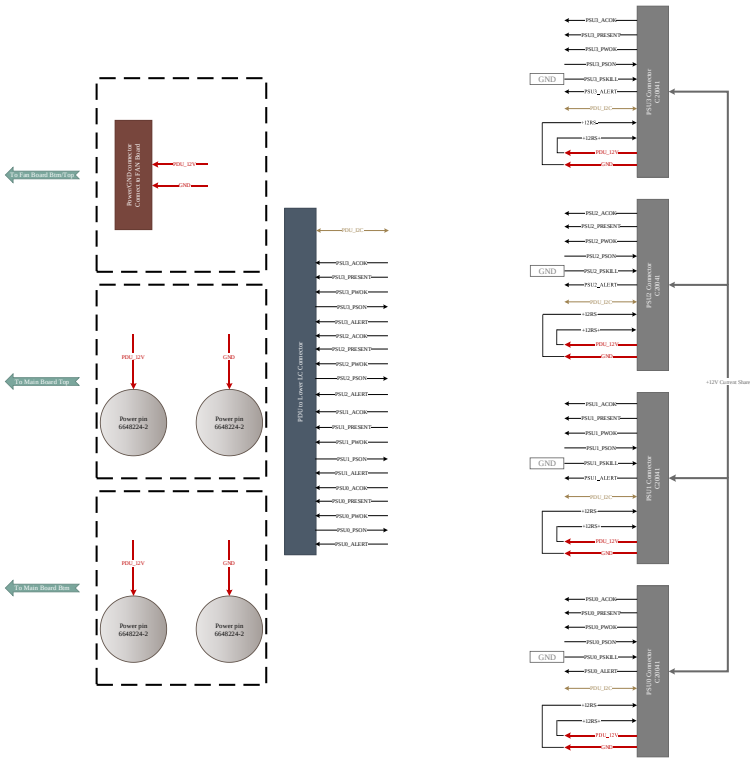


Figure 45. PDU Board Block Diagram

5.2. PDU Board LED Indicator

The power supply has a LED which indicates the status of the power supply.

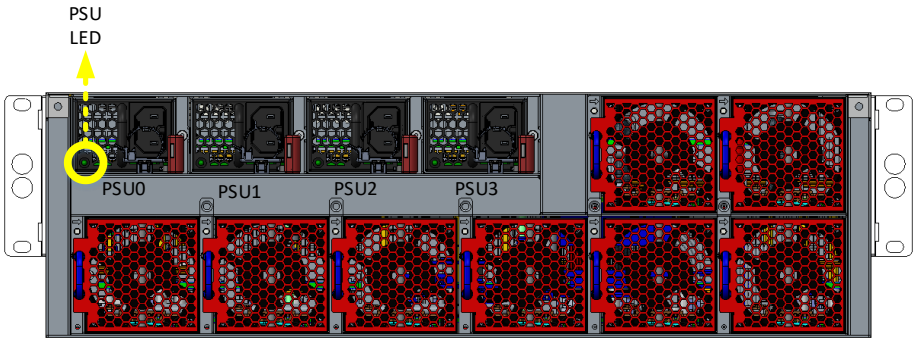


Figure 46. Rear panel of 3U Chassis

5.2.1. POWER SUPPLY LED

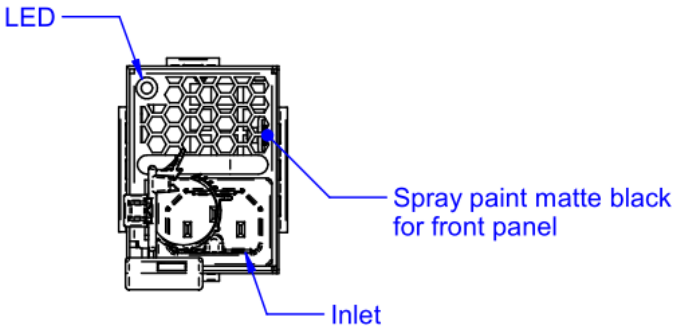


Figure 47. Front Panel of Power supply

Table 23. Power supply LED Definition

OPERATING CONDITION	LED SIGNALING
PSU LED (Green/Red)	
No AC power to all power supplies	OFF
No AC power to this PSU only, FAN Fault	Flashing RED (1 Sec On/ 1 Sec Off)
AC Present/ only standby output on	Flashing GREEN (0.5 Sec On/ 0.5 Sec Off)
Power supply DC output ON and OK	GREEN
Power supply failure	RED
Power supply warning	Flashing RED & GREEN (0.5 Sec Red/ 0.5 Sec Green)

5.3. PDU BOARD I2C ADDRESS TABLE

Table 24. I2C Address Table, PDU Board

Device	Address (HEX)
PSU0 Controller	0x5B
PSU0 EEPROM	0x53
PSU1 Controller	0x59
PSU1 EEPROM	0x51
PSU2 Controller	0x5A
PSU2 EEPROM	0x52
PSU3 Controller	0x58
PSU3 EEPROM	0x50

6. Mini-IO Sub-system

The ASF7680BBX Mini IO Board has 4 LEDs to indicate the status of the system, which is ""PWR LED", "SYS LED", "DIAG LED", and "FAN LED"."

The Mini IO board also has two connectors for external control, one is micro USB connector, and the other one is 1PPS connector.

The following is key feature of the Mini IO board:

- 1 Micro USB port.
- 1 1PPS port.

6.1. Mini IO Board Block Diagram

The Mini IO board has 4 LEDs to indicate the status of the system, which is "PWR LED", "SYS LED", "DIAG LED", and "FAN LED". For the PWR LED, it indicates the status of the power supplies. For the SYS LED, it indicates the location the 3U Chassis. For the DIAG LED, it shows the operating condition of the system, if there is any fail condition coming up, it will show the status of the system by using different color of the LED. For the FAN LED, it indicates the status of the fan modules.

The Mini IO board has two connectors, one is the USB connector, which is connecting the CPU, and the other one is the 1PPS connector, which provides the Sync-E function.

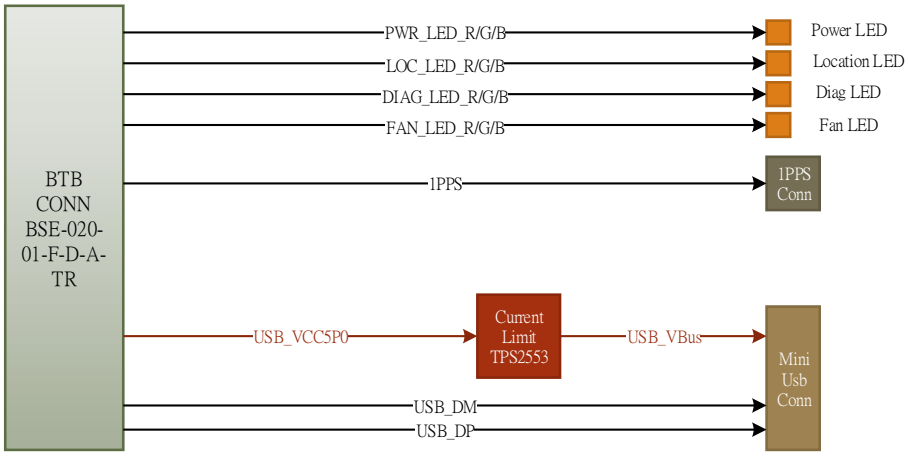


Figure 48. Mini Board Block Diagram

6.2. Mini IO Board LED Indicator

The Mini IO board has 4 LEDs which indicates the status of the system.

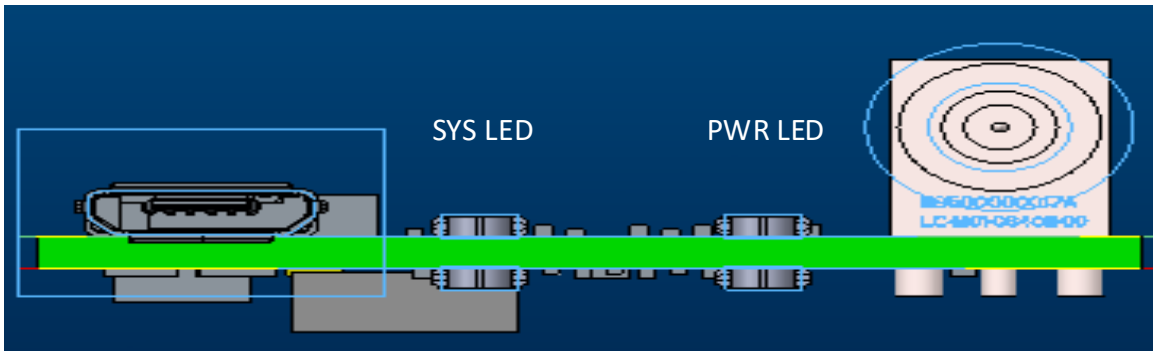


Figure 49. Front view of Mini IO board

7. Power Consumption

Table 25. Power Consumption Table

Power Consumption Estimation Table																												
Voltage(V) / Current(mA)		STB_VCC5P0	VCC5P0	VDD3P3	Vstby_3v3	VDD3P3_OCXO	HBM VPP	PLL	HVA 18	MIM & VDDIO		Blackhawk	HBM VDDC	HBM VDDO	HVA	ROV			DRAM PHY	AVS	VDDM	LVD	LVA	AVS	SerDes	(W)/device	Quantity	Total(W)
	12	5	5	3.3	3.3	3.3	2.5	1.8	1.8	1.8	1.8	1.2	1.2	1.2	1.2	0.87	1.0	0.9	0.88	0.85	0.85	0.8	0.8	0.8	0.8			
BCM88690				1000			1000	506				3744	12000	11000		355000			2000						55347	393.6912	2	787.3824
BCM16K									777.78						833.333					156470	8823.5	8363	11271			158.6067	2	317.2134
BCM81724										92														11100		9.0456	20	180.912
PEX8724											277							12222								11.4984	1	11.4984
CPLD SYS & FAN					500																					1.65	7	11.55
SYS LED				10																						0.033	8	0.264
100G Transceiver				1515																						4.9995	80	399.96
SFP+				455																						1.5015	2	3.003
LED				20																						0.066	330	21.78
UCD90320					54.9																					0.18117	1	0.18117
IDT 89H24NT24G2				5			205										5669									6.198	1	6.198
USB			500																							2.5	1	2.5
Fan	5000																									60	8	480
CPU Module	4000																									48	1	48
Sub Current(mA)	44000	0	500	130795	3554.9	0	2205	1012	1555.6	1840	277	7488	24000	22000	1666.67	710000	5669	12222	4000	312940	17647	16726	22542	222000	110694			2270.44237
Current+10%	48400	0	550	143875	3910.39	0	2425.5	1113.2				8236.8				781000	6235.9			344234	19412				121763			
PWM Spec																												
Efficiency=90%																												2522.71374

8. PCB
8.1. Dimension

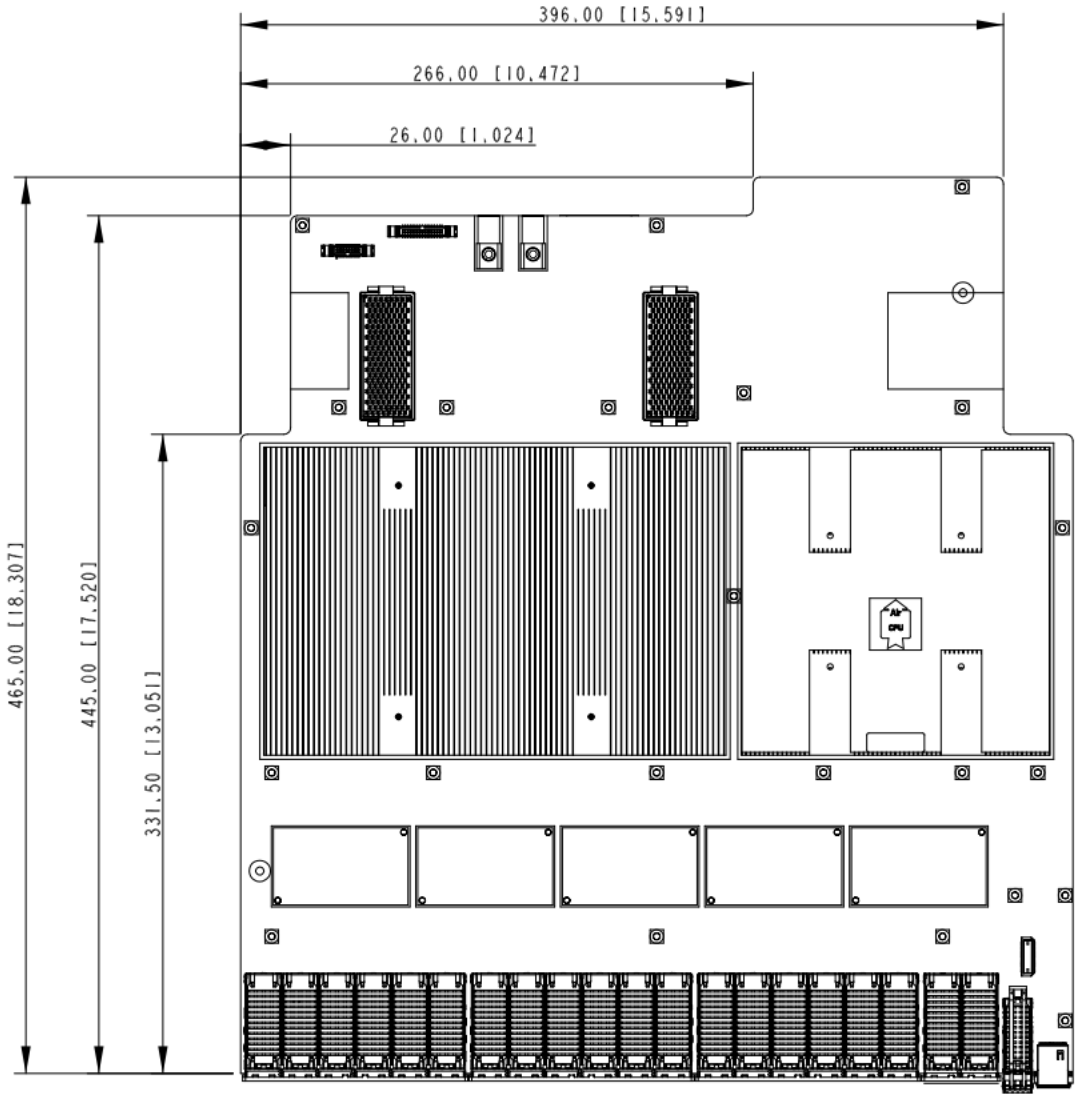


Figure 50. Bottom Main Board PCB Dimension

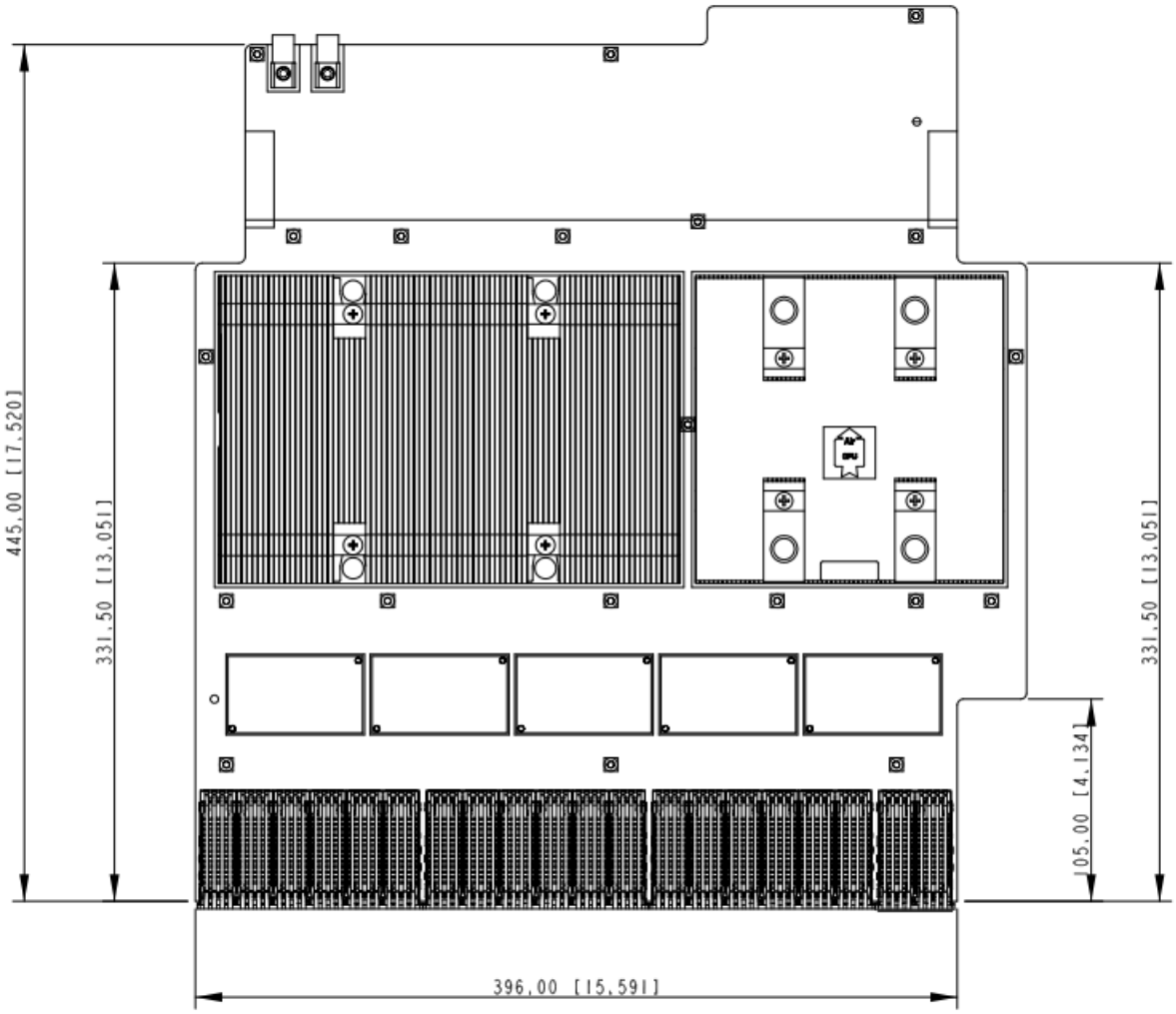


Figure 51. Top Main Board PCB Dimension

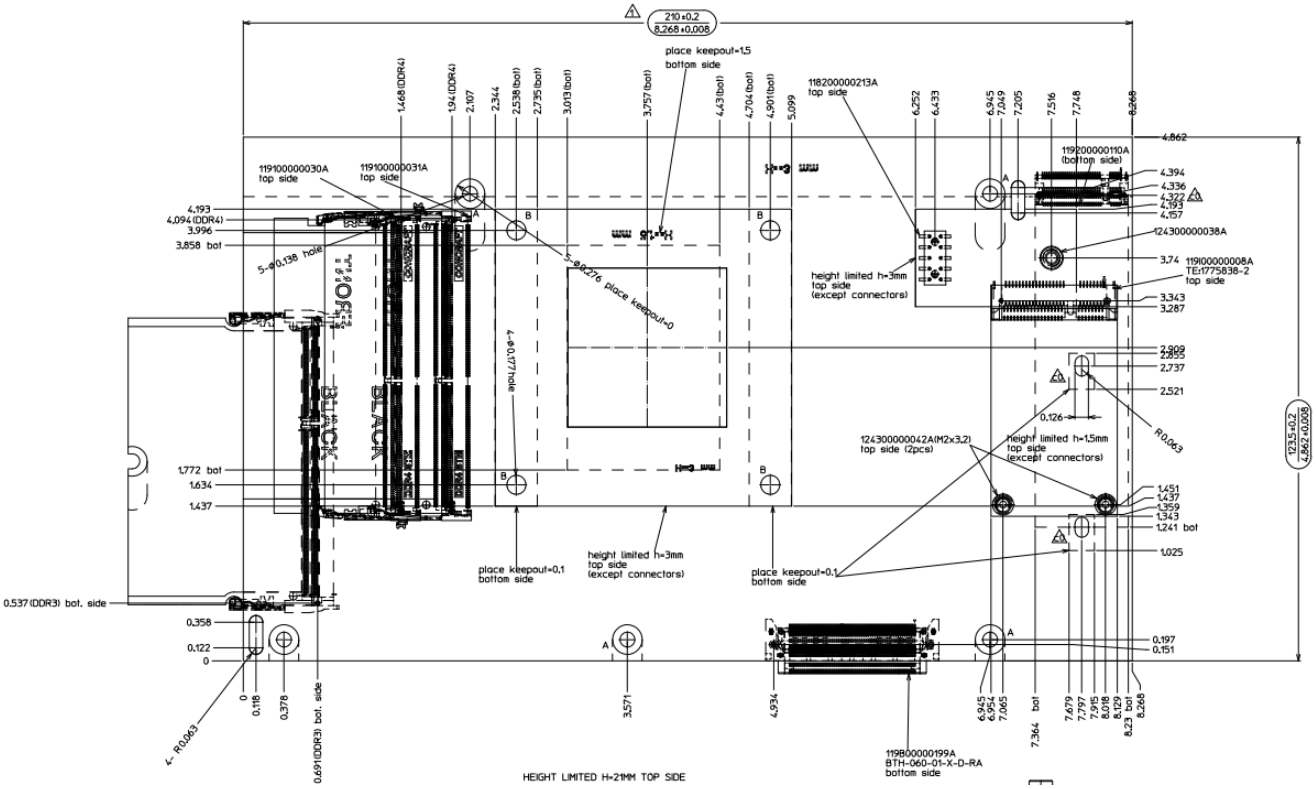


Figure 52. CPU module PCB Dimension

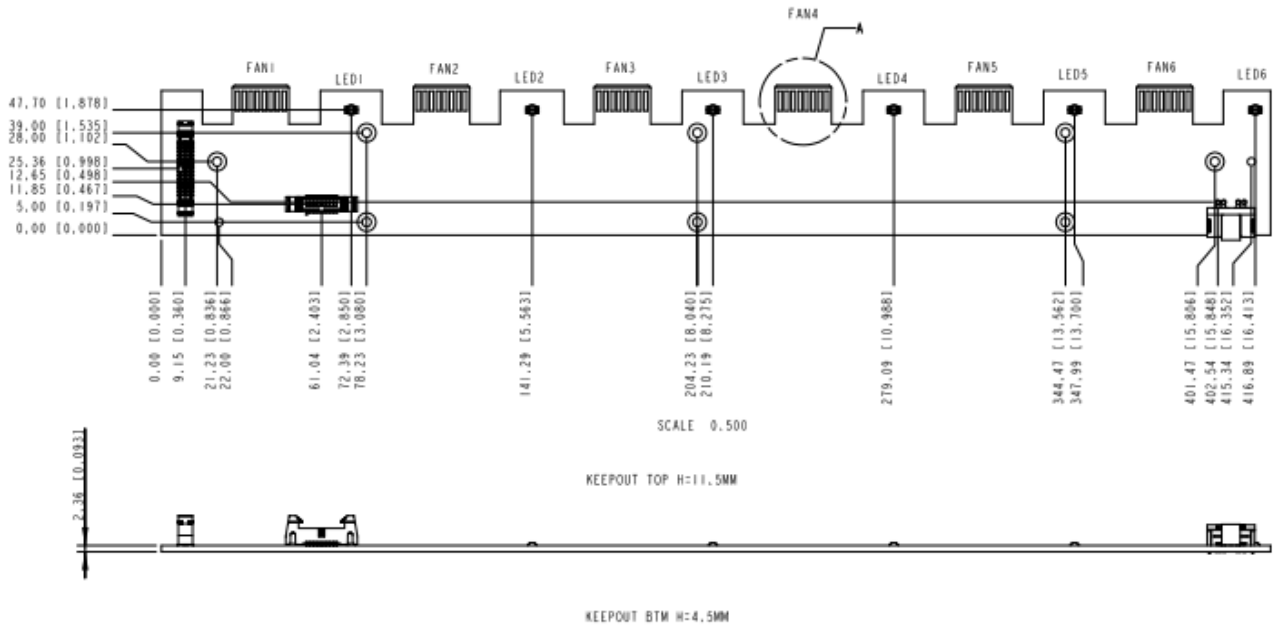


Figure 53. Fan Board Bottom PCB Dimension

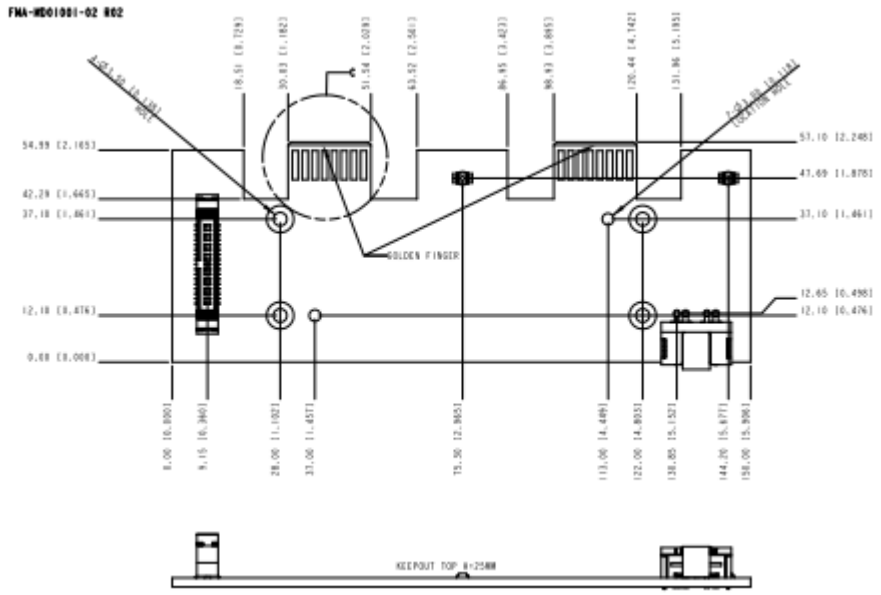


Figure 54. Fan Top Board PCB Dimension

The PDU Board PCB dimension is 60.0 x 393.0 mm.

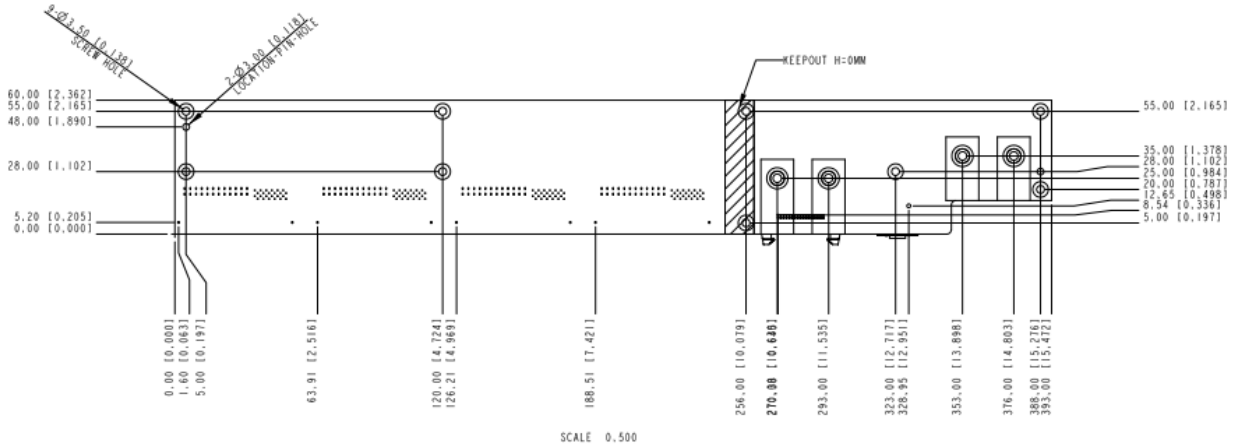


Figure 55. PDU Board PCB Dimension

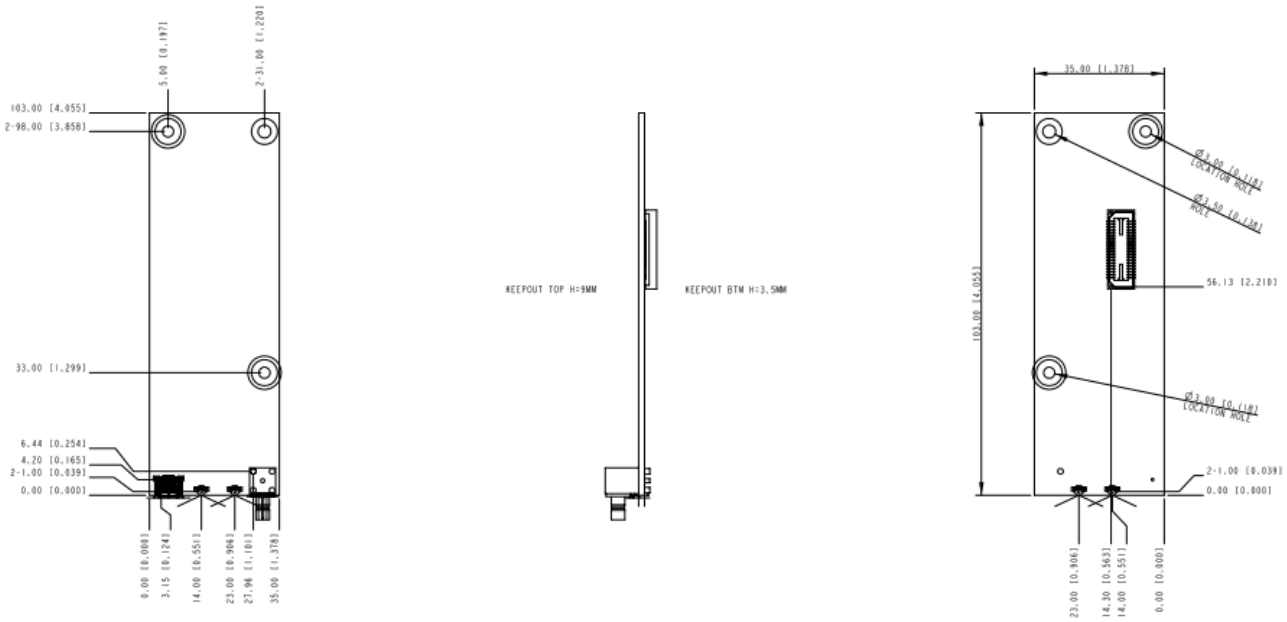


Figure 56. Mini IO Board PCB Dimension

8.2. Placement

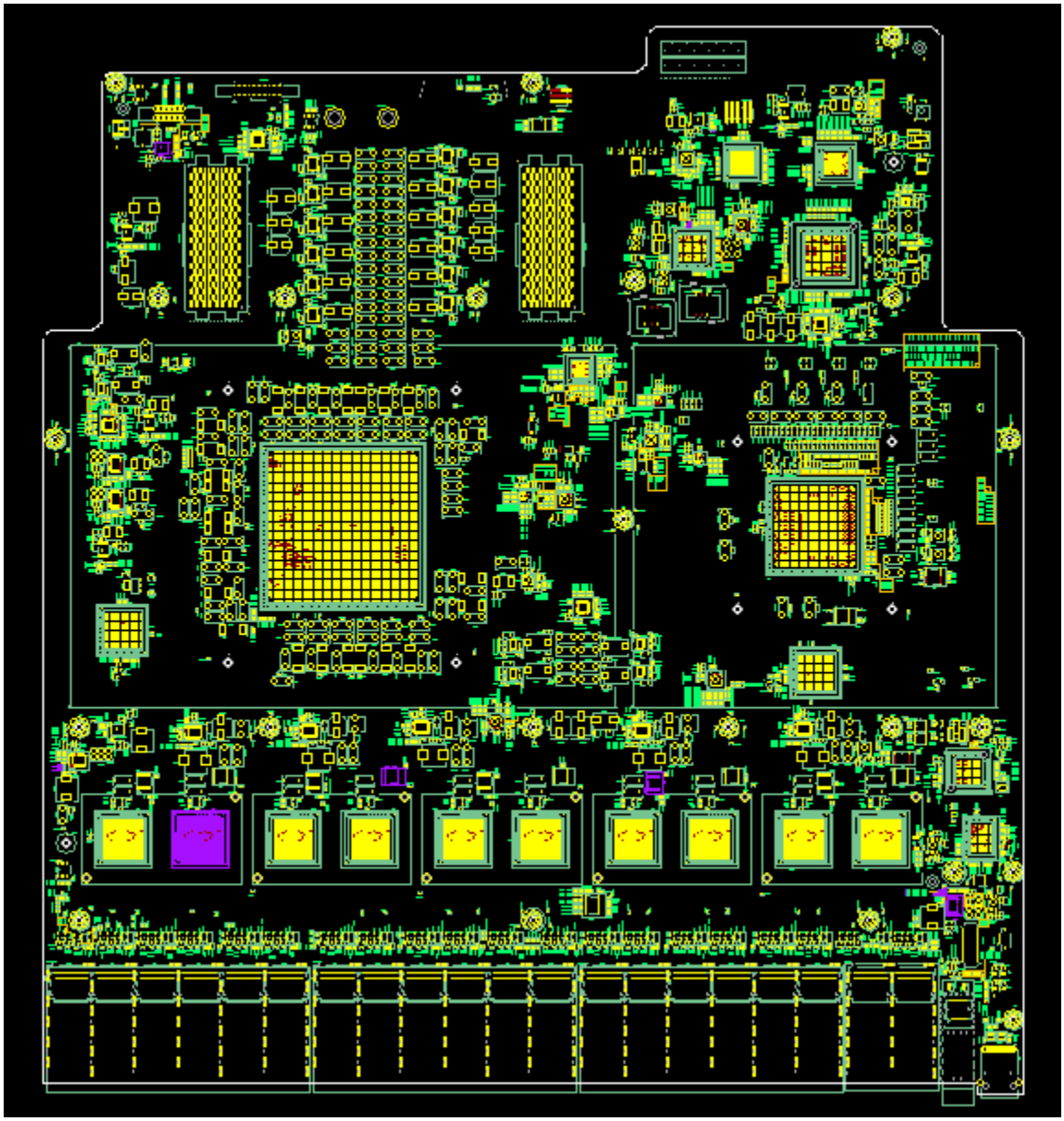


Figure 57. Bottom Main Board PCB Placement

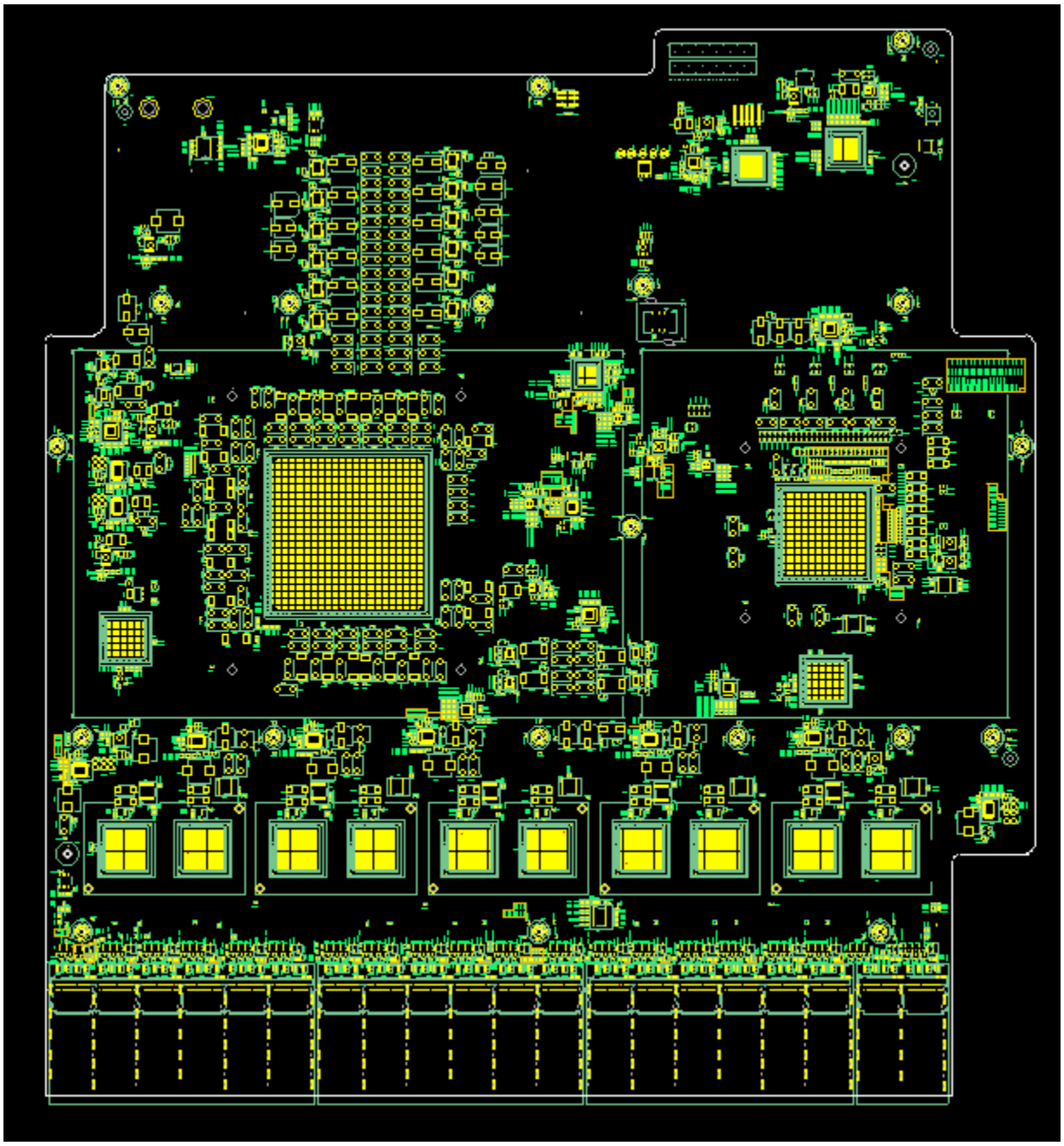


Figure 58. Top Main Board PCB Placement

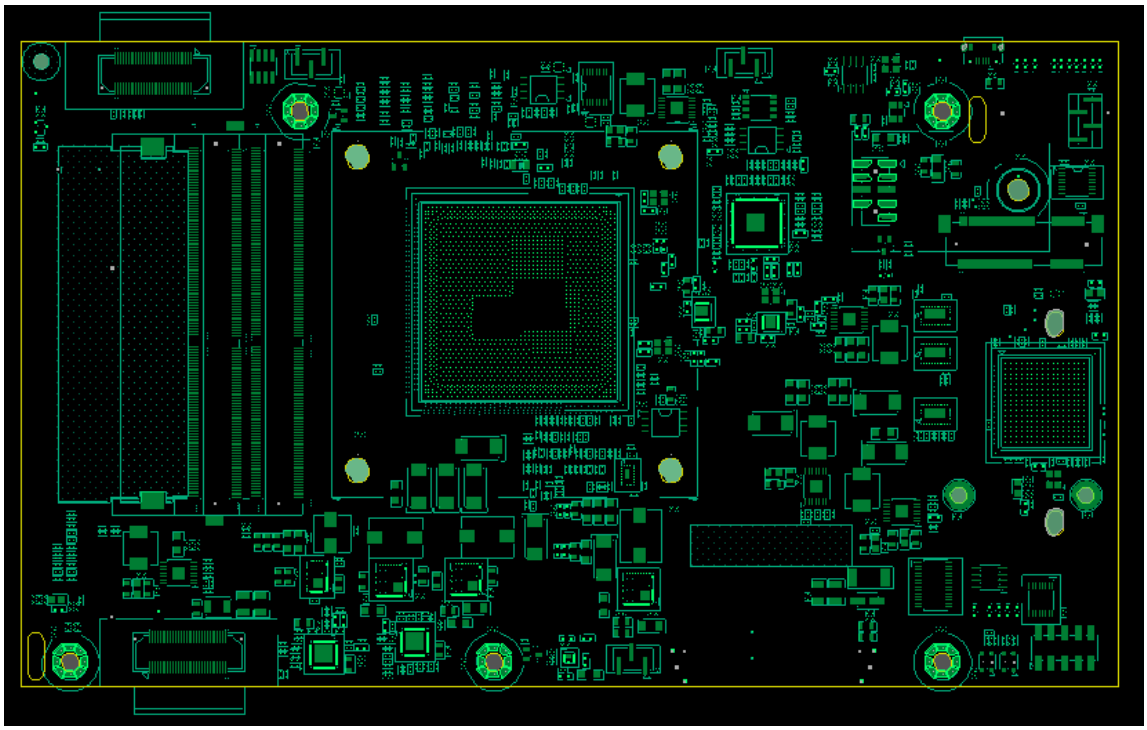


Figure 59. CPU module PCB Placement

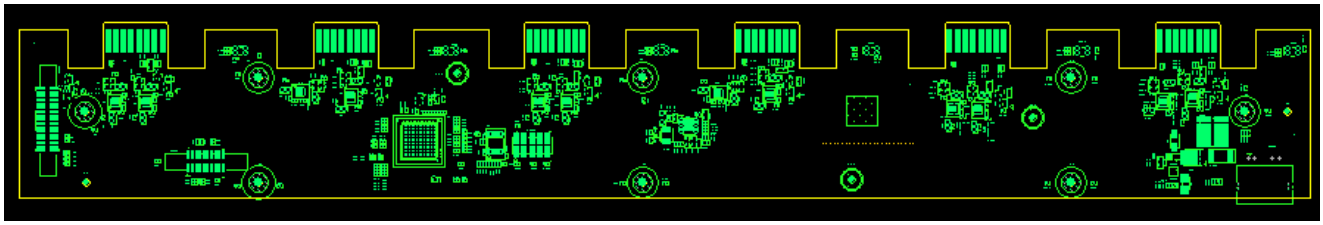


Figure 60. Fan Board Bottom - PCB Placement

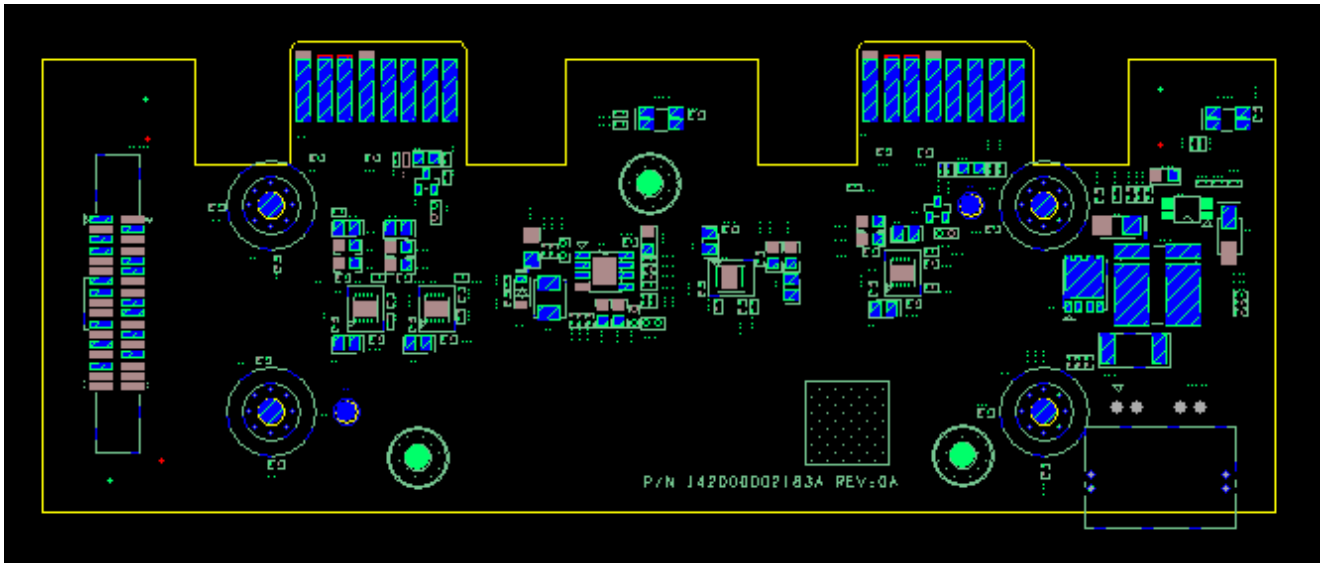


Figure 61. Fan Board Top - PCB Placement

9. Mechanical

Height: 131mm

Width: 440mm

Depth: 760mm

9.1. Dimension

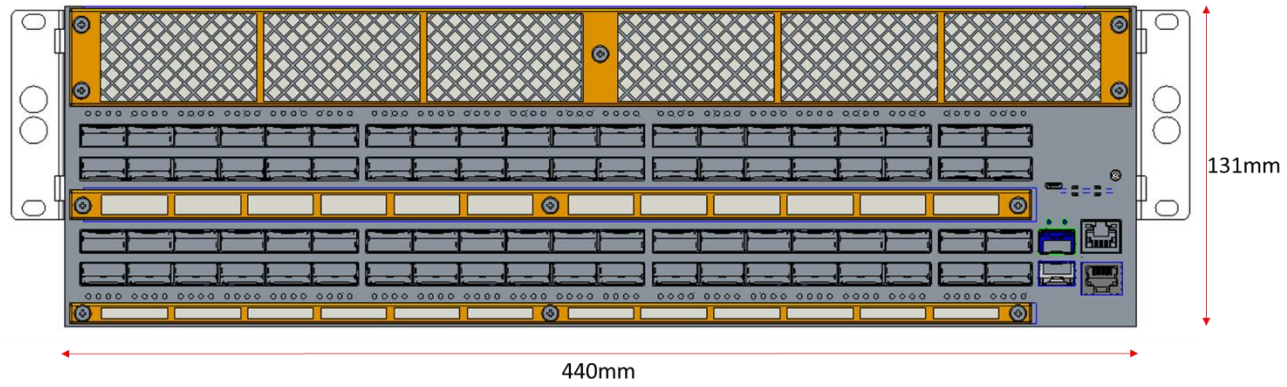


Figure 62. Mechanical Front view

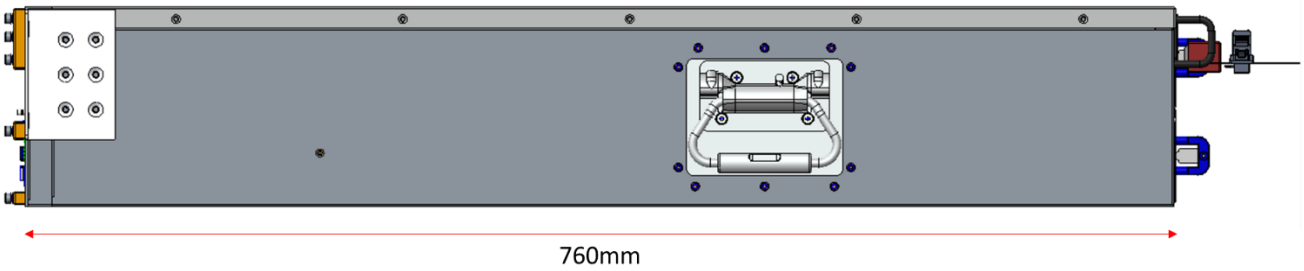


Figure 63. Mechanical Side view

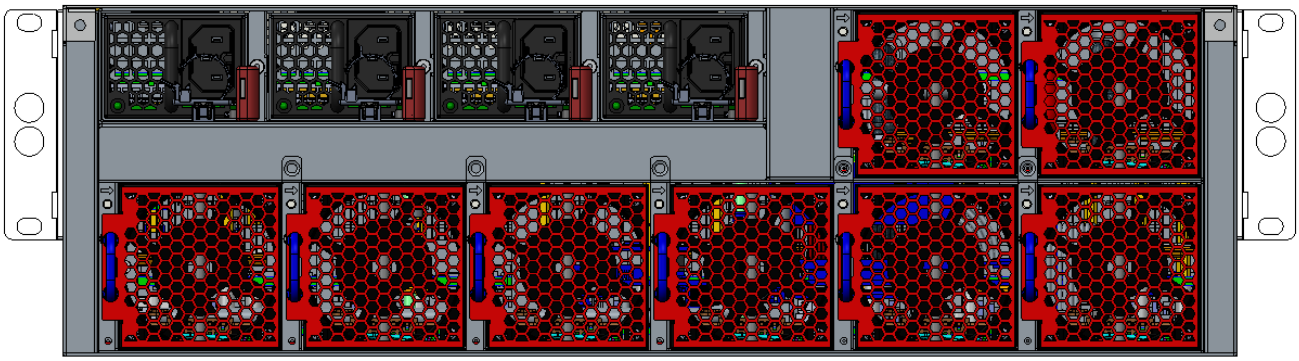


Figure 64. Mechanical Rear view

10 Standards and Specifications

Software Support

The AS7926-40/80X supports a base software package composed of the following components:

BIOS support

The AS7926-40/80X Supports AMI AptioV BIOS version A01 or greater with the x86 CPU module

ONIE

See https://github.com/opencomputeproject/onie/tree/master/machine/accton for the latest supported version

Open Network Linux

See http://opennetlinux.org/ for latest supported version

ROHS

Restriction of Hazardous Substances (6/6)

Compliance with Environmental procedure 020499-00 primarily focused on Restriction of Hazardous Substances (ROHS Directive 2002/95/EC) and Waste and Electrical and Electronic Equipment (WEEE

- Reference Documents
  1) ATT-TP-76200

Safety

- UL (CAN/CSA 22.2 No 60950-1 & UL60950-1)
- CB (IEC/EN60950-1)
- CCC (GB4943.1-2011)
- BSMI (CNS14336-1)

Electromagnetic Compatibility

- CE Mark
  - EN55032 Class A
  - EN55024 (Immunity) for Information Technology Equipment
  - EN 61000-3-3
  - EN 61000-3-2
- FCC Title 47, Part 15, Subpart B Class A
- VCCI Class A
- CNS 13438 (BSMI)
- CCC (GB9254-2008)

Environmental

- Low-Temperature Exposure and Thermal Shock (packaged) : NEBS GR63-CORE ISSUE 4 , Section 4.1.1.1
- High Relative Humidity Exposure (Packaged) : NEBS GR63-CORE ISSUE 4 , Section 4.1.1.2
- High-Temperature Exposure and Thermal Shock (Packaged) : NEBS GR63-CORE ISSUE 4 , Section 4.1.1.3
- Operating Temperature and Relative Humidity : NEBS GR63-CORE ISSUE 4 , Section 4.1.2
- Altitude : NEBS GR63-CORE ISSUE 4 , Section 4.1.3
- Handling Drop Tests -Packaged Equipment : NEBS GR63-CORE ISSUE 4 , Section 4.3.1.1
- Unpackaged Equipment -Drop Tests (All Equipment) : NEBS GR63-CORE ISSUE 4 , Section 4.3.2
- Earthquake (10U Rack) : NEBS GR63-CORE ISSUE 4 , Section 4.4.1 (Zone4)
- Office Vibration Test Procedure; 90 minutes/axis (Stand & 42U Rack) : NEBS GR63-CORE ISSUE 4 , section 4.4.4
- Transportation Vibration-Packaged Equipment : NEBS GR63-CORE ISSUE 4 , section 4.4.5
- Acoustic noise : NEBS GR63-CORE ISSUE 4 , section 4.6
- Bump : IEC60068-2-29- packaged
- Shock : ETSI EN 300 019-2-3 -Operational Tests, Class T3.2 op