

Edgecore AS7316-26X

Switch Specification

Revision 1.0



OPEN
Compute Project

Revision History

Revision	Date	Author	Description
1.0	9/13/2018	Jeff Catlin	Initial Draft

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	AS7316-26X
CPU sub-system	CPU: Intel Xeon D1519 1.5G DDR SDRAM: 8GB x 2 2133MHz with ECC (SO-DIMM) DDR4 SPI Flash (Boot): 16MB x 2 mSATA: 128GB MLC TPM: SLB 9665XT2.0 FW5.63 INFINEON
Management MAC	UART RS232 console port (RJ45), Out-band Management Ethernet port (RJ45) Broadcom BCM88470, 300Gbs full duplex switching
Ethernet Ports	16x 10G SFP + 8x 25G SFP28 + 2x 100G QSFP28
BMC	AST2400
CPLD	Altera 5M2210ZF324I5N (FBGA324) and 5M1270ZF256I5 (FBGA256)
FPGA	Altera 10M16DCU324I7G
PCB	20-Layers, TU-883+TU-862HF (Hybrid material) for Mainboard 12-Layers, TG 180 for CPU module 10-Layers, TG 150 for Connection Board 4-Layers, TG 150 for FAN Board 8- Layers, TU-662 、 EM-825 for BMC Board
Power Supply	400W PSU, airflow direction is front to back, DC to DC, AC to DC, 1+1 redundant load-sharing, hot-swappable. Notes: The airflow is front to back from chassis system view.
Cooling	5 fan-tray modules with 5 pcs of 40mm x40mm x 28mm 12V fans, hot-swappable
Dimension	L(Depth):299.8±0.5mm (11.8031±0.0196inch) W(Width):438.4±0.5mm (17.259808 ± 0.0196 inch) H(Height):43.25±0.5 mm (1.7027±0.0196inch)

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Scope

This document outlines the technical specifications for the Edgework AS7316-26X Open Switch Platform submitted to the Open Compute Foundation.

Overview

This document describes the technical specifications of the AS7316-26X Cell Site Gateway Router designed by Edgework Networks Corporation. The AS7316-26X is a cost optimized design focused on the aggregation of 10G/25G cellular equipment and providing 100G backhaul connections. The AS7316-26X supports a broad set of IEEE 1588 /SyncE features geared towards 4G and 5G timing needs.

The AS7316-26X supports sixteen SFP+ ports, eight SFP28 ports, and two QSFP28 ports for network connectivity.

The AS7316-26X is a PHY-Less design with the network interface connections directly attaching to the Serdes interfaces of the Broadcom 88470 switching silicon providing the lowest cost, latency, and power. The AS7316-26X supports traditional features found in switches such as:

- Redundant field replaceable power supply and fan units
- Support for “Front to Back” air flow direction
- Supports a modular CPU card that allows flexibility in the CPU and/or memory configurations that can be offered.
- Support for AC or DC power supply units

Physical Overview

Front View

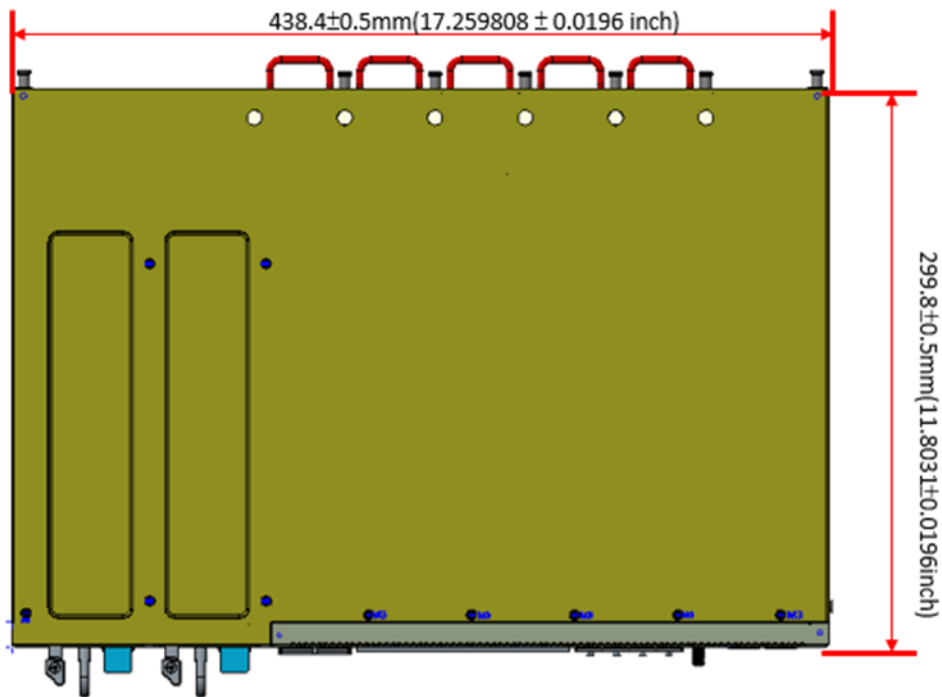


Rear View



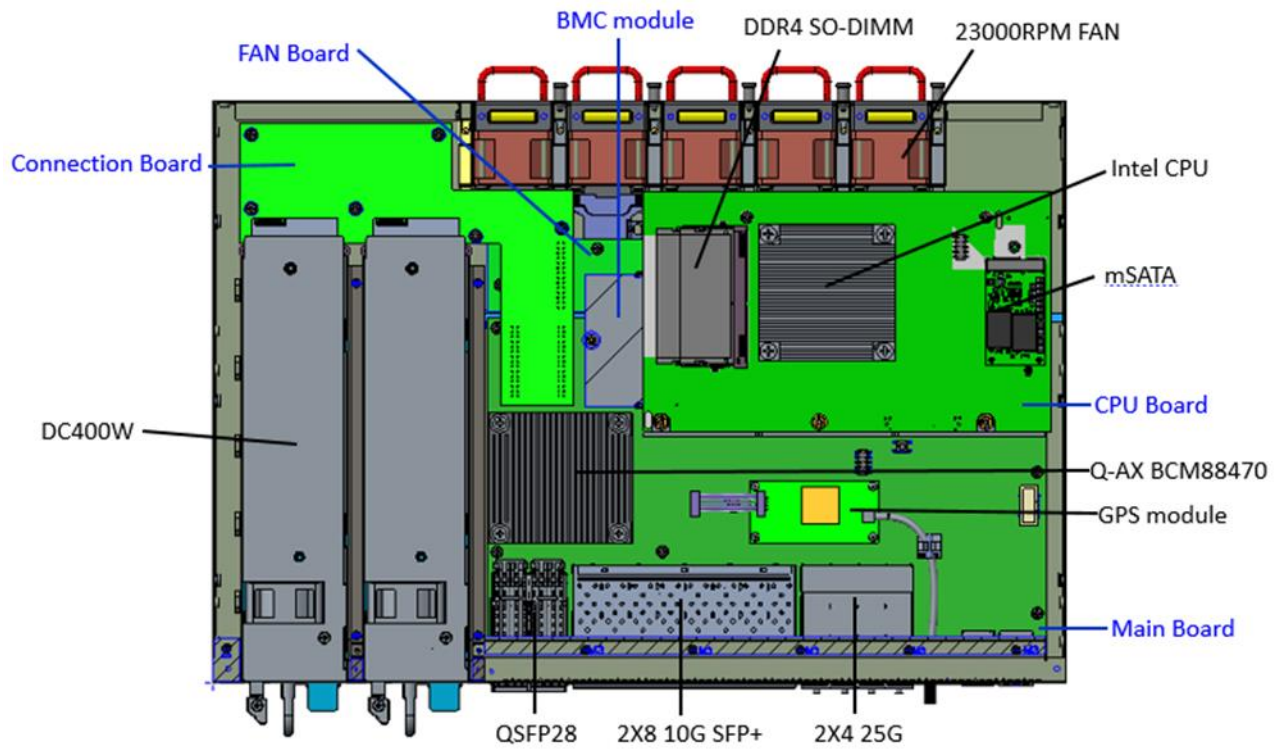
Dimensions

	Inches	Millimeters
Length	11.80	299.8
Width	17.26	438.4
Height	1.70	43.25

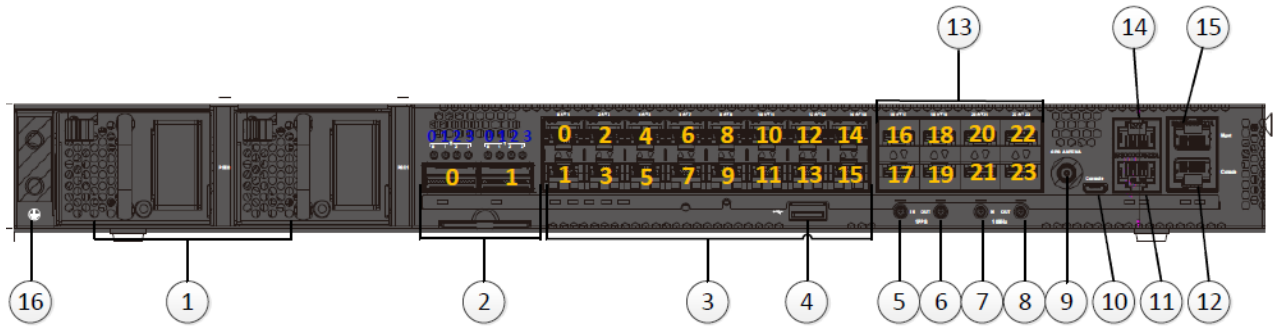


Top View

The top view of the AS7316-26X shows the PCBs and associated components in the AS7316-26X system



Front View Detail



The front panel view of the AS7316-26X includes the following key components:

<u>Description</u>	
<u>1- Power Supplies</u>	<u>9- GPS antenna port</u>
<u>2-100 Gigabit Ethernet QSFP28 ports</u>	<u>10-Micro USB console port</u>
<u>3-10 Gigabit Ethernet SFP+ ports</u>	<u>11-Time of day (ToD) RJ45 port</u>
<u>4-USB storage port</u>	<u>12-RJ45 console port</u>
<u>5-1PPS input port</u>	<u>13-25 Gigabit Ethernet SFP28 ports</u>
<u>6-1PPS output port</u>	<u>14- Building-Integrated Timing System port (BITS)</u>
<u>7-10MHz input port</u>	<u>15-Management Ethernet port (MGMT)</u>
<u>8-10MHz output port</u>	<u>16-Grounding mark</u>

Front Panel LEDs

Network / Timing LEDs

Each port has its dedicated LED with QSFP28 and SFP+ connectors. The management port has dedicated LED to indicate Link and Activity. The ToD and BITS ports have dedicated LED to indicate Link status.

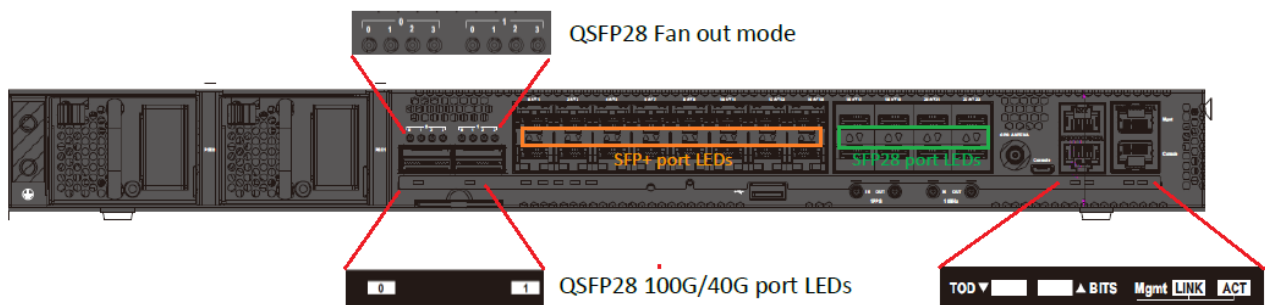


Figure 1 Network and Timing Port LEDs

Port LED Definition		
LED	CONDITION	STATUS
SFP+ Port LED (Port00 to Port15)	On/Flashing Green	SFP+ port has a valid activity at 10G mode and the flashing to indicate activity.
	On/Flashing Amber	SFP+ port has a valid activity at 1G mode and the flashing to indicate activity.
	Off	There is no link on the port.
SFP28 Port LED (Port16 to Port23)	On/Flashing Blue	SFP28 port has a valid activity at 25G mode and the flashing to indicate activity.
	On/Flashing Green	SFP28 port has a valid activity at 10G mode and the flashing to indicate activity.
	Off	There is no link on the port.
QSFP28 Port LED in 40G/100G Mode. (The LEDs are under the port24&port25 of QSFP28 cage)	On/Flashing Green	QSFP28 port has a valid activity at 100G mode and the flashing to indicate activity.
	On/Flashing Blue	QSFP28 port has a valid activity at 40 G mode and the flashing to indicate activity.
	Off	There is no link on the port.
QSFP28 Port LED in 25G Fan Out Mode. (With Breakout cable)	On/Flashing Amber	QSFP28 port has a valid link at 25G via break out cable. The LED on 100G QSFP28 end is also present OFF. Flashing indicates activity.
	Off	There is no link on the port.
QSFP28 Port LED in 10G Fan Out Mode. (With Breakout cable)	On/Flashing Purple	QSFP28 port has a valid link at 10G via break out cable. The LED on 40G QSFP28 end is also present OFF. Flashing indicates activity.
	Off	There is no link on the port.
OOB Port LED (Link)	On / Green	Port has a valid link
	Off	There is no link on the port
OOB Port LED (Activity)	Flashing / Green	Flashing indicates activity
	Off	There is no link on the port
ToD Status LED	On/Flashing Green	ToD port has an activity and the flashing to indicate activity.
	Off	There is no link on the port
BITS Status LED	On/Flashing Green	Bits port has activity and the flashing to indicate activity.

	Off	There is no link on the port
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System LEDs

The system LEDs are used to indicate the status of power and system.

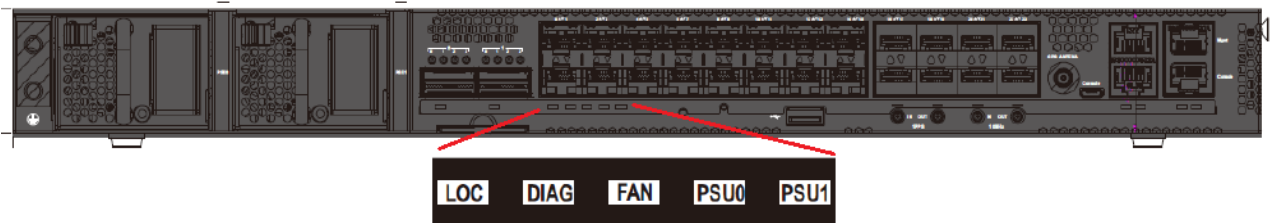


Figure 2 System LEDs

System LED Definition		
LED	CONDITION	STATUS
PSU0 (Power Supply Status)	Green	This power is operating normally.
	Amber	PWR present but not power on or this power is fault.
	Off	Power supply not present.
PSU1 (Power Supply Status)	Green	This power is operating normally.
	Amber	PWR present but not power on or this power is fault.
	Off	Power supply not present.
DIAG (Diagnostic)	Green	System self-diagnostic test successfully completed.
	Green Blink	System self-diagnostic test is in progress.
	Amber	System self-diagnostic test has detected a fault.
FAN	Green	System FAN operating normally.
	Green Blink	System FAN tray is power off when ambient temperature is less than 10 degree C.
	Amber	System FAN tray present but is fault.
LOC	Amber Flashing	Flashing by remote management command. Assists the technician in finding the right device for service in the rack.
	Off	Not a particular switch that technician need to find.

Front panel ports

- Micro USB port console port
 - Used for RS232 type management
- RJ45 Console Port
 - Used for RS232 type management
- RJ45 10/100/1000 Ethernet management port
 - Connected directly to the system CPU
- RJ45 ToD Port

- RJ45 BITs Port

Console Port

The console port interface conforms to the RJ45 electrical specification.

The interface supports asynchronous mode with default eight data bits, one stop bit, and no parity.

The unit will operate at any one of the following baud rates:

- 9600, 19200, 38400, 57600, **115200 (Default)**

Pin number	Pin name	Pin number	Pin name
1	RTS	2	UART_TXD
3		4	
5	GND	6	UART_RxD
7		8	CTS

Network ports

SFP+ Ports (sixteen in total)	Standard SFP / SFP+ MSA compliant modules supporting 1G and 10G options for copper and fiber
SFP28 Ports (eight in total)	Standard SFP / SFP+ MSA compliant modules supporting 1G and 10G options for copper and fiber Support for 25G Copper and fiber SFP28 modules
QSFP28 Ports (two in total)	Standard 40Gb QSFP+ modules including but not limited to: 40GBASE-SR4, 40GBASE-LR4, 40GBASE-ER, AOC Cables
QSFP28 Ports	Standard DAC cables including but not limited to: Passive cables up to 7m, QSFP<> QSFP DAC, QSFP<>SFP+ DAC Breakout

QSFP28 Ports	Support for all standards compliant QSFP28 XCVRS including but not limited to 100GBASE-SR4, 100GBASE-LR4
QSFP28 Ports	Standard DAC cables including but not limited to: Passive cables up to 3m, QSFP28<-> QSFP28 DAC, QSFP28<->SFP28 DAC Breakout

Rear View



The rear view of the AS7316-26X includes the following key components:

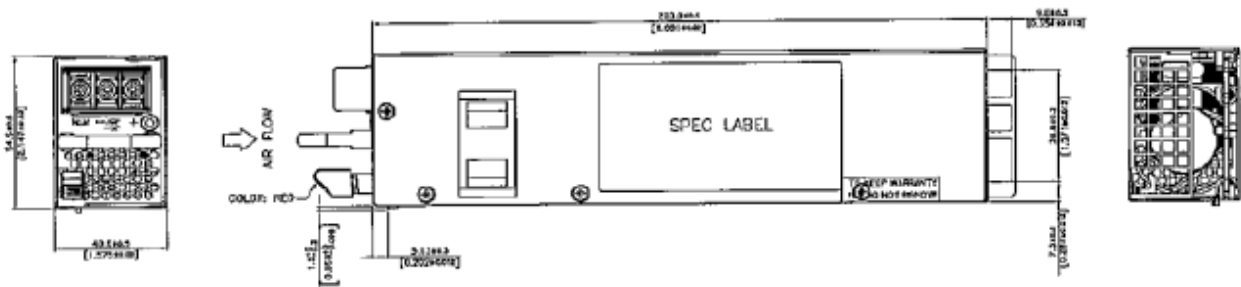
- Five(4+1) redundant hot swappable fan modules
 - LED per fan module to indicate status
 - Color coding to indicate airflow direction
- Chassis Grounding Lug

Field Replaceable Units

Power Supply Modules

The AS7316-26X supports two redundant power supply modules as listed below

400 Watt PSU: DC Input Range 36-72VDC Front to back airflow		
<ul style="list-style-type: none"> Vendor 3Y Vendor part number YM-2401UB01R 		
400 Watt PSU: AC input Range 90-264VAC / 47-63Hz Front to back airflow		
<ul style="list-style-type: none"> Vendor 3Y Vendor part number YNEA0400AM-1R01P10 		
	<u>Inches</u>	<u>Millimeters</u>
Length	8.66	220
Width	2.15	54.5
Height	1.57	40



Power Supply LEDs

Each power supply has a single LED to indicate status of the power supply unit.

Power supply status	Power supply LED color
No AC power to all PSU	OFF
Only +5V standby output on (AC OK)	0.5Hz Blinking Green*
Power supply DC output ON and OK	Green
Power supply fail	Red
FAN fail	1 Hz Blinking Red
Power supply warning	0.5Hz Blinking Red/Green*

Power supply Pin-Out

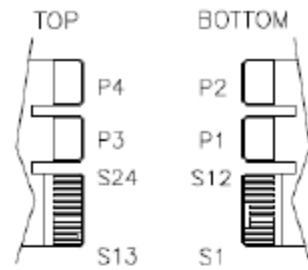


Figure 2 – Card Edge Pin Out Location

Pin Assignment:

- P1~4 : Power Circuits
- S1 ~ S24 : Signal Circuits

Table 1 – Card Edge Pin Out Definition

PIN NO.	CONDITION	PIN NO.	CONDITION
P4	GND	P2	+12V
P3	GND	P1	+12V
S24	+5VSB	S12	+5VSB
S23	+5VSB	S11	+5VSB
S22	NC	S10	A1
S21	NC	S9	PW OK
S20	NC	S8	PS ON
S19	NC	S7	PS-KILL
S18	NC	S6	SCL
S17	NC	S5	SDA
S16	NC	S4	PS-ALERT
S15	A0	S3	+12VBUS
S14	PRESENT	S2	NC
S13	PDB-FAIL	S1	NC

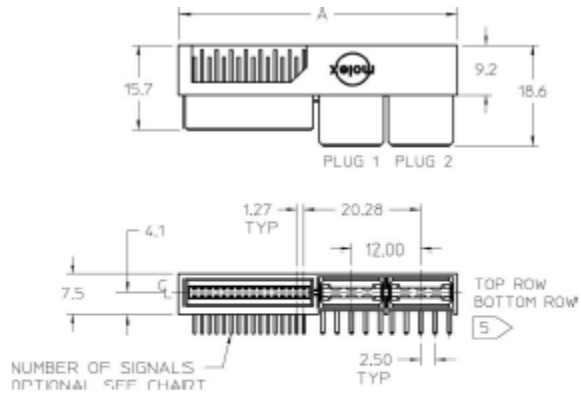


Figure 3 – PDB Mating Connector

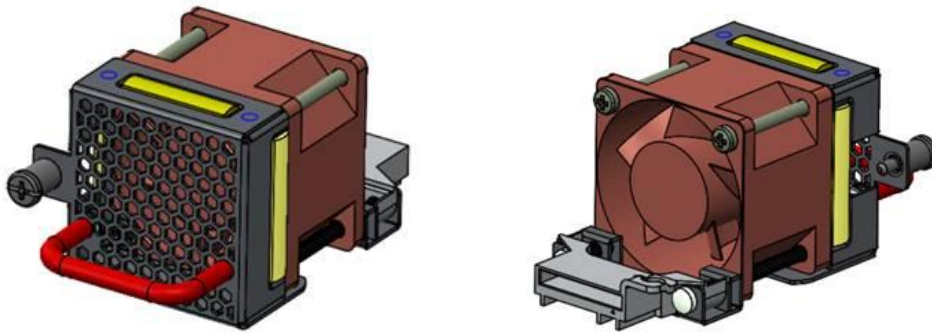
Pin Assignment:

- P1~4 : Power Circuits
- S1 ~ S24 : Signal Circuits

Fan Modules

The AS7316-26X supports five individual fan modules. Each fan module supports two 40mmx40mmx28mm fans shown below.

Description	Manufacturer	Part Number
Fan – Front to back airflow	INVNI	PF40561BX-Q020-S99



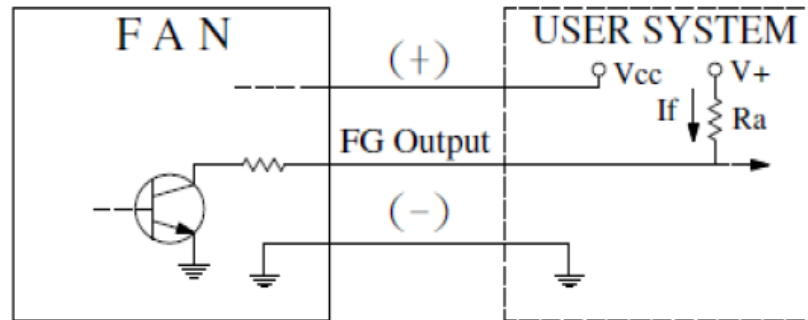
Front to Back fan module

- FAN characters::
- Operating temperature: -10C to +85C

ITEM	DESCRIPTION
RATED VOLTAGE	12 VDC
OPERATING VOLTAGE	10.2 ~ 13.2 VDC
STARTING VOLTAGE	10.2 VDC (25 deg. C POWER ON/OFF at PWM Duty 100%)
RATED CURRENT (AVG.)	1150mA
RATED POWER (AVG.)	13.8W
RATED SPEED	23000 RPM \pm 8% IN FREE AIR AT RATED VOLTAGE
MAX AIRFLOW AT ZERO STATIC PRESSURE	31.6 CFM
MAX STATIC PRESSURE AT ZERO AIRFLOW	3.25 inch-H ₂ O
ACOUSTICAL NOISE (AVG.)	62 dB(A)
INSULATION TYPE	UL CLASS A
INSULATION RESISTANCE	10M OHM MIN. AT 500 VDC BETWEEN FRAME AND (+) TERMINAL
DIELECTRIC STRENGTH	5mA MAX. AT AC 500 VAC 50/60 Hz ONE MINUTE BETWEEN FRAME AND (+) TERMINAL
LIFE EXPECTANCY	70,000 HOURS AT 40 °C WITH 15~65% RH.
DIRECTION OF ROTATION	COUNTER-CLOCKWISE FROM BLADE SIDE

Fan characters

FREQUENCY GENERATOR (FG) SIGNAL

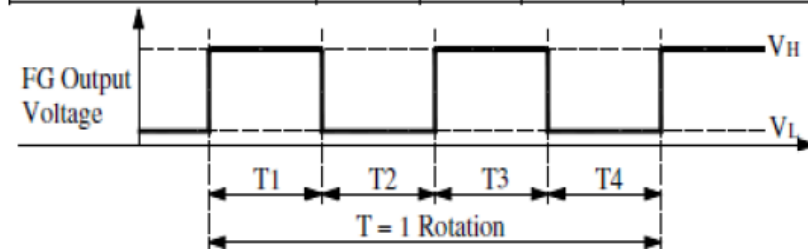


$$*R_a \geq V^+ / I_f (\text{max})$$



★Electrical Characteristics : (at $T_a = 25^\circ\text{C}$, $V_{cc} = 12\text{V}$.)

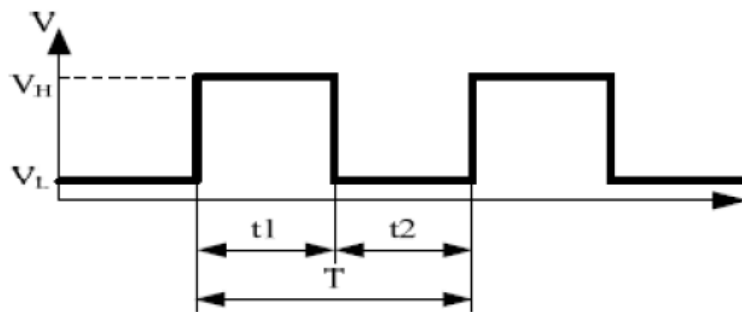
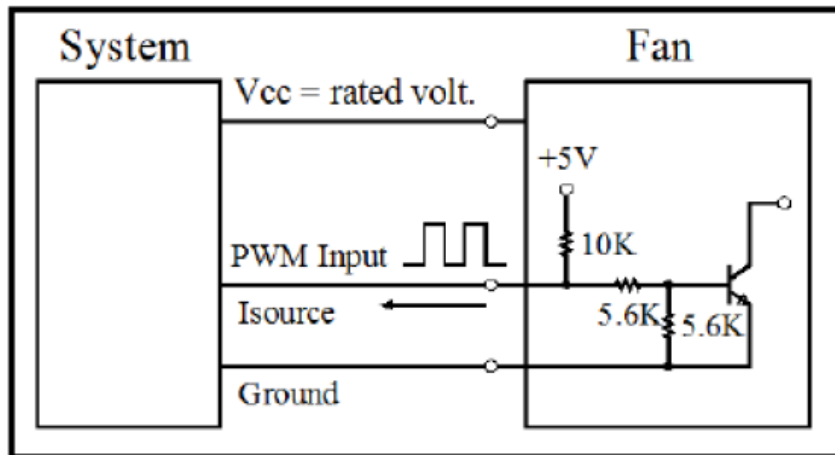
Parameter	Ratings			Unit
	min.	typ.	max.	
FG Supply Voltage(V_+)	--	--	13.2	Voltage
FG Output Current (I_f)	--	--	5	mA
FG Output (V_L)	--	--	0.6	Voltage
FG Output (V_H)	--	--	V_+	Voltage
t_1 (OFF)	--	--	9	S
t_2 (ON)	--	--	600	mS



$$T = T_1 + T_2 + T_3 + T_4 = 1 \text{ Rotation}$$

$$T = \frac{60}{\text{rpm}}$$

Fan information



1. PERIOD :
$$T = \frac{1}{f_{PWM}} = t1 + t2(\text{sec})$$

2. DUTY CYCLE (D.C.) :
$$\frac{t1}{t1+t2} * 100 = \frac{t1}{T} * 100(\%)$$

3. PWM DUTY CYCLE VS SPEED (AT TA = 25°C, VCC = 12 V , FPWM=25KHz)

PWM Duty Cycle (%)	FAN Speed (R.P.M.)
100	23000±8%
50	15700±8%
0	0

Parameter	Min	Typical	Max	Unit
f _{pwm}	22K	25K	28K	Hz
V _H	2.3	5	5.5	V
V _L	0	--	0.8	V
I _{source}	--	--	1	mA
D.C.	0	--	100	%

* The speed is default to be maximum if PWM input pin is unconnected.

* Min. start up duty cycle is 10%.

Fan PWM

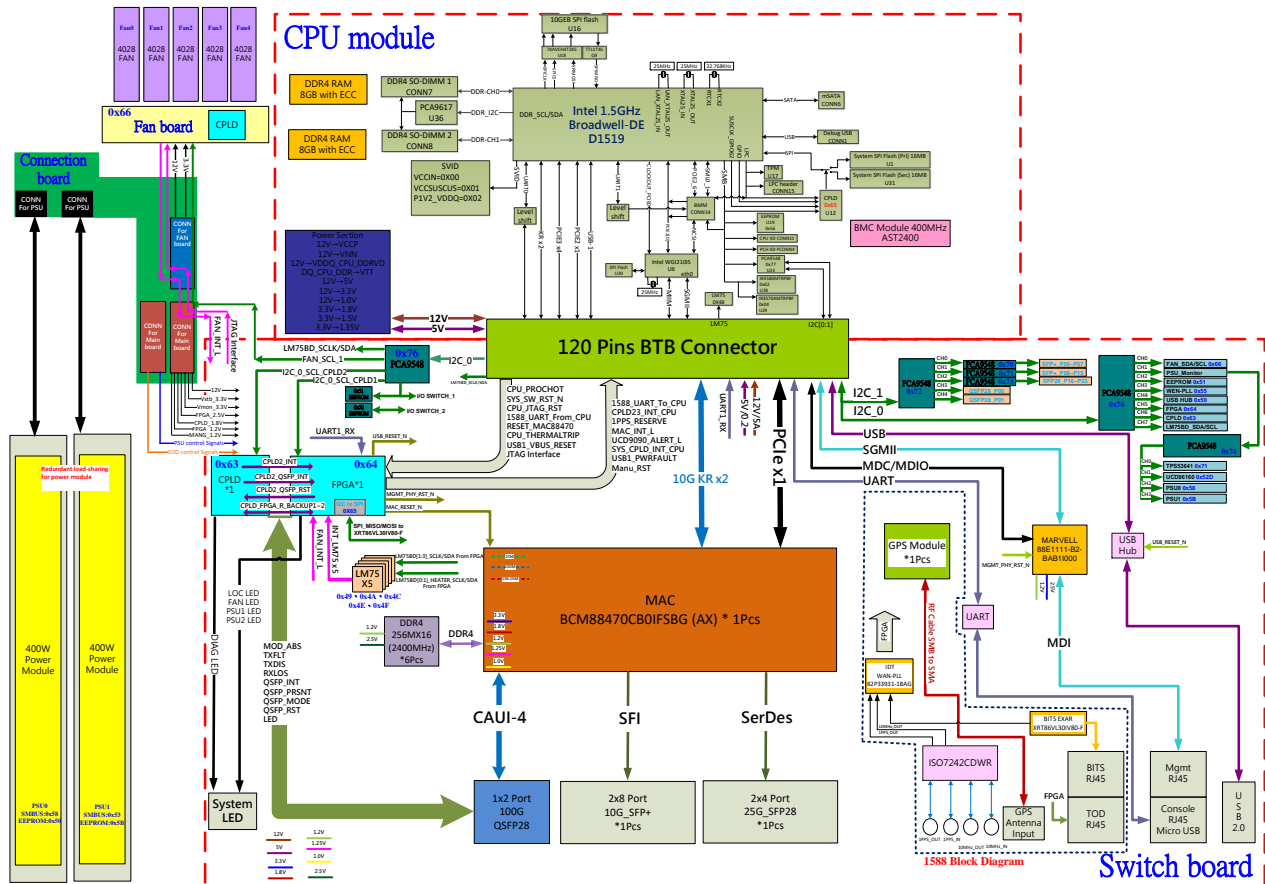
Fan Connector pinout

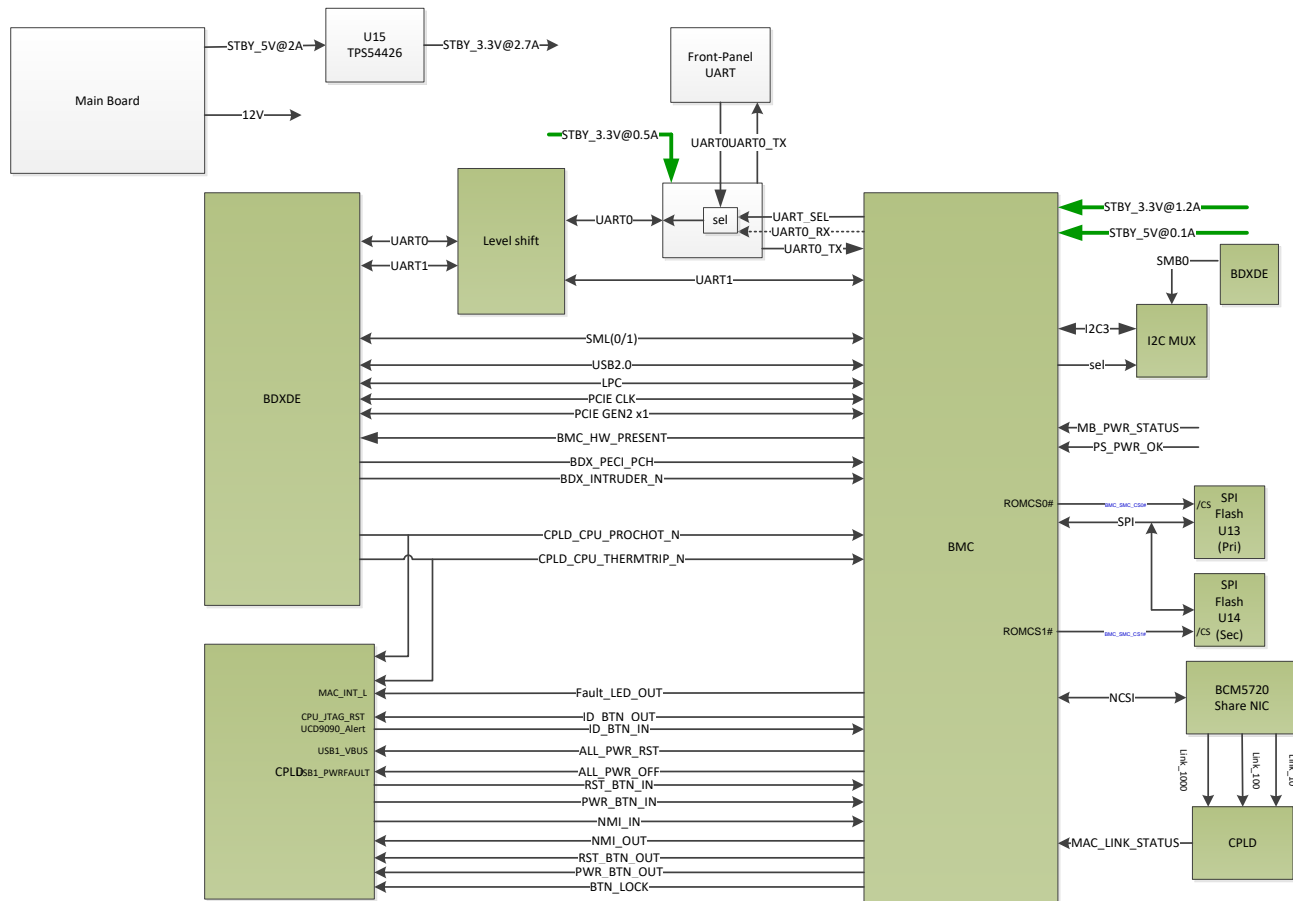
The Main board uses gold finger type to connect fan module. Here is gold finger pin mapping.

1	Reserved
2	Sensor
3	Reserved
4	PWM
5	Pin5 wire to pin6
6	Present
7	VCC12V
8	GND

System Overview:

Main PCB Block Diagram





BMC connection

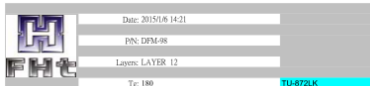
PCB Board Set

The AS7316-26X is composed of 5 unique PCB assemblies as follows:

- Main switch PCB which supports the switching silicon and all front panel connections
- X86 Broadwell-DE CPU module PCB which provides the control processor and associated components
- BMC PCB which supports the BMC controller and associated components. The BMC module plugs into the system through a connector on the CPU module
- Connection Board connecting the power supplies, the main PCB, and to the fan PCB together
- Fan PCB which provides connectivity for the 5 Fan modules in the system

PCB Stack-up

CPU board PCB Stack-up



Layer Name	Plane Description	Material	Thickness (mil)	Etch	Single-end Impedance	Single-end Width	Differential Impedance	Differential Width/Space	Differential Impedance	Differential Width/Space	Differential Impedance	Differential Width/Space	Differential Impedance	Differential Width/Space	Differential Impedance	Differential Width/Space	Differential Impedance	Differential Width/Space	Ref. Pin					
Layer 1	Solder mask	Urbia HTF plating	0.00																					
Layer 2	POW/END	Urbia HTF	0.00																					
Layer 3	Signal	Urbia HTF	0.21		40	6	50	4	68	8/8	80	5/5.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	1.26/4	
Layer 4	POW/END	Urbia HTF	0.00																					
Layer 5	Signal	Urbia HTF	0.21		40	6	50	4	68	8/8	80	5/5.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	1.48/6	
Layer 6	POW/END	Urbia HTF	0.00																					
Layer 7	Signal	Urbia HTF	0.21		40	6	50	4	68	8/8	80	5/5.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	1.08/1.1	
Layer 8	POW/END	Urbia HTF	0.00																					
Layer 9	Signal	Urbia HTF	0.21		40	6	50	4	68	8/8	80	5/5.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	1.26/2	
Layer 10	POW/END	Urbia HTF	0.00																					
Layer 11	POW/END	Urbia HTF	0.00																					
Layer 12	Solder mask	Urbia HTF plating	0.00		40	7	50	4.5	68	8/6	80	4/7	63	9/5	83	5/5	85	5/5.5	90	5/6	100	4/7	L11	
Total Thickness:			1.93																					

- 本堆棧圖之厚度係以理論值計算，或係以符合客戶規格為製作原則。All values of impedance and stack up are in tolerance calculated, the finished board should be meet customer requirement.
- 本堆棧圖之厚度，係以理論值計算，或係以符合客戶規格為製作原則。In order to meet impedance control, this design will be fine tune by process needed during the PCB fabrication and the finished should be meet IPC specification and customer requirement.
- 本堆棧圖之厚度係以理論值計算，或係以符合客戶規格為製作原則。If other the without requirement true design, we will cancel which impedance control directly when PCB production.

BMC board PCB Stack-up

Stackup Control Table										
Accoton proposed			Vendor Confirmed		Vendor verified Single-End 50 Ω ±10%		Vendor verified Diff 90 Ω ±10%		Vendor verified Diff 100 Ω ±10%	
Layer	Type	Thickness (mil)	Vendor stackup structure	Vendor thickness after lam.	Width	Sim Z0	Width/Spacing	Sim Z0	Width/Spacing	Sim Z0
1	TOP		0.6 0.5 oz + Plating	0.6 1.7	5.8	50.16	5/6/5	89.9	4/7/4	100.67
2	GND2		2116 0.5 oz	4 0.6						
3	SIG3		core 0.13 mm 0.5 oz	5.1 0.6	4.3	50.36	5/8/5	90.06	4/8/4	100.13
4	PWR9		2116HR 0.5 oz	5 0.6						
5	PWR10		core 0.077 mm 0.5 oz	3 0.6						
6	SIG6		2116HR 0.5 oz	5 0.6	4.3	50.36	5/8/5	90.06	4/8/4	100.13
7	GND17		core 0.13 mm 0.5 oz	5.1 0.6						
8	BOTTOM		2116 0.5 oz + Plating	4 1.7	5.8	50.16	5/6/5	89.9	4/7/4	100.67
	solder mask		0.6	0.6						
Board thickness (mil):		39.000	Board thickness (mil)							
		mm	mm							
		0.991	1.001							


Main board PCB Stack-up


 Date: 2016/03/15/56
 PN: DFM-26-17000-VOLT STACKUP
 Layers: LAYER 20
 Tg: 150

Layer Name	Plane Description	Remain Copper (%)	Material	Type	Value after process	Er	Dk @1GHz	Df @1GHz	Dk @5GHz	Df @5GHz	Dk @10GHz	Df @10GHz	Single-end Impedance		Single-end Impedance		Single-end Impedance		Differential Impedance		Differential Impedance		Differential Impedance		Differential Impedance		Ref. Pin	
													Impedance	Width	Impedance	Width	Impedance	Width	Impedance	Width/Space	Impedance	Width/Space	Impedance	Width/Space	Impedance	Width/Space		Impedance
Layer 1	solder mask				0.08																							
Layer 2	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016	50	5	55	4	47.5	5.5	90	50	95	4.58/5	100	3.75/5.25	95	50	L2	
Layer 2	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 3	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 3	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 4	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 4	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 5	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 5	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 6	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 6	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 7	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 7	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 8	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 8	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 9	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 9	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 10	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 10	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 11	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 11	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 12	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 12	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 13	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 13	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 14	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 14	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 15	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 15	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 16	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 16	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 17	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 17	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 18	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 18	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 19	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 19	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 20	Signal		FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Layer 20	POW/GND	80	FR4		0.08	3.3	3.6	0.001	3.58	0.0017	3.57	0.0016																
Total Thickness		2.97			1.90	0.08																						

- 疊構與阻抗均為理論計算值，成品以符合客戶規格為製作原則
All value of impedance and stack up are in simulative calculated, the finished board should be meet customer requirement.
- 為符合阻抗要求，製作時會依廠內製程參數作微調，成品需符合IPC規範與客戶要求
In order to meet impedance control, the design will be fine tune by process needed during the PCB fabrication and the finished should be meet IPC specification and customer requirement.
- 若Gerber內並無阻抗表所指定的線寬設計，製作時將直接取該阻值控制要求
If gerber file without assignment trace design, we will cancel which impedance control directly when PCB production.
- 小於50Ω的阻抗且公差規格不足±5Ω者，依廠內製程能力設定該阻值公差為±5Ω
When impedance requirement was smaller than 50Ω and which tolerance less than ±5Ω, according to our capability the tolerance for it will be default as ±5Ω.


Connection board PCB Stack-up


 Date: 2017/12/8 08:57
 PN: DFM-10-171207_POWER BOARD
 Layers: LAYER 10
 Tg: 150

Layer Name	Plane Description	Remain Copper (%)	Material	Value after process	Finish Thickness	Er	Single-end Impedance		Ref. Pin
							Impedance	Width	
Layer 1	solder mask				0.50				
Layer 1	Signal		1/2oz *Plating		1.81		50	5	L2
Layer 2	POW/GND	80	FR4	0.52	2.89	3.65			
Layer 3	POW/GND	80	FR4	0.52	2.89	4			
Layer 4	POW/GND	80	FR4	0.52	2.89	3.825			
Layer 5	POW/GND	80	FR4	0.52	2.89	4			
Layer 6	POW/GND	80	FR4	0.52	2.89	3.65			
Layer 7	POW/GND	80	FR4	0.52	2.89	4			
Layer 8	POW/GND	80	FR4	0.52	2.89	3.825			
Layer 9	POW/GND	80	FR4	0.52	2.89	4			
Layer 10	Signal		1/2oz *Plating		1.81		50	5	L9
Total Thickness		3.01		4.66	118.54				

- 疊構與阻抗均為理論計算值，成品以符合客戶規格為製作原則
All value of impedance and stack up are in simulative calculated, the finished board should be meet customer requirement.
- 為符合阻抗要求，製作時會依廠內製程參數作微調，成品需符合IPC規範與客戶要求
In order to meet impedance control, this design will be fine tune by process needed during the PCB fabrication and the finished should be meet IPC specification and customer requirement.
- 若Gerber內並無阻抗表所指定的線寬設計，製作時將直接取該阻值控制要求
If gerber file without assignment trace design, we will cancel which impedance control directly when PCB production.
- 小於50Ω的阻抗且公差規格不足±5Ω者，依廠內製程能力設定該阻值公差為±5Ω
When impedance requirement was smaller than 50Ω and which tolerance less than ±5Ω, according to our capability the tolerance for it will be default as ±5Ω.

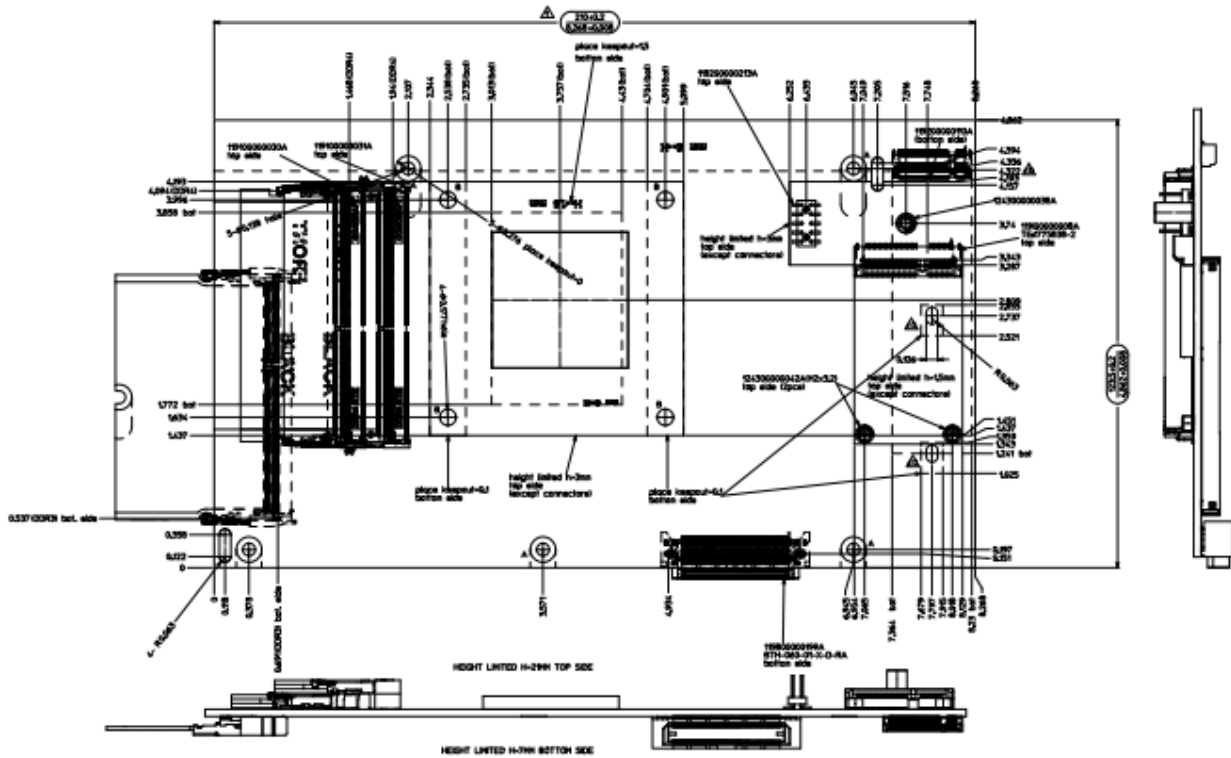
Fan board PCB Stack-up

		Date : 2014/1/13 20:54
		P/N :
		Layers : LAYER 4
		Tg : 150 NP155F · HTE-590 · IT158 · EM-825

Layer Name	Plane Description	Remain Copper (%)	reduce after pressed	Material Thickness	finish Thickness	tolerance	成本	Er	Single-end Impedance	50ohm Width	differential Impedance	100ohm Width/Space	Ref.
Layer1	solder mask			0.5									
	Signal			1.4					50	8	100	5.5/5	L2
Layer2	PREPREG			4.6	4.425	+/-1	1.16	3.85					
	POW/GND	86%	0.175	1.25									
Layer3	CORE			76.34	76.34	+/-10%	25.48	4					
	POW/GND	86%	0.175	1.25									
LAYER 4	PREPREG			4.6	4.425	+/-1	1.16	3.85					
	Signal			1.4					50	8	100	5.5/5	L3
	solder mask			0.5									
Total Thickness=		2.32	mm										
			0.35	91.84	91.49		27.8						

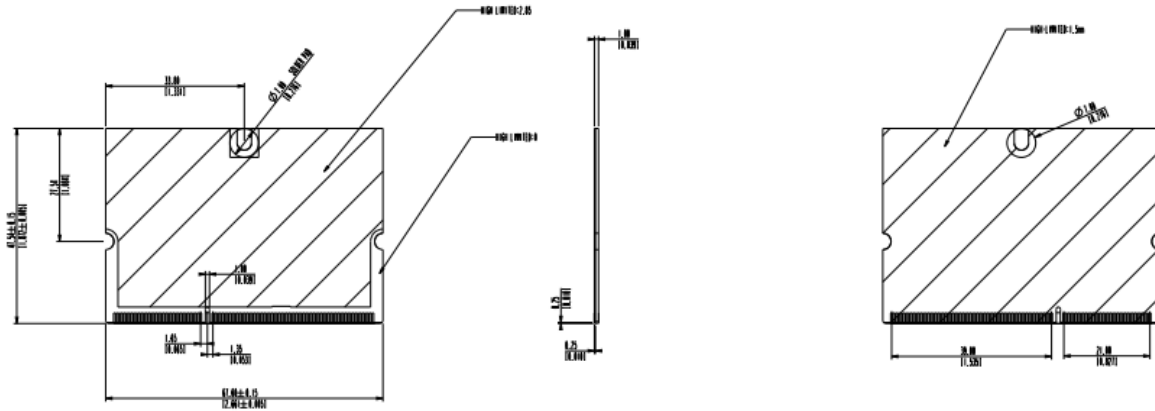
PCB Dimensions CPU board PCB Dimension

■ CPU_L x W = 123.5mm x 210mm



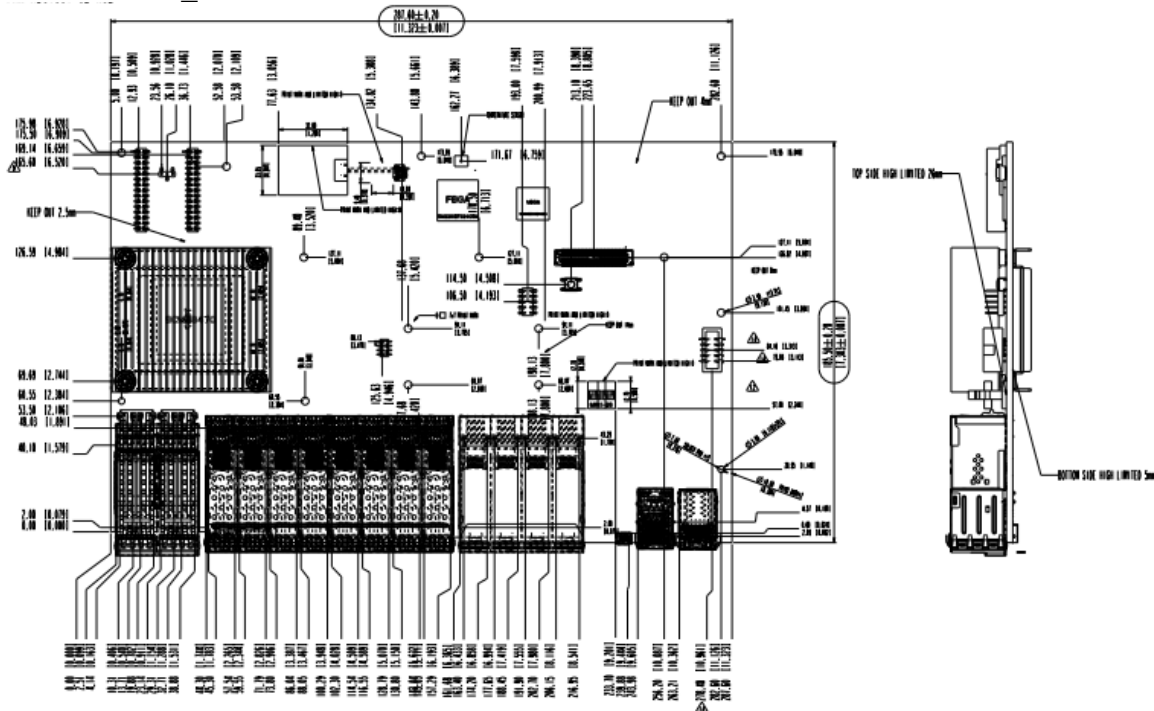
BMC board PCB Dimension

- BMC_L x W = 47.54mm x 67.6mm



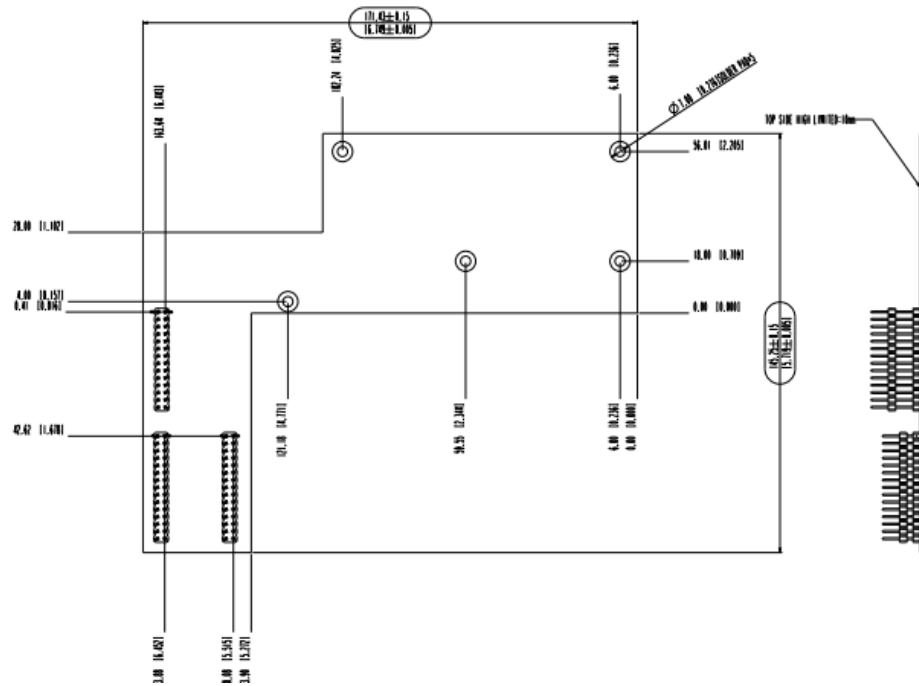
Main board PCB Dimension

- Main_L x W = 185.5mm x 287.6mm



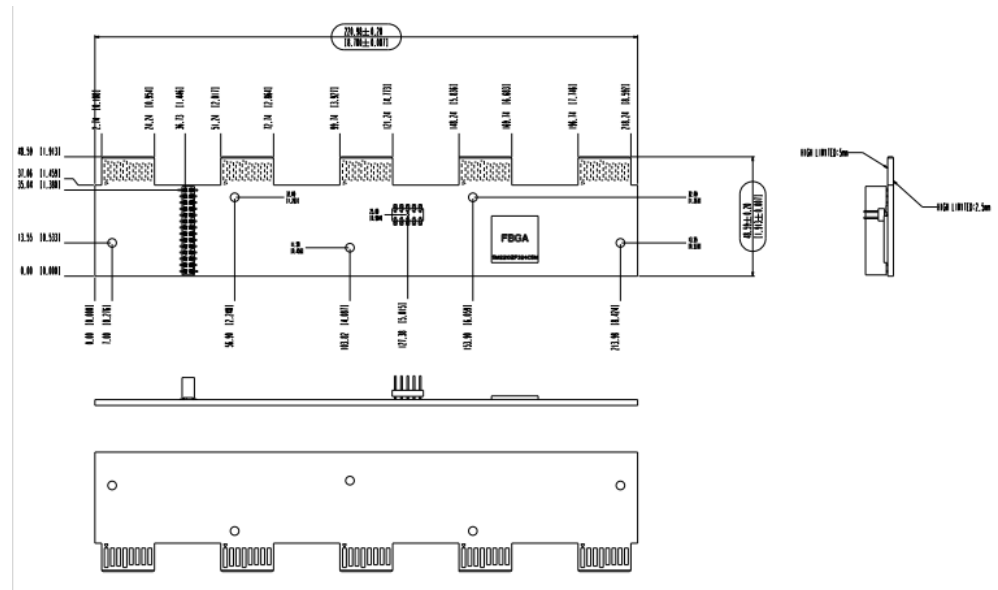
Connection board PCB Dimension

- Connection_L x W = 145.25mm x 171.43mm

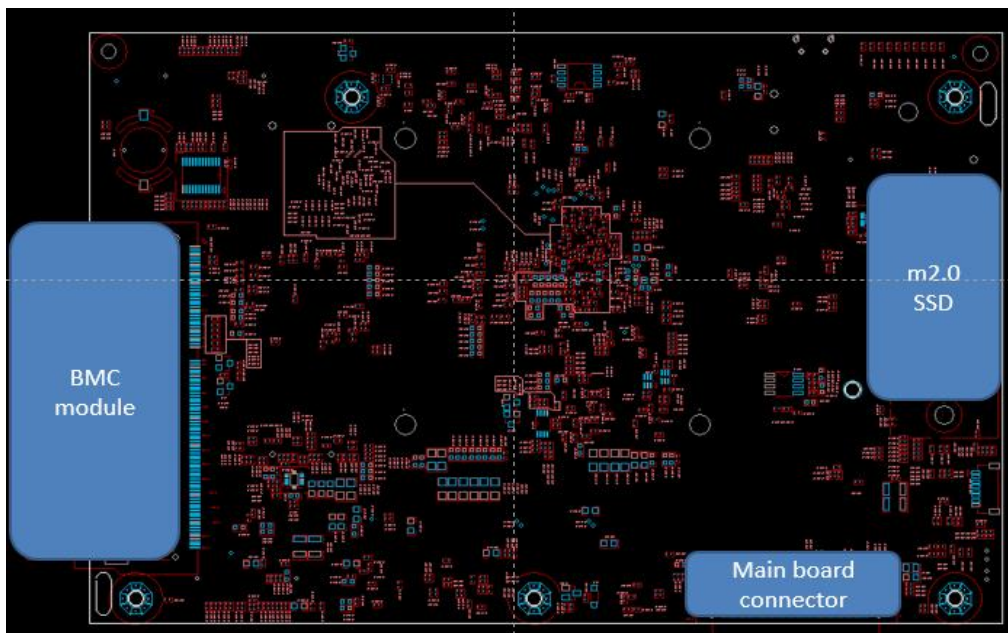
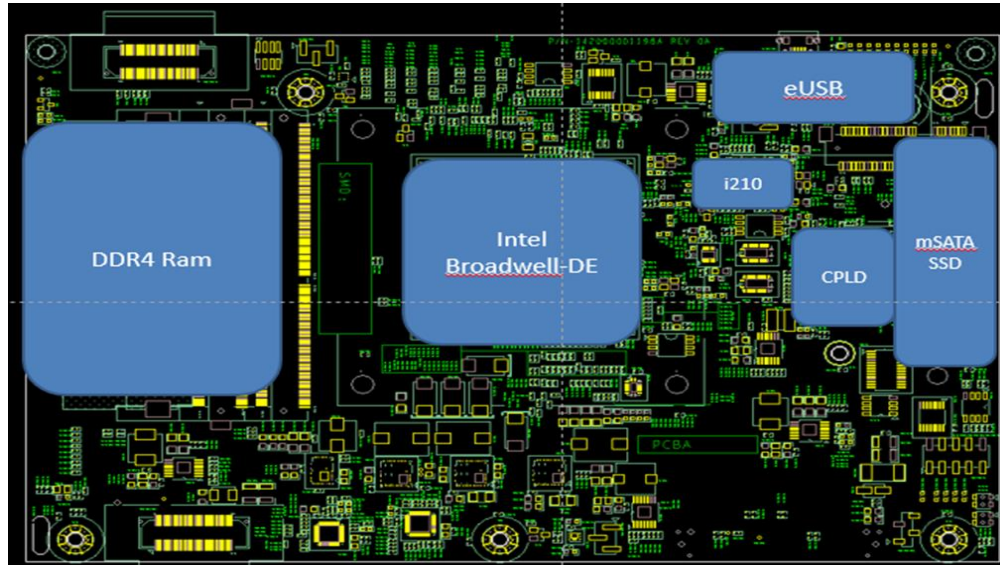


FAN board PCB Dimension

- FAN_L x W = 48.59mm x 220.98mm

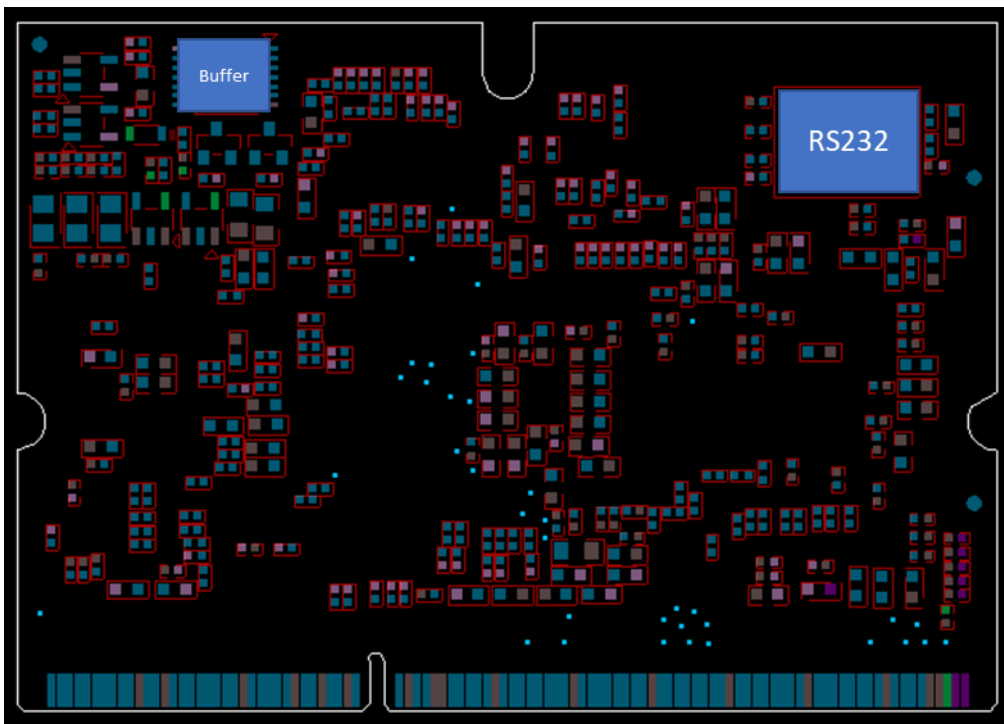
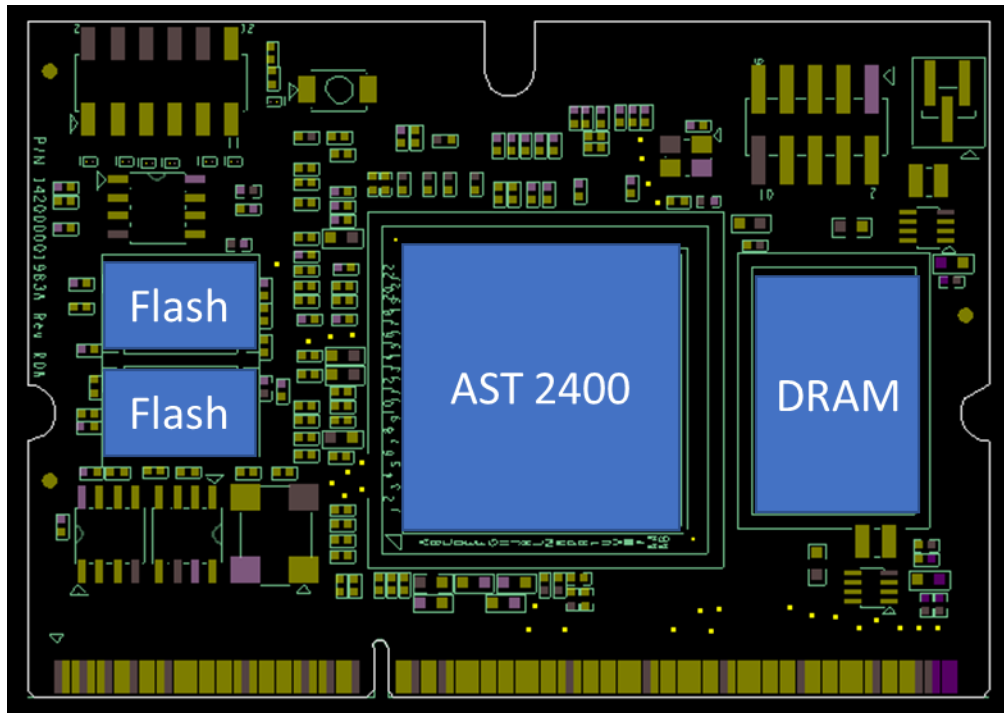


Placement
CPU board:



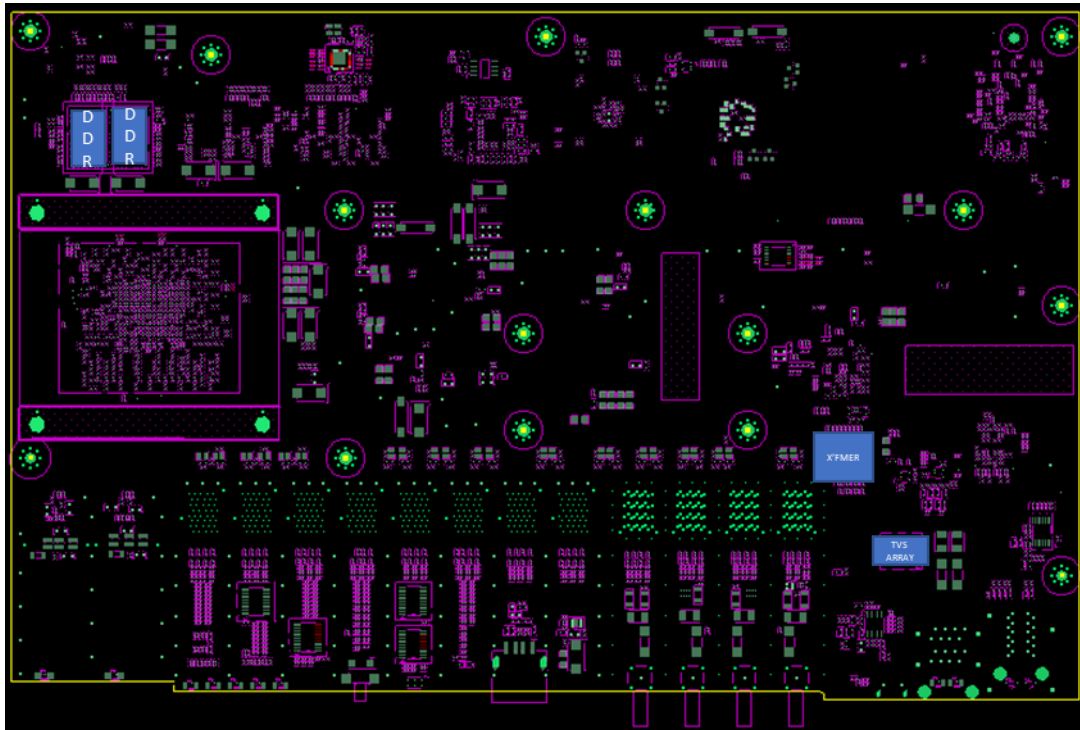
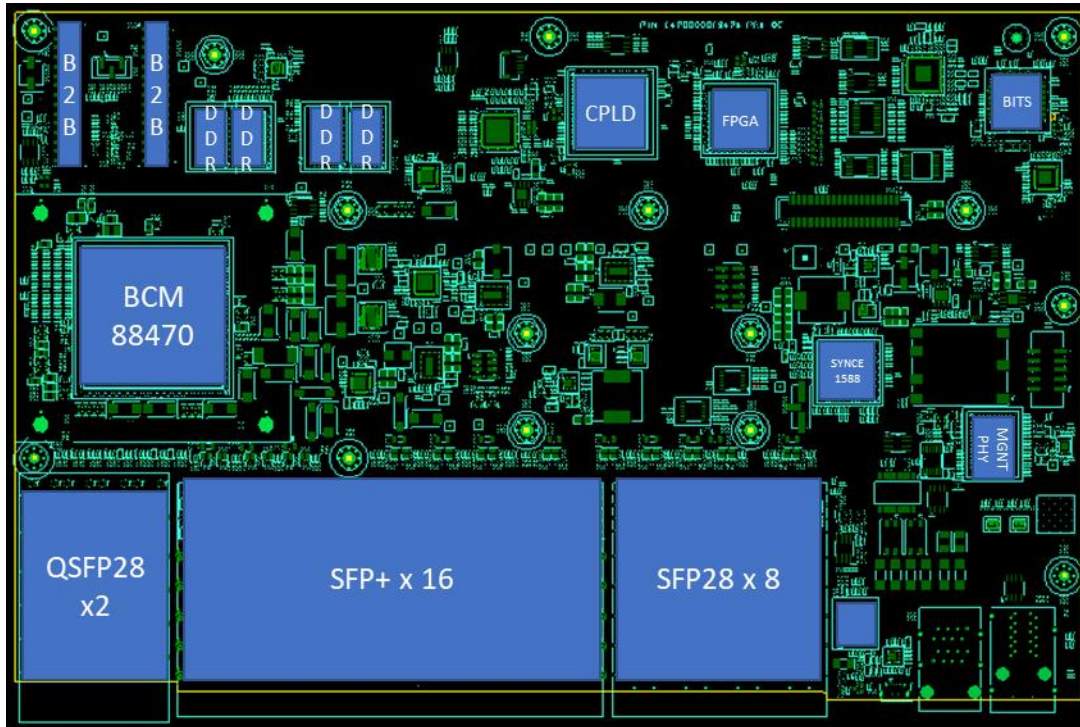
CPU Board TOP/Bottom PCB Placement

BMC board:



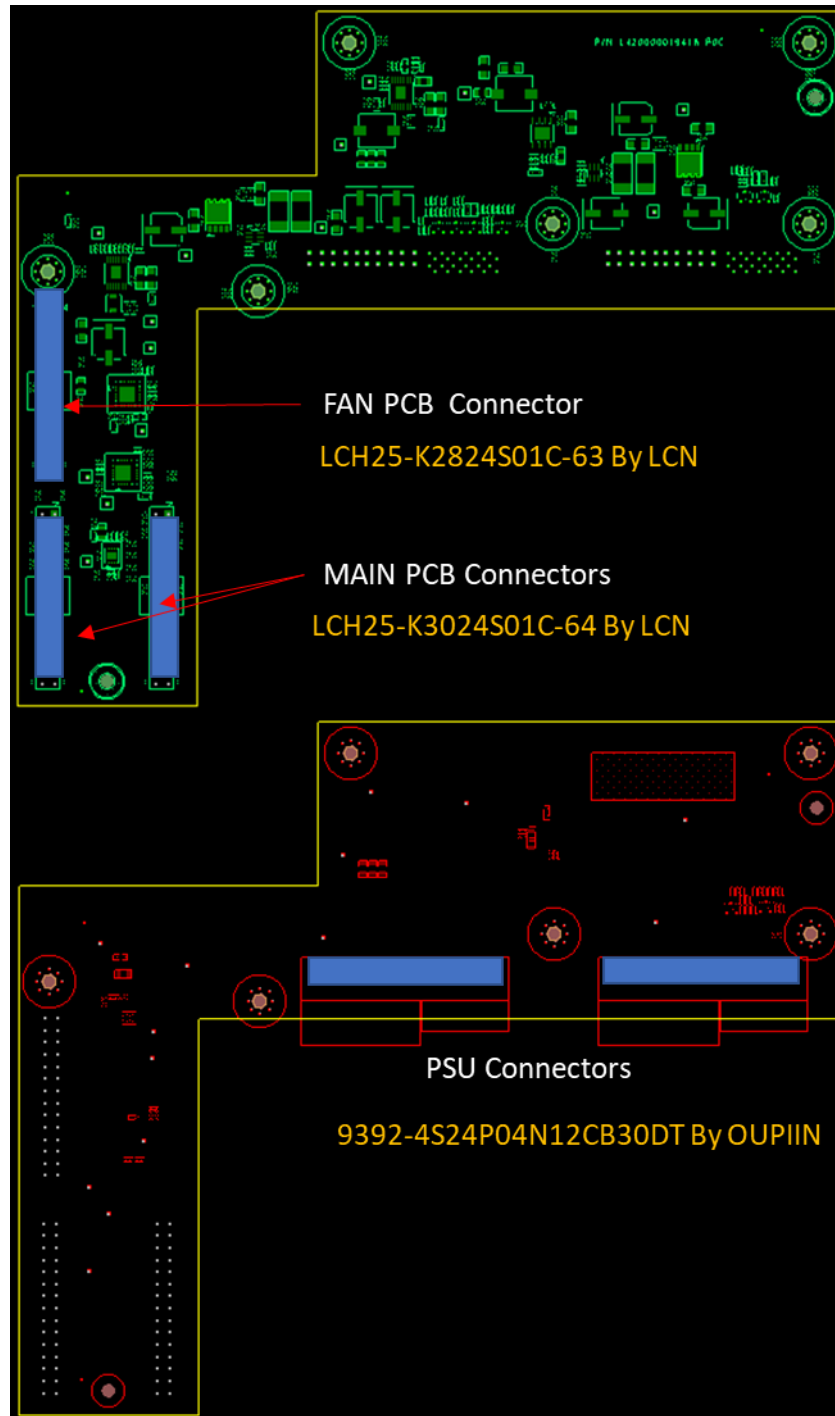
BMC Board TOP/Bottom PCB Placement

Main board:



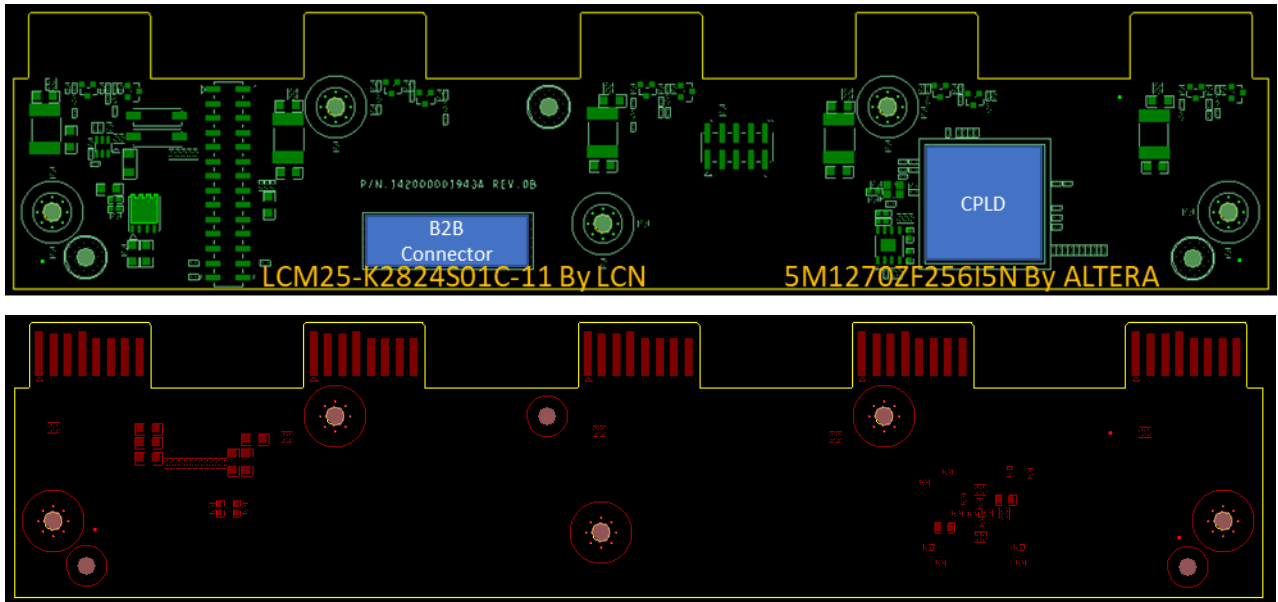
Main board TOP/Bottom PCB Placement

Power Connection board:



Connection board TOP/Bottom PCB Placement

FAN board:



FAN board TOP/Bottom PCB Placement

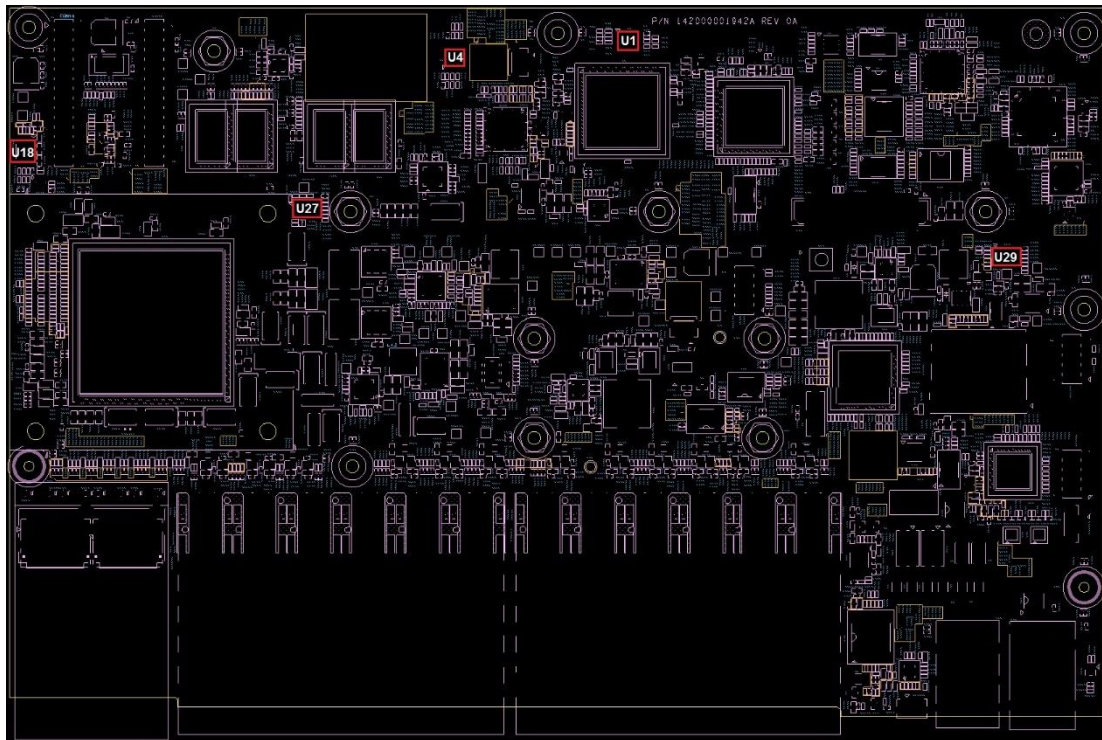
120 Pin CPU PCB to Main PCB Connector

ES7632BT 120 Pin	ES7632BT 120 Pin	General Function	CONNECTOR				General Function	ES7632BT 120 Pin	ES7632BT 120 Pin
			IN/OUT	PIN #	PIN #	IN/OUT			
(D)LM75BD_SCLK	IN	TEMP_ANODE	IN/OUT	119	120	OUT	I2C_2_SCL	IN	I2C_1_SCL
(O)LM75BD_SDA	IN/OUT	TEMP_CATHODE	IN/OUT	117	118	IN	MGMT_RS232_DCD	IN	CPU_PROCHOT
GND		GND	-	115	116	IN/OUT	GPIO		Not Used
CPU_MPHY_SGMII_TX_0_S_P	OUT	MPHY_SGMII_TX_P	OUT	113	114	IN/OUT	I2C_2_SDA	IN/OUT	I2C_1_SDA
CPU_MPHY_SGMII_TX_0_S_N	OUT	MPHY_SGMII_TX_N	OUT	111	112	IN/OUT	GPIO		Not Used
GND		GND	-	109	110	IN	INTERRUPT		GND
MPHY_CPU_SGMII_RX_0_S_N	IN	MPHY_SGMII_RX_N	IN	107	108	IN	INTERRUPT	OUT	PCIE_OOB_TX_P
MPHY_CPU_SGMII_RX_0_S_P	IN	MPHY_SGMII_RX_P	IN	105	106	OUT	MGMT_RS232_DTR	OUT	PCIE_OOB_TX_N
GND		GND	-	103	104	IN/OUT	PROCHOT#		GND
CPU_MPHY_MDC	OUT	GPIO(MPHY_MDC)	OUT	101	102	IN/OUT	GPIO	IN	PCIE_OOB_RX_P
Not Used		INTERRUPT(MPHY)	IN	99	100	OUT	THRMTRIP#	IN	PCIE_OOB_RX_N
CPU_MPHY_MDIO	IN/OUT	GPIO(MPHY_MDIO)	IN/OUT	97	98	IN	INTERRUPT		GND
GND		GND	-	95	96	IN	MGMT_RS232_RXD	IN	UART1_RX
IP_UART0_SOUT	IN	GPIO	IN/OUT	93	94	IN	MGMT_RS232_CTS	IN	UART1_CTS
CPLD23_INT_CPU	IN		IN	91	92	IN	INTERRUPT	IN	CPU_TDI
1PPS_CPU	IN	GPIO	IN/OUT	89	90	OUT	MGMT_RS232_TXD	OUT	UART1_TX
GND		GND	-	87	88	IN	INTERRUPT	IN	MAC_INT_L
GND		GND	-	85	86	-	GND		GND
CPU_XFI_BC_TX_0P	OUT	DIFF_PAIR_TX_0_P	OUT	83	84	IN/OUT	MGMT_USB_N	IN/OUT	USB2_N
CPU_XFI_BC_TX_0N	OUT	DIFF_PAIR_TX_0_N	OUT	81	82	IN/OUT	MGMT_USB_P	IN/OUT	USB2_P
GND		GND	-	79	80	-	GND		GND
GND		GND	-	77	78	OUT	HWIO	OUT	UCD9090_ALERT_L
CPU_XFI_EC_RX_0P	IN	DIFF_PAIR_RX_0_P	IN	75	76	OUT	MGMT_RS232_RTS	OUT	UART1_RTS
CPU_XFI_EC_RX_0N	IN	DIFF_PAIR_RX_0_N	IN	73	74	OUT	HWIO	OUT	RESET_SYS_CPLD
GND		GND	-	71	72	IN/OUT	GPIO	OUT	CPU_TMS
GND		GND	-	69	70	OUT	JTAG_TRST#	OUT	CPU_JTAG_RST
CPU_XFI_EC_RX_2P	IN	DIFF_PAIR_RX_1_P	IN	67	68	OUT	HWIO	IN	PI014_RST
CPU_XFI_EC_RX_2N	IN	DIFF_PAIR_RX_1_N	IN	65	66	IN/OUT	GPIO	OUT	CPU_TDO
GND		GND	-	63	64	IN/OUT	GPIO	OUT	CPU_TCK
GND		GND	-	61	62	IN/OUT	GPIO	OUT	IP_UART0_SIN
CPU_XFI_EC_TX_2P	OUT	DIFF_PAIR_TX_1_P	OUT	59	60	IN/OUT	I2C_0_SDA		Not Used
CPU_XFI_EC_TX_2N	OUT	DIFF_PAIR_TX_1_N	OUT	57	58	OUT	I2C_0_SCL		Not Used
GND		GND	-	55	56	IN	INTERRUPT	IN	SYS_CPLD_INT_CPU
GND		GND	-	53	54	OUT	HWIO	IN	USB1_PWRFAULT
CPU_PEX_PCIEA_TX_0_P	OUT	PCIE_TX_2_P	OUT	51	52	IN	RESET_MODULE_REQ#	IN	Manu_RST
CPU_PEX_PCIEA_TX_0_N	OUT	PCIE_TX_2_N	OUT	49	50	OUT	I2C_1_SCL	OUT	I2C_0_SCL
GND		GND	-	47	48	IN/OUT	I2C_1_SDA	IN/OUT	I2C_0_SDA
GND		GND	-	45	46	OUT	RESET_SYS_REQ#	OUT	RESET_MAC
CPU_PEX_PCIEA_TX_1_N	OUT	PCIE_TX_3_P	OUT	43	44	IN	SYS_PWR_GOOD	OUT	CPU_THERMALTRIP
CPU_PEX_PCIEA_TX_1_P	OUT	PCIE_TX_3_N	OUT	41	42	OUT	HWIO	OUT	USB1_VBUS
GND		GND	-	39	40	-	GND		GND
GND		GND	-	37	38	-	GND		GND
PEX_CPU_PCIEA_RX_0_N	IN	PCIE_RX_2_P	IN	35	36	OUT	PCIE_TX_0_P	OUT	CPU_PEX_PCIEB_TX_0_P
PEX_CPU_PCIEA_RX_0_P	IN	PCIE_RX_2_N	IN	33	34	OUT	PCIE_TX_0_N	OUT	CPU_PEX_PCIEB_TX_0_N
GND		GND	-	31	32	-	GND		GND
GND		GND	-	29	30	-	GND		GND
PEX_CPU_PCIEA_RX_1_N	IN	PCIE_RX_3_P	IN	27	28	IN	PCIE_RX_0_P	IN	PEX_CPU_PCIEB_RX_0_P
PEX_CPU_PCIEA_RX_1_P	IN	PCIE_RX_3_N	IN	25	26	IN	PCIE_RX_0_N	IN	PEX_CPU_PCIEB_RX_0_N
GND		GND	-	23	24	-	GND		GND
GND		GND	-	21	22	-	GND		GND
CPU_PEX_PCIEB_TX_1_N	OUT	PCIE_TX_1_P	OUT	19	20	IN	PCIE_RX_1_P	IN	PEX_CPU_PCIEB_RX_1_P
CPU_PEX_PCIEB_TX_1_P	OUT	PCIE_TX_1_N	OUT	17	18	IN	PCIE_RX_1_N	IN	PEX_CPU_PCIEB_RX_1_N
GND		GND	-	15	16	-	GND		GND
GND		GND	-	13	14	-	GND		GND
GND		GND	-	11	12	-	GND		GND
VCC12		12VDC	-	9	10	-	12VDC		VCC12
VCC12		12VDC	-	7	8	-	12VDC		VCC12
VCC5P0		5VDC	-	5	6	-	12VDC		VCC12
VCC5P0		5VDC	-	3	4	-	12VDC		VCC12
VCC5P0		5VDC	-	1	2	-	12VDC		VCC12

Thermal Monitoring

The AS7316-26X contains 5 system fans used to cool device. The system is also designed with several temperature sensors to detect temperature at several locations within the system. The system supports three temperature sensors on the main PCB board and one temperature sensor on the CPU board.

Main PCB Thermal sensor locations



LM75 sensor location.

- U1 is at rear of main board
- U4 is under BMC
- U18 is behind the MAC.
- U27 locates to MAC right upper corner.
- U29 locates Main board right side.

Heater function

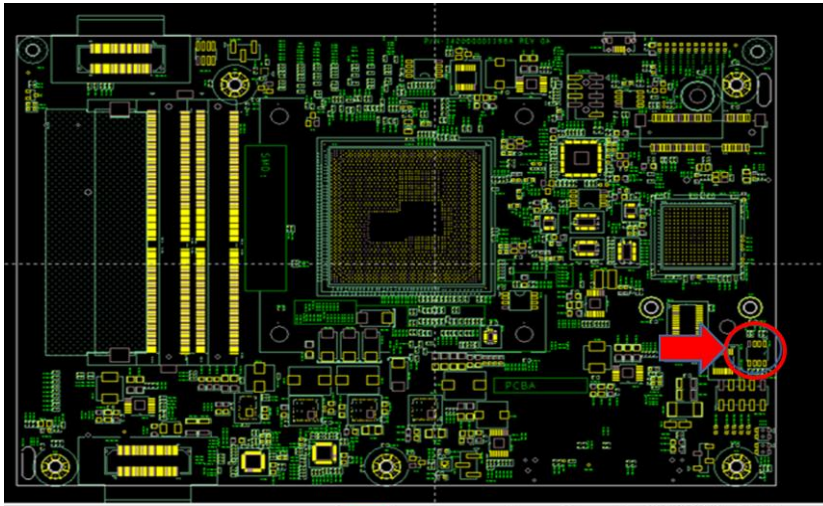
The operating temperature of AS7316-26X is -40°C to 65°C . There is BMC IC (AST2500) belong to commercial grade which must be pre-heated by heater to reach system operating temperature.

One thermal sensor LM75 (U4) puts under BMC IC for detecting temperature. Then, the FPGA will detect U4 temperature to enable/disable heater function.

A thermal sensor LM75 at location U29 on main board is used for detecting temperature accurately. There is no heating impact at U29 from result of thermal simulation. Therefore, the U29 is as ambient temperature reference to enable/disable fan function. Once the fan function is enabled, the fan control algorithm will utilize LM75 (U18/U27/U29) temperature data to control fan speed.

Heating time: from -40°C to 0°C is around 4-6 minutes

X86 Broadwell-DE CPU Module thermal sensor location



Power Consumption

Power Consumption Estimation Table / CURRENT (max) Per Device (A)																				
Device	Voltage(V)																	Quantity	Unity(%)	Total(W)
	12	5	3.3	1.8	2.5	for MPHY	0.75	1.5	1.538	1.35	1.25	1.2	0.6	1.1	1	0.95				
CPU Module is below																				
Intel BDXXDE CPU D1519			3.58700	0.35000				0.16200		3.50000		3.00000				16.98600	1.00	38.02110		
DDR4 Module 8GB ECC SODIMM Transcend TS1GSH7ZV1H-I												2.55200	0.75000				2.00	7.02480		
INTEL WG1210IS			0.35900														1.00	1.18470		
m-SATA SSD 32GB Transcend TS128EPTDE1500I			0.18200														1.00	0.60060		
CPLD			0.50000														1.00	1.65000		
SPI Flash			0.05000														4.00	0.66000		
NAND Flash			0.05000														0.00	0.00000		
BMC Module																				
AST2400			0.19100						0.45200								1.00	1.32548		
DDR3 Nanya NT5CC128M16IP-DI 128MX16									0.52500								1.00	0.80745		
RTL8211E			0.65000														1.00	2.14500		
Main Board is below																				
Broadcom BCM88470CB0IFSBG			0.20000	1.20500							0.76800	1.14300				52.25500	1.00	57.41560		
DDR4 Hynix H5AN4G6NAFR-UH1 256MX16					0.33300							0.42500					6.00	8.05500		
MARVELL 88E1111-B2-BAB11000						0.92000						0.20000					1.00	2.54000		
CPLD (Altera 5M2210ZF32415N)			0.25000														1.00	0.82500		
FPGA (Altera 10M08DCU32417G)			0.30000		0.15000							1.10000					1.00	2.68500		
IDT 82P33931-1BAG (SYNCE+1588)			0.90000	0.09000													1.00	3.13200		
IDT CLK Generator (8V49NS0412NLG18)			0.90000														1.00	2.97000		
IDT CLK Generator (8V43N104NLG18)			0.25000														1.00	0.82500		
BITS (Maxim DS26503LN+)			0.15000														1.00	0.49500		
OCXO 25MHz (Rakon STP 2921 LF)			1.10000														1.00	3.63000		
USB Connector & USB2.0 Hub Controller			1.00000	0.32000													1.00	6.05600		
10G_SFP+ Transceiver				0.45400													24.00	35.95680		
100G_QSFP28+ Transceiver				1.50000													2.00	9.90000		
GPS Module (Trimble_67974-00)				0.12000													1.00	0.39600		
Fan Board																				
FAN Module	1.50000																5.00	90.00000		
CPLD (Altera 5M1270ZF2515N)				0.25000													1.00	0.82500		
SFP+ / QSFP LEDs				0.03000													26.00	2.57400		
QSFP fan out LED				0.05000													8.00	1.32000		
ToD/BITS/MGMT LEDs				0.02500													4.00	0.33000		
SYS LEDs				0.02500													5.00	0.41250		
Other Specific IC				0.50000													1.00	1.65000		
Heater	1.25000																2.00	30.00000		
Total Current (A)	10.00000	1.00000	26.21000	1.64500	2.14800	0.92000	0.00000	0.16200	0.97700	3.50000	0.76800	13.09700	1.50000	0.00000	69.24100	0.00000		315.41203		
Voltage Tolerantion (%)	5%		5%									5%			3%	3%				
PSU Efficiency (84%)																		375.49051		
PSU Efficiency (85%)																		371.07297		
PSU Efficiency (86%)																		366.75817		

PSU input need watt

Switch Silicon configuration

Port mapping

Below show BCM88470 Network Interface block diagram and NIF SerDes Interface mapping, PM25-2/3 runs at 100G per port and design for two of uplink port that connects to QSFP28 connector. The PM25-0/1 runs at 25G per port and connects to 2x4 SFP28 connector. Other NIFE SerDes configures as 10GbE that connects to SFP+ connector.

PM#	Interface	SFP+/SFP28/ QSFP28	Physical Port	Logical Port	MAC		
					Device	Lane	Interface
PM10-7	SerDes	SFP+	0	xe1	BCM88470	2	NIFE_TX[30]_P/N
	SerDes	SFP+	1	xe2	BCM88470	3	NIFE_RX[30]_P/N
	SerDes	SFP+					NIFE_TX[31]_P/N

							NIFE_RX[31]_P/N
	SerDes	SFP+	2	xe3	BCM88470	0	NIFE_TX[28]_P/N
							NIFE_RX[28]_P/N
	SerDes	SFP+	3	xe4	BCM88470	1	NIFE_TX[29]_P/N
							NIFE_RX[29]_P/N
PM10Q-6	SerDes	SFP+	4	xe5	BCM88470	1	NIFE_TX[25]_P/N
							NIFE_RX[25]_P/N
	SerDes	SFP+	5	xe6	BCM88470	0	NIFE_TX[24]_P/N
							NIFE_RX[24]_P/N
	SerDes	SFP+	6	xe7	BCM88470	3	NIFE_TX[27]_P/N
							NIFE_RX[27]_P/N
	SerDes	SFP+	7	xe8	BCM88470	2	NIFE_TX[26]_P/N
							NIFE_RX[26]_P/N
PM10Q-5	SerDes	SFP+	8	xe9	BCM88470	2	NIFE_TX[22]_P/N
							NIFE_RX[22]_P/N
	SerDes	SFP+	9	xe10	BCM88470	3	NIFE_TX[23]_P/N
							NIFE_RX[23]_P/N
	SerDes	SFP+	10	xe11	BCM88470	0	NIFE_TX[20]_P/N
							NIFE_RX[20]_P/N
	SerDes	SFP+	11	xe12	BCM88470	1	NIFE_TX[21]_P/N
							NIFE_RX[21]_P/N
PM10Q-4	SerDes	SFP+	12	xe13	BCM88470	2	NIFE_TX[18]_P/N
							NIFE_RX[18]_P/N
	SerDes	SFP+	13	xe14	BCM88470	3	NIFE_TX[19]_P/N
							NIFE_RX[19]_P/N
	SerDes	SFP+	14	xe15	BCM88470	0	NIFE_TX[16]_P/N
							NIFE_RX[16]_P/N
	SerDes	SFP+	15	xe16	BCM88470	1	NIFE_TX[17]_P/N
							NIFE_RX[17]_P/N
PM25-0	SerDes	SFP28	16	ce17	BCM88470	1	NIF_P/N_TX[01]
							NIF_P/N_RX[01]
	SerDes	SFP28	17	ce18	BCM88470	0	NIF_P/N_TX[00]
							NIF_P/N_RX[00]
	SerDes	SFP28	18	ce19	BCM88470	3	NIF_P/N_TX[03]
							NIF_P/N_RX[03]
	SerDes	SFP28	19	ce20	BCM88470	2	NIF_P/N_TX[02]

							NIF_P/N_RX[02]
PM25-1	SerDes	SFP28	20	ce21	BCM88470	1	NIF_P/N_TX[05]
							NIF_P/N_RX[05]
	SerDes	SFP28	21	ce22	BCM88470	0	NIF_P/N_TX[04]
							NIF_P/N_RX[04]
	SerDes	SFP28	22	ce23	BCM88470	3	NIF_P/N_TX[07]
							NIF_P/N_RX[07]
	SerDes	SFP28	23	ce24	BCM88470	2	NIF_P/N_TX[06]
							NIF_P/N_RX[06]
PM25-3	SerDes	QSFP28	0	ce25	BCM88470	3	NIF_TX[15]_P/N
							NIF_RX[15]_P/N
						2	NIF_TX[14]_P/N
							NIF_RX[14]_P/N
						1	NIF_TX[13]_P/N
							NIF_RX[13]_P/N
						0	NIF_TX[12]_P/N
							NIF_RX[12]_P/N
PM25-2	SerDes	QSFP28	1	ce26	BCM88470	3	NIF_TX[11]_P/N
							NIF_RX[11]_P/N
						2	NIF_TX[10]_P/N
							NIF_RX[10]_P/N
						1	NIF_TX[09]_P/N
							NIF_RX[09]_P/N
						0	NIF_TX[08]_P/N
							NIF_RX[08]_P/N

Table 1 NIF/NIFE mapping Table

CAUI-4 interface

The PM25-2 and PM25-3 run a 100GbE ports with CAUI-4 interface and directly connects to QSFP28 ports.

The PM25-0 and PM25-1 run a 25GbE ports with CAUI-4 interface and directly connects to SFP28 ports.

10G KR interface

The PM10-11 runs at 10GbE ports with KR interface and directly connects to CPU for packet transmission between CPU and MAC.

LED stream

BCM88470 has two-wire (clock and data) LED interface is to control network port LEDs. Both signals are held low during periods of inactivity. A single LED refresh cycle consists of clocking out a programmable

number of LED data bits. The LED data signal is pulsed high at the start of each LED refresh cycle, this selection defines the Led stream.

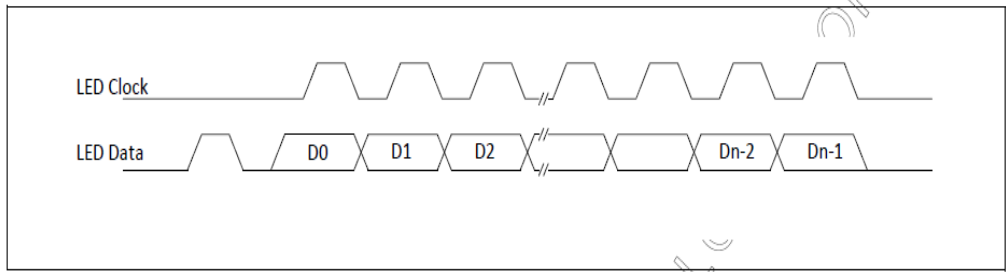
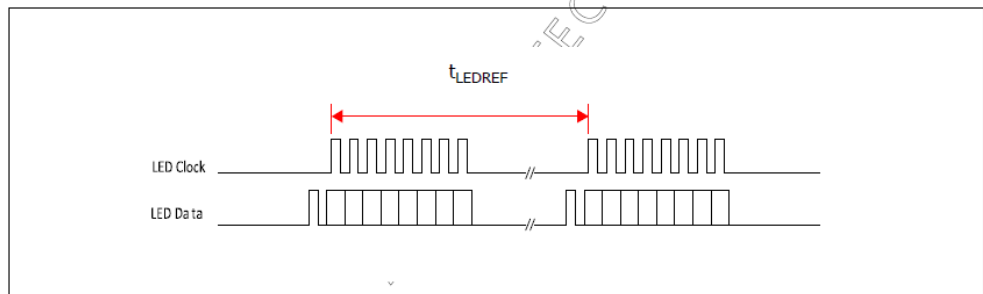


Figure 13: LED Refresh Timing



3 Led Refresh cycle

The table shows LED stream from BCM88470 to CPLD then decode by CPLD. CPLD base on decode result to indicate each port LED status.

0	1	2	3	4	5	6	7	8	9	10	11	12	13
Port 25		Port 25 Lane 0			Port 25 Lane 1			Port 25 Lane 2			Port 25 Lane 3		
Lane[1:0]		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity
14	15	16	17	18	19	20	21	22	23	24	25	26	27
Port 26		Port 26 Lane 0			Port 26 Lane 1			Port 26 Lane 2			Port 26 Lane 3		
Lane[1:0]		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity
28	29	30	31	32	33	34	35	36	37	38	39	40	41
Lane[1:0]		Port 1			Port 2			Port 3			Port 4		
		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity
42	43	44	45	46	47	48	49	50	51	52	53	54	55
Lane[1:0]		Port 5			Port 6			Port 7			Port 8		
		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity
56	57	58	59	60	61	62	63	64	65	66	67	68	69
Lane[1:0]		Port 9			Port 10			Port 11			Port 12		
		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity
70	71	72	73	74	75	76	77	78	79	80	81	82	83
Lane[1:0]		Port 13			Port 14			Port 15			Port 16		
		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity
84	85	86	87	88	89	90	91	92	93	94	95	96	97
Lane[1:0]		Port 17			Port 18			Port 19			Port 20		
		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity
98	99	100	101	102	103	104	105	106	107	108	109	110	111
Lane[1:0]		Port 21			Port 22			Port 23			Port 24		
		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity

LED Stream bit define

Lane speed	Speed [1:0]	Lane Number	Lane [1:0]
1G	11	reserve	11
25G	10	4	10
20G	01	2	01
10G	00	1	00

Port configuration	Lane [1:0]	Speed [1:0]
100G	10	10
40G	10	00
10G	00	00
1G	00	11
4 x 25G	00	10
2 x 50G	01	10

	LED
--	-----

Link-up/ Activity	
<u>1</u>	<u>ON</u>
<u>0</u>	<u>OFF</u>
Toggle	Activity

Below table shows default value of LED stream.

0	1	2	3	4	5	6	7	8	9	10	11	12	13
Port 25		Port 25 Lane 0			Port 25 Lane 1			Port 25 Lane 2			Port 25 Lane 3		
0	Lane[1:0] 1	0	Speed [1:0] 1	Link-up/ Activity 0	0	Speed [1:0] 1	Link-up/ Activity 0	0	Speed [1:0] 1	Link-up/ Activity 0	0	Speed [1:0] 1	Link-up/ Activity 0
14	15	16	17	18	19	20	21	22	23	24	25	26	27
Port 26		Port 26 Lane 0			Port 26 Lane 1			Port 26 Lane 2			Port 26 Lane 3		
0	Lane[1:0] 1	0	Speed [1:0] 1	Link-up/ Activity 0	0	Speed [1:0] 1	Link-up/ Activity 0	0	Speed [1:0] 1	Link-up/ Activity 0	0	Speed [1:0] 1	Link-up/ Activity 0
28	29	30	31	32	33	34	35	36	37	38	39	40	41
Port 1		Port 2			Port 3			Port 4					
0	Lane[1:0] 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0
42	43	44	45	46	47	48	49	50	51	52	53	54	55
Port 5		Port 6			Port 7			Port 8					
0	Lane[1:0] 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0
56	57	58	59	60	61	62	63	64	65	66	67	68	69
Port 9		Port 10			Port 11			Port 12					
0	Lane[1:0] 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0
70	71	72	73	74	75	76	77	78	79	80	81	82	83
Port 13		Port 14			Port 15			Port 16					
0	Lane[1:0] 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0
84	85	86	87	88	89	90	91	92	93	94	95	96	97
Port 17		Port 18			Port 19			Port 20					
0	Lane[1:0] 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0
98	99	100	101	102	103	104	105	106	107	108	109	110	111
Port 21		Port 22			Port 23			Port 24					
0	Lane[1:0] 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0	0	Speed [1:0] 0	Link-up/ Activity 0

Software Support

The AS7316-26X supports a base software package composed of the following components:

BIOS support

The AS7316-26X Supports AMI AptioV BIOS version A01 or greater with the x86 CPU module

ONIE

See <https://github.com/opencomputeproject/onie/tree/master/machine/accton> for the latest supported version

Open Network Linux

See <http://opennetlinux.org/> for latest supported version

Specifications

Power Consumption

The total estimated system power consumption of the AS7316-26X is ~315 Watts. This is based upon worst case power assumptions for traffic, optics used and environmental conditions. Typical power consumption will be less.

ROHS

Restriction of Hazardous Substances (6/6)

Compliance with Environmental procedure 020499-00 primarily focused on Restriction of Hazardous Substances (ROHS Directive 2002/95/EC) and Waste and Electrical and Electronic Equipment (WEEE

- Reference Documents
 - 1) ATT-TP-76200

Safety

- UL (CAN/CSA 22.2 No 60950-1 & UL60950-1)
- CB (IEC/EN60950-1)
- CCC (GB4943.1-2011)
- BSMI (CNS14336-1)

Electromagnetic Compatibility

- CE Mark
 - ◆ EN55032 Class A
 - ◆ EN55024 (Immunity) for Information Technology Equipment
 - ◆ EN 61000-3-3
 - ◆ EN 61000-3-2
- FCC Title 47, Part 15, Subpart B Class A
- VCCI Class A
- CNS 13438 (BSMI)
- CCC (GB9254-2008)

Environmental

- Low-Temperature Exposure and Thermal Shock (packaged) : NEBS GR63-CORE ISSUE 4 , Section 4.1.1.1
- High Relative Humidity Exposure (Packaged) : NEBS GR63-CORE ISSUE 4 , Section 4.1.1.2
- High-Temperature Exposure and Thermal Shock (Packaged) : NEBS GR63-CORE ISSUE 4 , Section 4.1.1.3
- Operating Temperature and Relative Humidity : NEBS GR63-CORE ISSUE 4 , Section 4.1.2
- Altitude : NEBS GR63-CORE ISSUE 4 , Section 4.1.3
- Handling Drop Tests -Packaged Equipment : NEBS GR63-CORE ISSUE 4 , Section 4.3.1.1
- Unpackaged Equipment -Drop Tests (All Equipment) : NEBS GR63-CORE ISSUE 4 , Section 4.3.2

- Earthquake (10U Rack) : NEBS GR63-CORE ISSUE 4 , Section 4.4.1 (Zone4)
- Office Vibration Test Procedure; 90 minutes/axis (Stand & 42U Rack) : NEBS GR63-CORE ISSUE 4 , section 4.4.4
- Transportation Vibration-Packaged Equipment : NEBS GR63-CORE ISSUE 4 , section 4.4.5
- Acoustic noise : NEBS GR63-CORE ISSUE 4 , section 4.6
- Bump : IEC60068-2-29- packaged
- Shock : ETSI EN 300 019-2-3 -Operational Tests, Class T3.2 op