Specification for

Dual SMALL FORM FACTOR PLUGGABLE MODULE

DSFP Published Specification Rev. 1.0

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Abstract:

This specification defines the electrical connectors, electrical signals and power supplies, mechanical and thermal requirements of the DSFP Module, connector and cage systems. The DSFP Management interface is an abridged version of CMIS.

This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules.

Points of Contact:

Editor	Ali Ghiasi, Ghiasi Quantum LLC	ali at ghiasiquantum.com
Chair	Chris Cole, Finisar	chris.cole at finisar.com

Revision History:

Revision	Date	Release	Remarks
0.1	Feb. 9, 2018	1st release	
0.2	April 3, 2018	2nd release	Added mechanical section
0.5	May 18, 2018	3rd release	
0.9	July 5, 2018	4th release	
1.0	Sept. 12, 2018	1st public release	

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1 Scope

The DSFP specification defines:

- The DSFP defines Dual Small Form Factor pluggable mechanical form factor;
- Latching mechanism compatible with SFP+;
- Host cage together with the mating connector;
- Electrical interface, including pin-out, data, control, power and ground signals;
- Mechanical interface, including package outline, front panel and printed circuit board (PCB) layout requirements;
- Thermal requirements and limitations, including heat sink design and airflow;
- Electrostatic discharge (ESD) requirements;
- DSFP electrical and mechanical interfaces will support 112G in future;
- The DSFP MIS is an abridged version of CMIS.

2 References

- IEC 61754-7-1:2014: Fibre optic interconnecting devices and passive components - Fibre optic connector interfaces - Part 701: Type MPO connector family – One fibre row.
- IEC 61754-20:2012: Fibre optic interconnecting devices and passive components - Fibre optic connector interfaces - Part 20: Type LC connector family.
- CMIS (Common Management Interface Specifications), see http://www.qsfp-dd.com.
- UM10204, I^2C-bus specification and user manual, Rev 6 – 4 April 2014.
- EN61000-4-2:2008: Electromagnetic compatibility (EMC)- Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test.
- ANSI/ESDA/JEDEC JS-001-2014: Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) - Component Level.
- IEEE 802.3cd: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation.
- IEEE 802.3-2015: IEEE standard for Ethernet Clause 83, 91, 92, 108, 109, and 120 and Annex 83E, 109A, 120C, and 120E.
- SFF-8024: Specification for SFF Cross Reference to Industry Products, Rev 4.1, June 27, 2016.
- SFF-8431 Specification for Enhanced Small Form Factor Pluggable Module SFP+, Rev 4.1, July 2009.
- SFF-8432 Specification for SFP+ Module and Cage, Rev 5.1, August 2012.
- INF-8074i SFP (Small Formfactor Pluggable) Transceiver, Rev 1.0, May 2001.

3 DSFP Application Reference Examples

Below sub-sections illustrate block diagrams for a sampling of optical physical medium dependent sublayers (PMDs) that can be realized in a DSFP form factor. These block diagrams are meant to serve as guidelines for better understanding of the form factor and are by no means exhaustive.

3.1 Optical PMD for dual port: 10/25GBASE-SR/LR, 50GBASE-SR/FR/LR

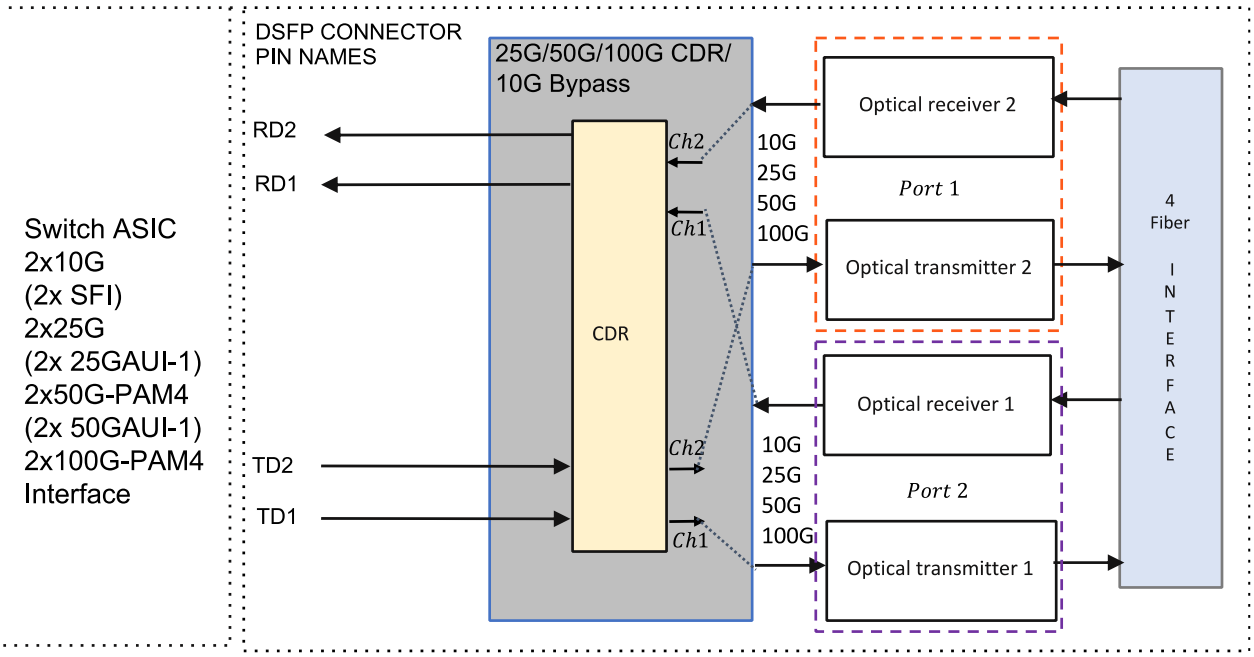

Figure 1: Block diagram for 10/25GBASE-SR/LR or 50GBASE-SR/FR/LR

3.2 Optical PMD for Parallel Fiber: 100GBASE-SR2

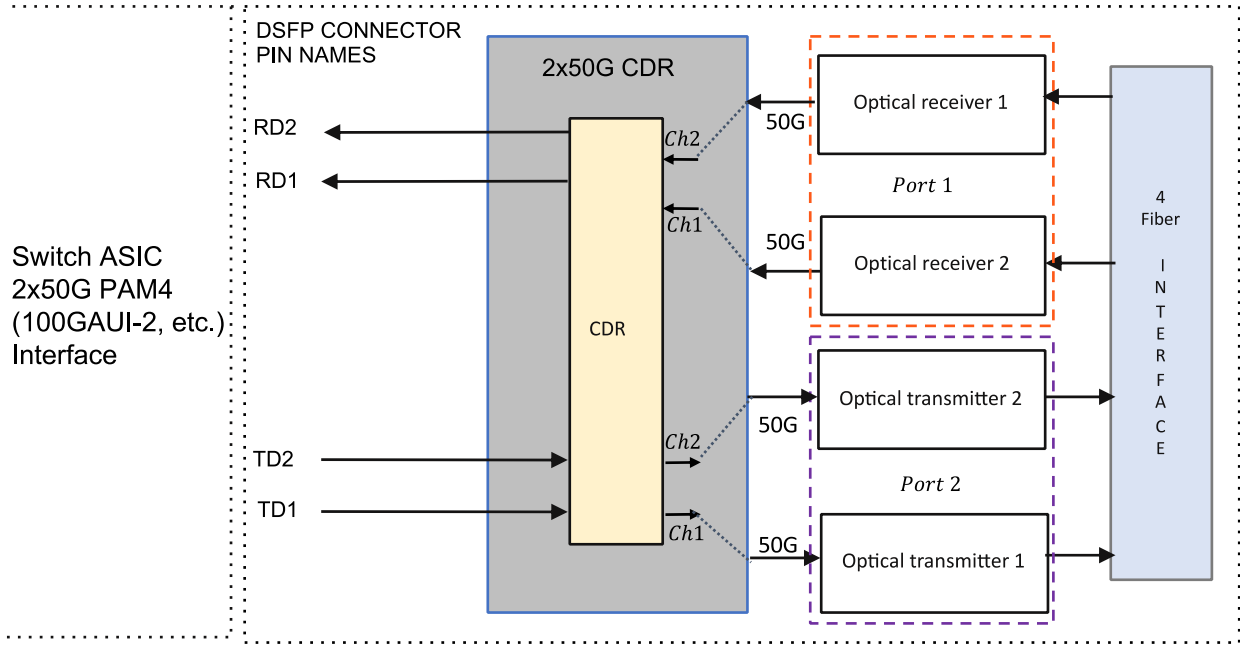

Figure 2: Block diagram for 100GBASE-SR2

3.3 Optical PMD with 2:1 Mux and 50GAUI-2: 50GBASE-SR/FR/LR

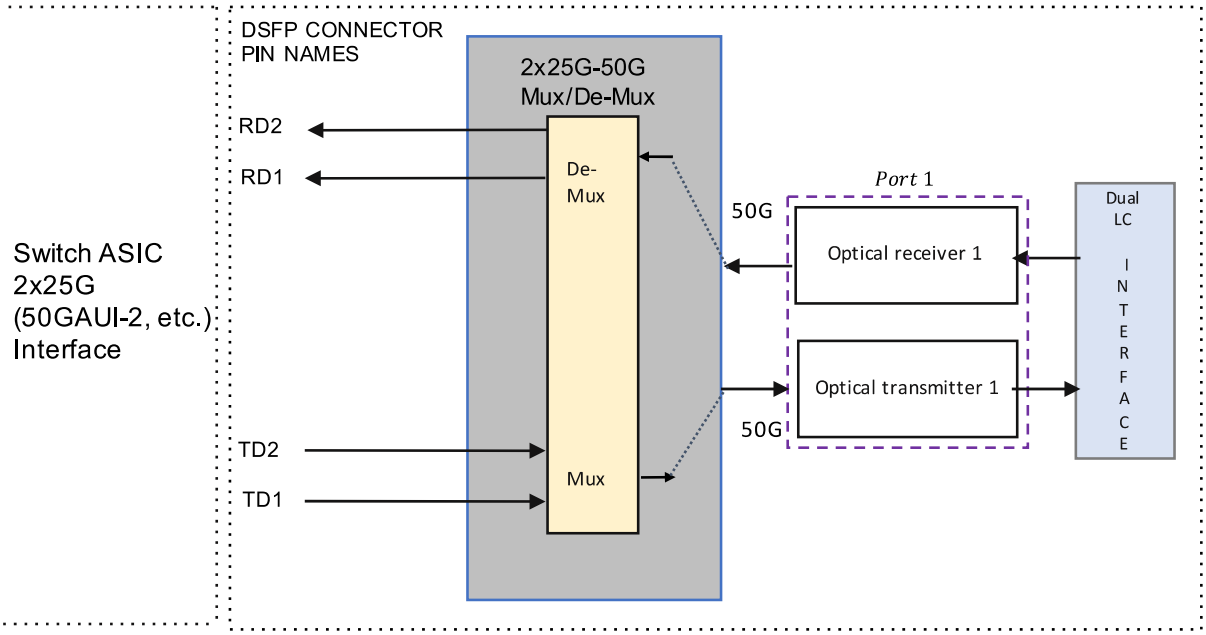

Figure 3: Block diagram for 50GBASE-SR/FR/LR with 2:1 mux

3.4 Optical PMD with 2:1 Mux and 100GAUI-2: 100GBASE-DR

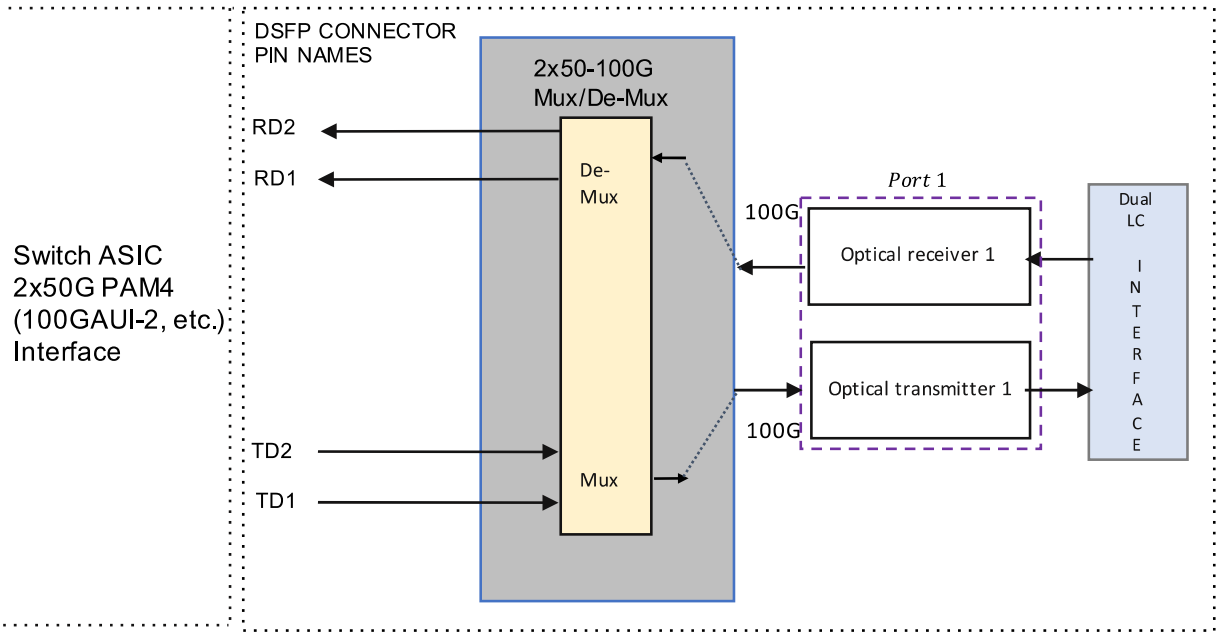

Figure 4: Block diagram for 100GBASE-DR

3.5 Dual port 10G/25G/50G-PAM4 Bi-Di Optical PMD

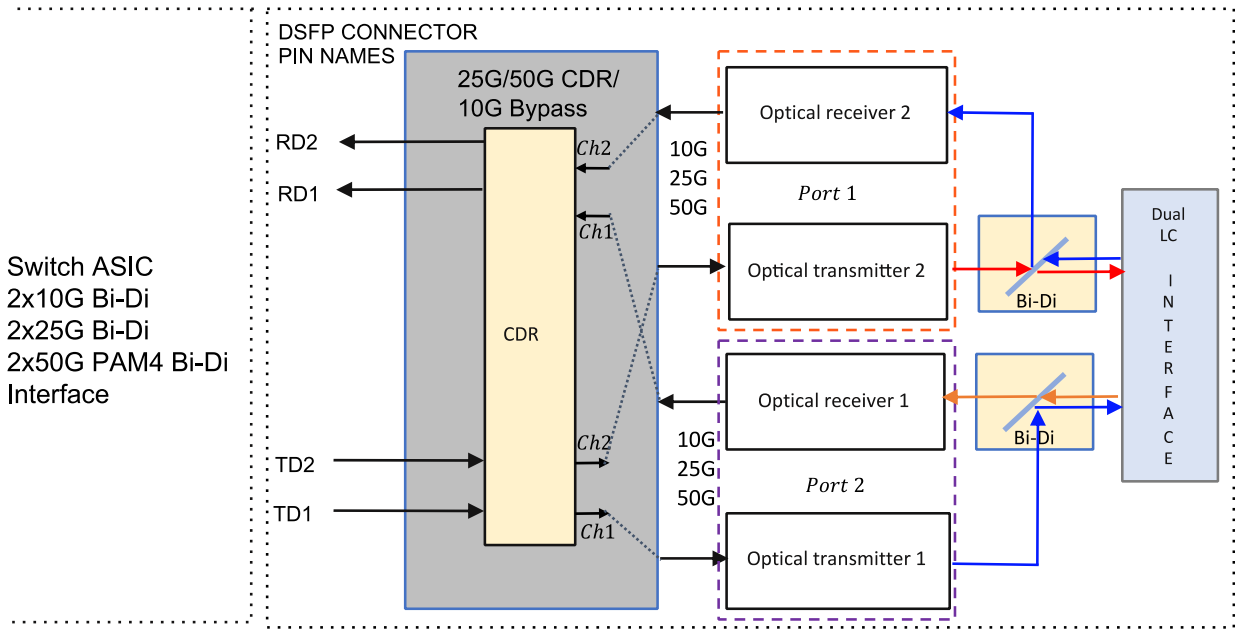

Figure 5: Block diagram for 10G/25G-NRZ and 50G-PAM4 Bi-Di

3.6 DSFP Optical Interface

3.6.1 Duplex LC Optical Interface

Figure 6 shows channel orientation of the optical connector when a duplex LC connector as in IEC 61754-20 is used in a DSFP module. The view is from the front of a typical DSFP module, but actual DSFP module design of the heat sink or height of the optical connector may be different than shown.

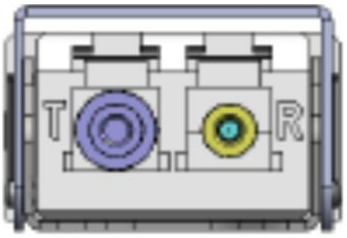

Figure 6. Optical receptacle and channel orientation for duplex LC connector

4 Electrical Interface

4.1 Module Electrical Connector

The DSFP connector is a 0.8 mm pitch 22 contacts improved connector compatible to SFP+ 20 contacts connector. Host PCB contact assignment is shown in Figure 7 and contact definitions are given in Table 4-1. DSFP module contacts mate with the host in the order of ground, power, followed by signal as illustrated by Figure 8 and the contact sequence order listed in Table 4-1.

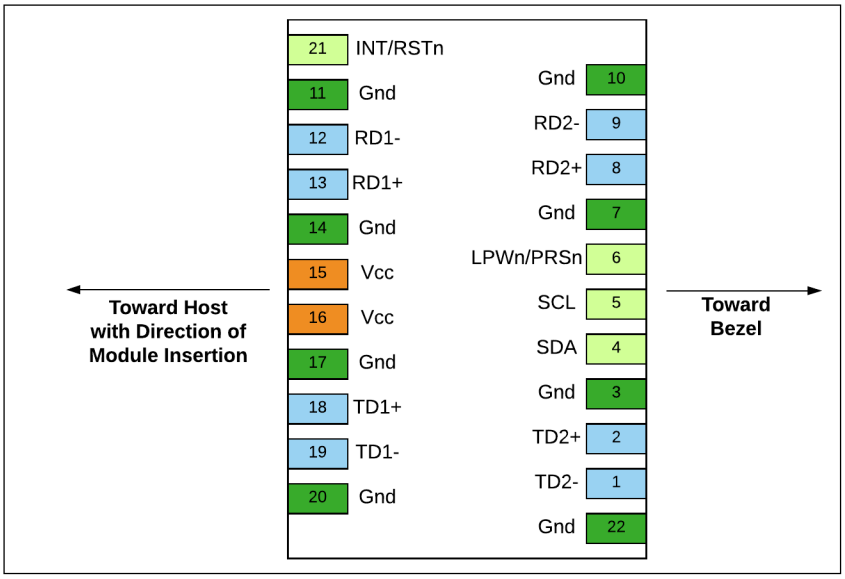

Figure 7: DSFP Host PCB pad assignment top view

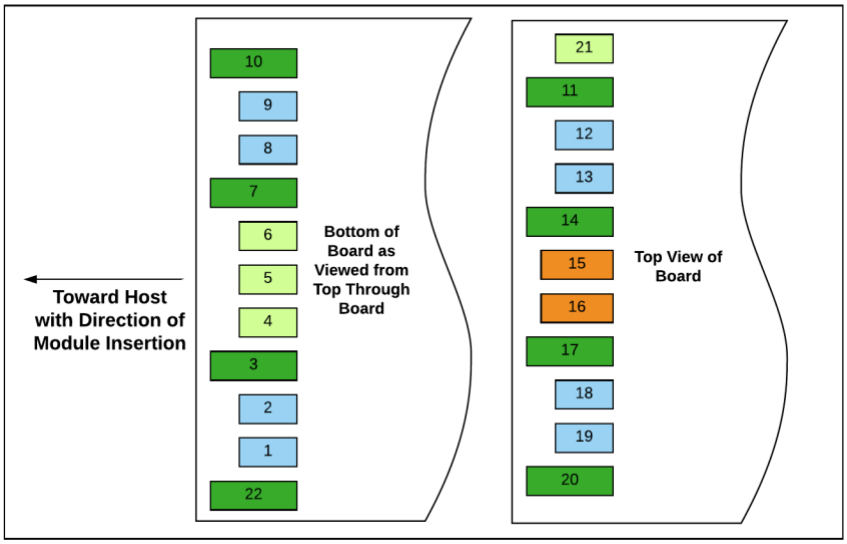

Figure 8: DSFP module contact assignment

Table 4-1: DSFP Module and Host Electrical contact definition

Contacts	Logic[1]	Symbol	Power Sequence Order	Name/Description	Note
case		case	See 2	Module case	
1	CML-I	TD2-	3rd	Transmitter Inverted Data Input Lane 2	
2	CML-I	TD2+	3rd	Transmitter Non-Inverted Data Input Lane 2	
3		Gnd	1st	Module Ground	5
4	LVTTL-I/O	SDA	3rd	2-wire Serial Interface Data Line	3
5	LVTTL-I/O	SCL	3rd	2-wire Serial Interface Clock	3
6	Multi-level-I/O	LPWn/PRSn	3rd	$\overline{\text{Low Power}}$ Mode/ $\overline{\text{Module Present}}$ (Mod_Abs)	
7		Gnd	1st	Module Ground	5
8	CML-O	RD2+	3rd	Receiver Non-Inverted Data Output Lane 2	
9	CML-O	RD2-	3rd	Receiver Inverted Data Output Lane 2	
10		Gnd	1st	Module Ground	5
11		Gnd	1st	Module Ground	5
12	CML-O	RD1-	3rd	Receiver Inverted Data Output Lane 1	4
13	CML-O	RD1+	3rd	Receiver Non-Inverted Data Output Lane 1	4
14		Gnd	1st	Module Ground	5
15		Vcc	2nd	Module 3.3 V Supply	
16		Vcc	2nd	Module 3.3 V Supply	
17		Gnd	1st	Module Ground	5
18	CML-I	TD1+	3rd	Transmitter Non-Inverted Data Input Lane 1	4
19	CML-I	TD1-	3rd	Transmitter Inverted Data Input Lane 1	4
20		Gnd	1st	Module Ground	5
21	Multi-level-I/O	INT/RSTn	3rd	Dual Function Module Interrupt and $\overline{\text{Reset}}$ Pin	
22		Gnd	1st	Module Ground	5

1. Labeling as inputs (I) and outputs (O) are from the perspective of the module.
2. The case makes electrical contact to the cage before any of the board edge contacts are made.
3. See 4.4 the 2-wire specifications.
4. Backward compatible with SFF-8431 SFI interface.
5. The module ground contacts Gnd recommended to be isolated from the module case by offering flexibility in the host EMI control strategy.

4.2 High-Speed Signals

The high-speed signals include two transmit and two receive differential pairs identified as TD[2:1]p / TD[2:1]n and RD[2:1]p / RD[2:1]n. For signaling at 10 Gb/s NRZ, the high-speed signals are compatible with the SFI signals defined in SFF-8431. The DSFP has single or dual ports on the media side of the module and supports up to 50 Gb/s per lane on the host side of the module. The module may include a multiplexing / demultiplexing function to map two electrical lanes to or from a single optical or electrical lane.

The DSFP module is a multi-standard module with each of the electrical lanes supporting data rates from 9.95-53.1 Gb/s. The DSFP module supporting following standards; SFI electrical specifications as defined by SFF-8431 for 10.3125 GBd NRZ; 25.78125 GBd NRZ signaling as defined by IEEE 802.3-2015 (clause 83E, 91, 92, 108, 109 and Annex 83E); 26.5625 GBd PAM4 signaling as defined by IEEE802.3-2015 (clause 120, and Annex 120C and 120E), IEEE802.3cd and OIF-CEI-04.0 (CEI-56G-VSR-PAM). The DSFP module supports single port (SFP+ mode) or dual ports (2xSFP+) modes or a single port implementation having 2-lanes AUI with a Mux, summary of DSFP implementations with example PMDs are listed in Table 4-2.

Table 4-2: DSFP Implementations and Modes

Interface	Lanes Active	Configuration	AUI Baudrate	AUI Modulation	Example PMDs
SFI	1, or 1 and 2	Single or dual ports	9.95-11.1 GBd	NRZ	10GBASE-SR, 10GBASE-LR 10GSFP+ DAC OTU-2
10G CPRI	1, or 1 and 2	Single or dual ports	10.1376 GBd	NRZ	10G-SR/LR CPRI
25GAUI	1, or 1 and 2	Single or dual ports	25.78 GBd	NRZ	25GBASE-CR 25GBASE-SR, 25GBASE-LR
25G CPRI	1, or 1 and 2	Single or dual ports	24.33024 GBd	NRZ	25G-SR/LR CPRI
50GAUI-2	1 and 2	Single port with Mux	25.78 GBd	NRZ	50GBASE-SR, *50GBASE-LR*
50GAUI	1, or 1 and 2	Single or dual ports	26.55 GBd	PAM4	50GBASE-CR 50GBASE-SR, *50GBASE-LR*
100GAUI-2	1 and 2	Single port	26.55 GBd	PAM4	100GBASE-CR2 100GBASE-SR2
100GAUI-2	1 and 2	Single port with Mux	26.55 GBd	PAM4	100GBASE-DR

The lane assignments in Table 4-3 shall be used for the different PMD configurations.

Table 4-3: High-speed signal lane mapping

PMD Configuration	Transmit and Receive Electrical Lanes	
	1	***2***
1x100G (PAM4)	Port 1	
2x50G (PAM4), 2x25G(NRZ), 2x10G(NRZ)	Port 1 (SFF-8431)	Port 2

4.3 Low-Speed Signals

The DSFP module has 4 low-speed signals consisting of SCL, SDA, LPWn/PRSn, and INT/RSTn. These signals are used for configuration and control of the module by the host. SCL and SDA are bidirectional signals with logic levels based on 3.3V LVCMOS. LPWn/PRSn and INT/RSTn have additional circuitry on the host and DSFP modules to enable multi-level bidirectional signaling. DSFP modules operating with power class I and II may omit LPWn circuitry in the module by tying PRSn contact to Gnd (Cautions: by removing the LPWn circuitry in the module it will eliminate TX_Disable function which exist in SFP+/SFP28).

4.3.1 SCL and SDA

SCL and SDA are a 2-wire I^2C compliant serial interface between the host and module using the 2-wire protocol. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value can be 2.2k ohms to 4.7k ohms. For 2-wire interface protocol and electrical specifications, see 4.4.

4.3.2 LPWn/PRSn

LPWn/ PRSn is a dual function bi-directional signal that allows the host to signal $\overline{Low\ Power}$ mode to enable DSFP power class III-IV and the module to indicate to the host the Module Present signal. DSFP host accepts legacy SFP+ module with PRSn[1] pulled to Gnd in the module. LPWn is a required function to enable DSFP high power class II-IV DSFP modules.

The circuit shown in Figure 9 enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

[1] PRSn pin is identical to Mod_Abs pins as defined by SFF-8431, where SFP+/SFP28/SFP56 Mod_ABS contact is connected to VeeT or VeeR in the module.

The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 9 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_PRSn signal and the module uses a voltage reference at 1.25V to determine the state of the M_LPWn signal.

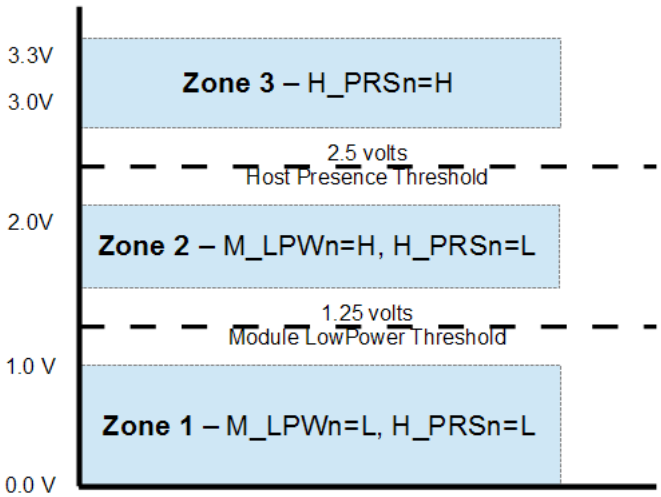

Figure 9: LPWn/PRSn voltage zones

- Zone 1 – Low Power mode – Zone 1 is the low power state and module is present (M_LPWn=Low, H_PRSn=Low). The min/max voltages for Zone 1 are defined by parameters V_LPWn/PRSn_1 in Table 4-4.
- Zone 2 – High Power mode – Zone 2 is the high-power state and module is present (M_LPWn=High, H_PRSn=Low). The min/max voltages for Zone 2 are defined by parameters V_LPWn/PRSn_2 in Table 4-4.
- Zone 3 – Module Not Present – Zone 3 is the state for when the module is not present (H_PRSn=High). The min/max voltages for Zone 3 are defined by parameters V_LPWn/PRSn_3 in Table 4-4.

Module Removal – If the module is being unplugged and LPWn/PRSn loses contact, the pull-down resistor on the module will assert Low Power mode on the module (M_LPWn=Low). The module is required to transition to low power (Power Class 1) and disable transmitters within the time specified by T_hplp in Table 4-4. This maximum transition time is to ensure the module is in Low Power mode before the power contacts lose connection to avoid potential damage from arcing.

The LPWn/PRSn signal is driven High or Open by the host for Low Power mode control. If logic is used to generate the High level, then 3.3V LVCMOS is preferred.

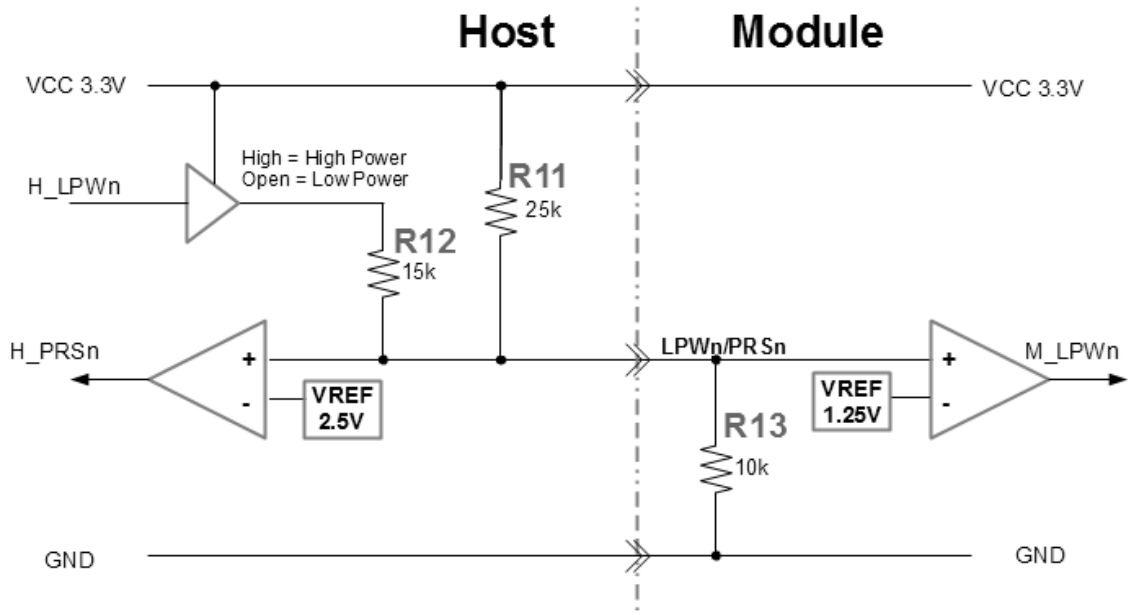

Figure 10: LPWn/PRSn circuit

Table 4-4: LPWn/PRSn circuit parameters

Parameter	Nominal	Min	Max	Units	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_PRSn	2.500	2.475	2.525	Volts	Precision voltage reference for H_PRSn
M_Vref_LPWn	1.250	1.238	1.263	Volts	Precision voltage reference for M_LPWn
R11	25k	24.5k	25.5k	Ohms	Recommend 24.9k ohms 1% resistor
R12	15k	14.7k	15.3k	Ohms	Recommend 15k ohms 1% resistor
R13	10k	9.8k	10.2k	Ohms	Recommend 10k ohms 1% resistor
V_LPWn/PRSn _1	0.950	0.000	1.100	Volts	LPWn/PRSn voltage for Module installed, H_LPWn=Low
V_LPWn/PRSn _2	1.700	1.400	2.250	Volts	LPWn/PRSn voltage for Module installed, H_LPWn=High
V_LPWn/PRSn_3	3.300	2.750	3.465	Volts	LPWn/PRSn voltage for No Module
T_hplp			200	µs	High power mode to Low power mode transition time from assertion of LPWn or RSTn.

4.3.3 INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown in Figure 11 enables multi-level signaling to provide direct signal control in both directions. Reset is an active-low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-low signal on the host.

The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 11 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_INTn signal and the module uses a voltage reference at 1.25V to determine the state of the M_RSTn signal.

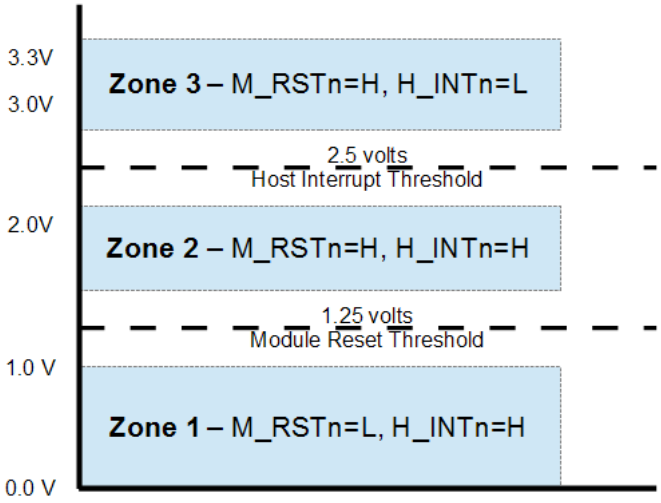

Figure 11: INT/RSTn voltage zones

- Zone 1 – Reset operation – Zone 1 is the state when the module is in reset and interrupt de-asserted (M_RSTn=Low, H_INTn=High). The min/max voltages for Zone 1 are defined by parameters V_INT/RSTn_1 and V_INT/RSTn_2 in Table 4-5.
- Zone 2 – Normal operation – Zone 2 is the normal operating state with reset de-asserted (M_RSTn=High) and interrupt de-asserted (H_INTn=High). The min/max voltages for Zone 2 are defined by parameter V_INT/RSTn_3 in Table 4-5.
- Zone 3 – Interrupt operation – Zone 3 is the state for the module to assert interrupt and the module must also be out of reset (M_RSTn=High, H_INTn=Low). The min/max voltages for Zone 3 are defined by parameter V_INT/RSTn_4 in Table 4-5.

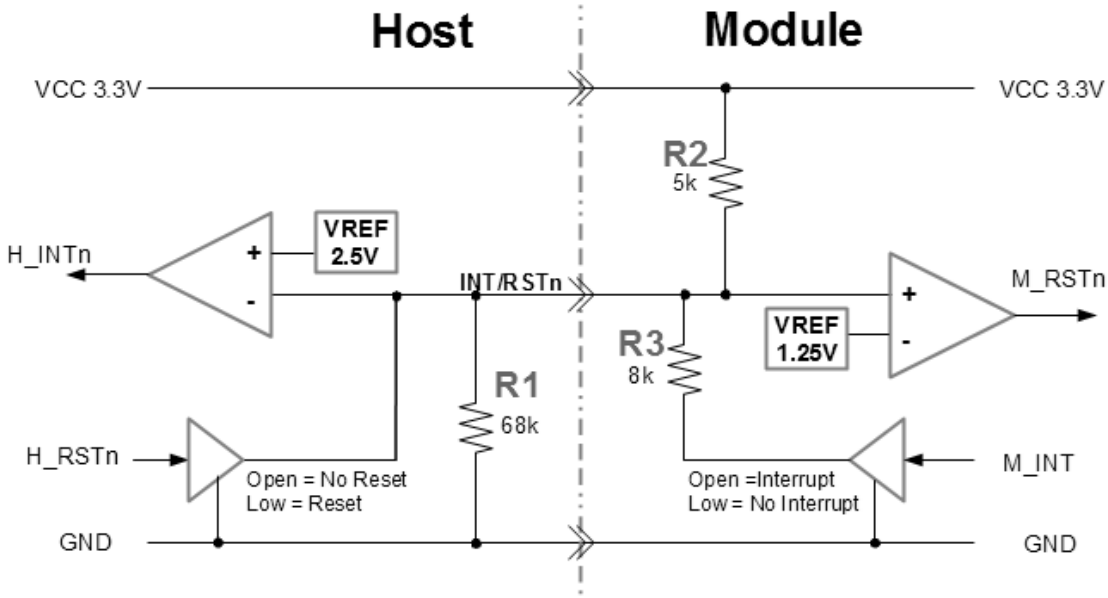

Figure 12: INT/RSTn circuit

Table 4-5: INT/RSTn circuit parameters

Parameter	Nominal	Min	Max	Units	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_INTn	2.500	2.475	2.525	Volts	Precision voltage reference for H_INTn
M_Vref_RSTn	1.250	1.238	1.263	Volts	Precision voltage reference for M_RSTn
R1	68k	66k	70k	Ohms	Recommend 68.1k ohms 1% resistor
R2	5k	4.9k	5.1k	Ohms	Recommend 4.99k ohms 1% resistor
R3	8k	7.8k	8.2k	Ohms	Recommend 8.06k ohms 1% resistor
V_INT/RSTn_1	0.000	0.000	1.000	Volts	INT/RSTn voltage for No Module
V_INT/RSTn_2	0.000	0.000	1.000	Volts	INT/RSTn voltage for Module installed, H_RSTn=Low
V_INT/RSTn_3	1.900	1.500	2.250	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=Low
V_INT/RSTn_4	3.000	2.750	3.465	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=High

4.4 The 2-wire Interface Protocol and Electrical Specifications

DSFP 2-wire interface is based on Low Voltage TTL (LVTTL) operating with a module supply of 3.3 V +/-5% and with a host supply range of 2.38 to 3.46 V.

The 2-wire interface protocol and electrical specifications are defined in SFF-8431 and compatible with I^2C bus specifications.

4.5 Timing Requirement of Control and Status IO Low-Speed Electrical Specifications

The timing requirements of control and status I/O are defined in.

Table 4-6: Timing Parameters for DSFP Management

Parameter	Symbol	Min	Max	Units	Conditions
Time to initialize 2-wire interface	t_2w_start_up		300	ms	From power on or hot plug after the supply voltage meet requirements in Table 4-9
Time to initialize	t_start_up		300	ms	From the time power supplies meeting conditions in Table 4-9 or hot plug, until non-cooled power level I part (or non-cooled power level II part already enabled at power level II) is fully operational.
Time to initialize cooled module and time to power up a cooled module to Power Level II-IV	t_start_up_cooled		90	s	From power supplies meeting conditions in Table 4-9 or hot plug, until cooled power level I part (or cooled power level II part during fault recovery) is fully operational. Also, from stop bit low-to-high SDA transition enabling Power Level II until cooled module is fully operational
Time to Power Up to Level II-IV	t_power_level2		300	ms	From stop bit low-to-high SDA transition enabling power level II until non-cooled module is fully operational
Time to Power Down from Level II-IV	t_power_down		300	ms	From stop bit low-to-high SDA transition disabling power level II until module is within power level I requirements

4.6 DSFP Power Requirements

The module host has two 3.3 V power contacts Vcc that are tight together. The maximum current capacity, both continuous and peak, for each connector contact is 1000 mA.

DSFP module maximum power consumption shall meet one of the following power classes:

- Power Level I modules – Up to 1.0 W
- Power Level II modules – Up to 1.5 W
- Power Level III Modules – Up to 2.5 W
- Power Level IV Modules – Up to 3.5 W

When the module powers up, on insertion, or bring up of Vcc, or de-assertion of RSTn, if the LPWn is asserted (held LOW) the module transitions to low power mode allowing the host to configure the module over I2C. When the module powers up, on insertion, or bring up of Vcc, or de-assertion of RSTn, if the LPWn is de-asserted (held HIGH) the module transitions to normal operating mode. This allows the module to power up to normal operating mode without host intervention. In addition, the module can be configured into Low Power or High Power modes by setting *ForceLowPWR* Bit (CMIS Byte=26, bit=4) to states listed in Table 4-7 during module set-up by the vendor. However, other applications may have different default values. For example, if the customer wants high power modules that just power up to the normal operating state without host intervention, then the *ForceLowPwr* bit is configured to 0 during module set-up by the vendor.

Table 4-7: Module power up default mode

Module Power Type	***ForceLowPwr* Bit (power up default)**
Low Power Module (Power ≤ 1.5 W)	0
High Power Module (Power > 1.5 W)	1

If the module powers up to Low Power state because the *ForceLowPwr* bit power on default is 1, to get the module into an operating state, the host simply writes a 0 into the *ForceLowPwr* bit location, see Table 4-8 for logical interaction of module LPWn HW pin with *ForceLowPwr* Bit.

Table 4-8: Module LPWn HW pin interaction with ForceLow Pwr bit

Module State	***ForceLowPwr* Bit = 0**	***ForceLowPwr* Bit = 1**
LPWn HW IO pin=0 (asserted)	Low Power (TX Off)	Low Power (TX Off)
LPWn HW IO pin=1 (de-asserted)	Operating (TX on)	Low Power (TX Off)

The maximum power level is allowed to exceed the classified power level for 500 ms following hot insertion or power up, or Power Level II-IV authorization, however the current is limited to values given by Table 4-9 and illustrated in Figure *13*.

4.6.1 Module Power Supply Requirements

DSFP module operates from two host supplied Vcc contacts. To protect the host and system operation, each DSFP module during hot plug and normal operation shall follow the requirements listed in Table 4-9 and illustrated by in Figure *13*. The requirements for current apply to the current through each inductor of SFF-8431 Figure 56 while the power supply voltages are defined at the DSFP connector.

4.6.2 Host Power Supply Noise Output

The host shall generate an effective weighted integrated spectrum RMS noise less than 25 mV in the frequency range 10 Hz to 10 MHz, according to the methods of SFF-8431 D.17.1.

4.6.3 Module Power Supply Noise Output

The module shall generate less than 15 mV RMS noise at point X of SFF-8431 Figure 56 in the frequency range 10Hz to 10MHz, according to the methods of SFF-8431 D.17.2.

4.6.4 Power Supply Noise Tolerance

SFP+ modules shall meet all electrical requirements and remain fully operational in the presence of a sinusoidal tolerance signal of amplitude given by Table 4-9 swept from 10 Hz to 10 MHz according to the methods of SFF-8431 D.17.3. This emulates the worst-case noise of the host.

It is also desirable for a module and host to each tolerate a degree of random or semi-random noise on Vcc simultaneously, but the characteristics of this noise are beyond the scope of this document.

Table 4-9: DSFP Module Power Supply Requirements

Parameter	Symbol	Conditions	Min	Max	Unit
DSFP Module Power Level I					
Power supply noise tolerance including ripple [peak-to-peak]		See SFF-8431 D.17.3		66	mV
Power supply voltages including ripple, droop and noise below 100 kHz	Vcc	Note 1	3.14	3.46	V
Instantaneous peak current at hot plug		Note 2, 3, 4		400	mA
Sustained peak current at hot plug		Note 2, 3, 5		330	mA
Module maximum power consumption		See SFF-8431 D.17.3		1.0	W
DSFP Module Power Level II-IV					
Power supply noise tolerance including ripple [peak-to-peak]		See SFF-8431 D.17.3		66	mV
Power supply voltages including ripple, droop and noise below 100 kHz	Vcc	Note 1	3.14	3.46	V
Instantaneous peak current at hot plug		Note 2, 3, 4		400	mA
Sustained peak current at hot plug		Note 2, 3, 5		330	mA
Module maximum power consumption at power up		Note 4		1.0	W
Instantaneous peak current on enabling Power Level II Instantaneous peak current on enabling Power Level III Instantaneous peak current on enabling Power Level IV		Note 2, 3, 5		600 1000 1400	mA
Module sustained peak current on enabling Power Level II Module sustained peak current on enabling Power Level III Module sustained peak current on enabling Power Level IV		Note 2, 3, 5		500 830 1160	mA
Module maximum power consumption Power Level II Module maximum power consumption Power Level III Module maximum power consumption Power Level IV				1.5 2.5 3.5	W

1. Set point is measured at the input to the connector on the host board reference to Gnd. Droop is any temporary drop in voltage of the power supply such as that caused by plugging in another module or when enabling another module to Power Level II-IV.

2. The requirements for current apply to the current through each inductor of SFF-8431 Figure 56.

3. The maximum currents for each Vcc power supply contact, therefore the total module peak currents can be twice this value. The instantaneous peak current is allowed to exceed the specified maximum current capacity of the connector contact for a short period, see Figure *13*.

4. Maximum module power consumption shall not exceed 1.0 W from 500 ms after power-up and until level II-IV operation are enabled.

5. Not to exceed the sustained peak limit for more than 50 µs; may exceed this limit for shorter durations.

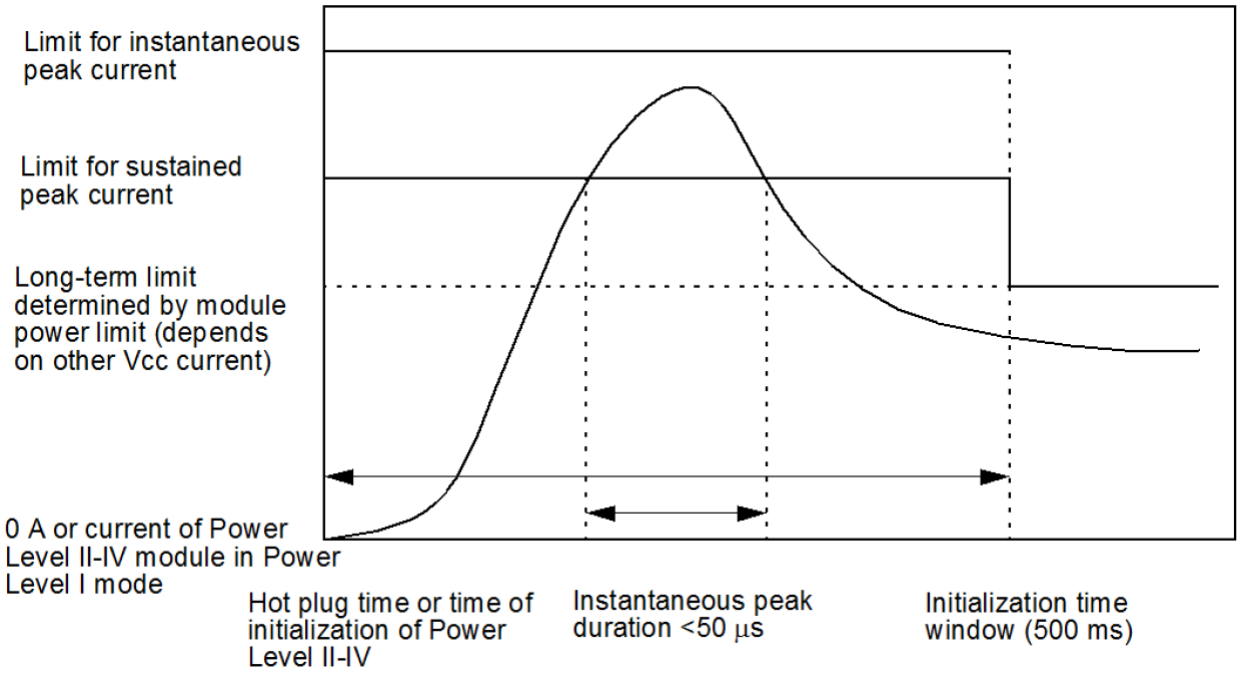

Figure 13*: Instantaneous and sustained peak current for Vcc*

4.7 ESD

The DSFP module and host high speed contacts shall withstand 1000 V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.

The DSFP module and all host contacts with exception of the high-speed contacts shall withstand 2 kV electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.

The DSFP module shall meet ESD requirements given in EN61000-4-2, criterion B test specification such that units are subjected to 15 kV air discharges during operation and 8 kV direct contact discharges to the case.

4.8 DSFP Host Application Reference

An example DSFP host application reference circuit where a DSFP module is plugged into the host shown in Figure 14. The logical host controls signals[2] are designated as H_RSTn, H_INT, H_LPWn, and H_PRSn and the logical module control signal are designated as M_RSTn, M_INT, M_LPWn. Example implementation also provide suggested host board power supply filters for a 3.3V supply. If an alternate circuit is used for power supply filtering, then the same filter characteristics as this example filter is required. The 2-wire SCL/SDA pull resistors of 3.3 kΩ shown on the reference diagram is designed to support 400 kHz bus speed with 100 pf load capacitance, for other bus configurations see SFF-8431 Chapter 4.

AC Caps on TD2+/- and RD2+/- lines of a DSFP module potentially could be removed if the DSFP module can be plugged into legacy SFP+ host without the module getting damaged.

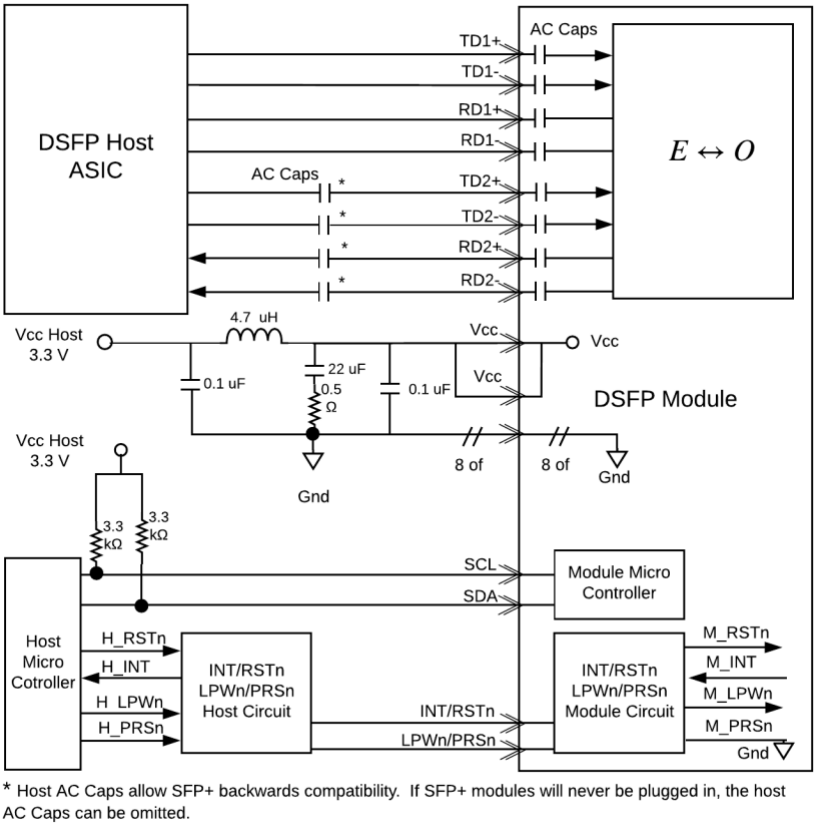

Figure 14: DSFP Host Application Reference with DSFP Module

An example DSFP host application reference circuit where an SFP+ module is plugged into the host shown in Figure 15. The DSFP host must provide appropriate protection to prevent damage to the transmitter outputs TD2+/- connected respectively to the module TX_Fault and Gnd. It is recommended that DSFP host only turns on the TD2+/TD2- after the module has been identified as a DSFP. SFP+ module RX_LOS and RS1 contacts respectively are

[2] The host H_ and module M_ designations are informative.

connected to the DSFP host RD2+/RD2- inputs. AC coupling RD2+/RD2- inputs are required to prevent damage to the high speed SerDes inputs from LVTTL levels of RX_LOS and RS1. The value of AC coupling capacitor depends on the application with capacitor size large enough to limit the impact of the baseline wander. The location of AC coupling capacitors on TD2+/- and RD2+/- signal lines could be at any of the following locations; mounted on the host PCB, integrated into the host ASIC package, or integrated into the host ASIC die.

The 2-wire SCL/SDA pull resistors of 3.3 kΩ shown on the reference diagram is designed to support a 400 kHz bus speed with 100 pf load capacitance, for other bus configuration see SFF-8431 Chapter 4.

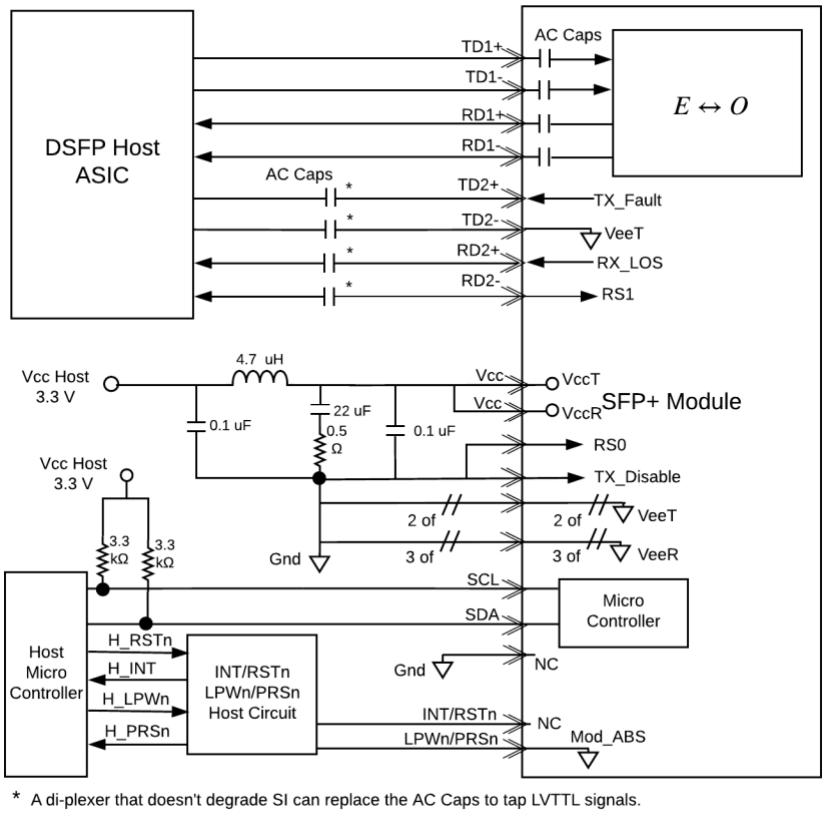

Figure 15: DSFP Host Application Reference with SFP+ Module

5 DSFP Module and Cage Mechanical Specifications

5.1 Overview

An example DSFP module plugged into a press fit cage is shown Figure 16. An SMT 1x1 DSFP cage is shown in Figure 17.

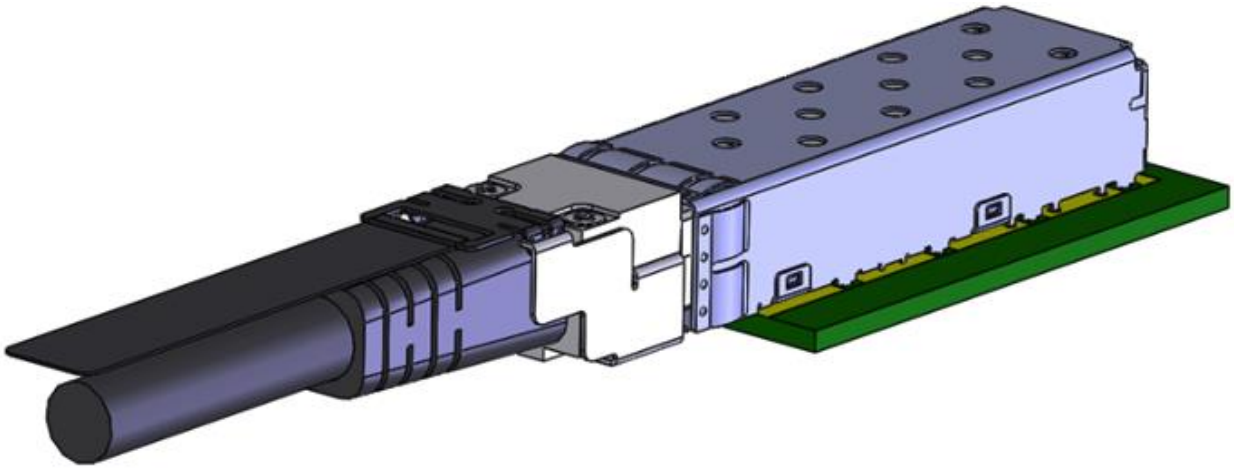

Figure 16: DSFP Module and Cage

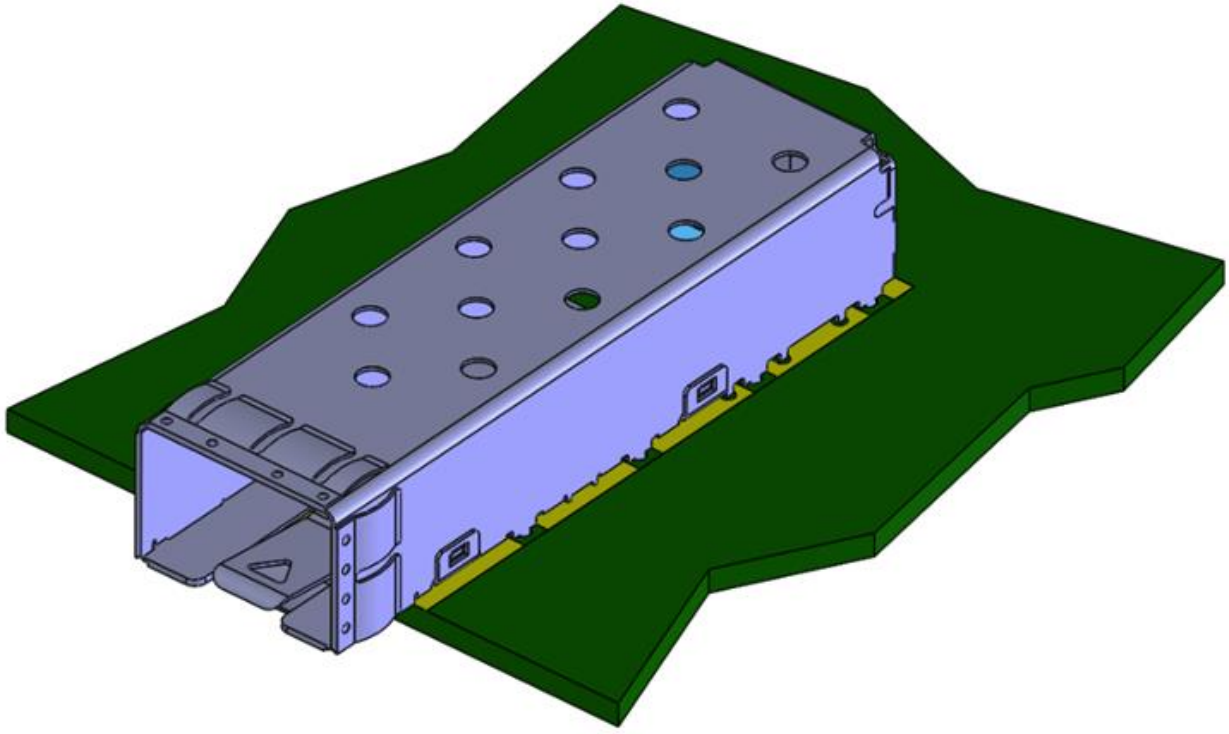

Figure 17: DSFP Press fit Cage

5.2 Datum, Dimension and Component Alignment

In the module mechanical drawings included throughout this specification, the datum as defined in Table 5-1 shall apply. Dimensions and tolerances conform to ASME Y14.5-2009. All dimensions are in millimeters unless otherwise noted.

Table 5-1: Datum descriptions

Designator	Description	Figure
A	Width of paddle card	Figure 20
B	Paddle card surface	Figure 20
C	End of signal contacts	Figure 20
E	Paddle card slot width	Figure 21
F	Bottom of connector body	Figure 21
G	Primary peg location	Figure 21
H	Connector positioning pin hole	Figure 22
J	Connector positioning pin hole	Figure 22
K	Cage press fit pin hole	Figure 23
L	Cage press fit pin hole	Figure 23
M	Front of cage	Figure 18
N	Seating surface of cage	Figure 18
P	Inside width of cage	Figure 18
X	Front of foot print	Figure 23
Y	Side of foot print	Figure 23

5.3 DSFP Cage Mechanical Specification

The mechanical outline of a press-fit style 1x1 cage is shown in Figure 18. Details of latch and riding heat sink are shown in Figure 19.

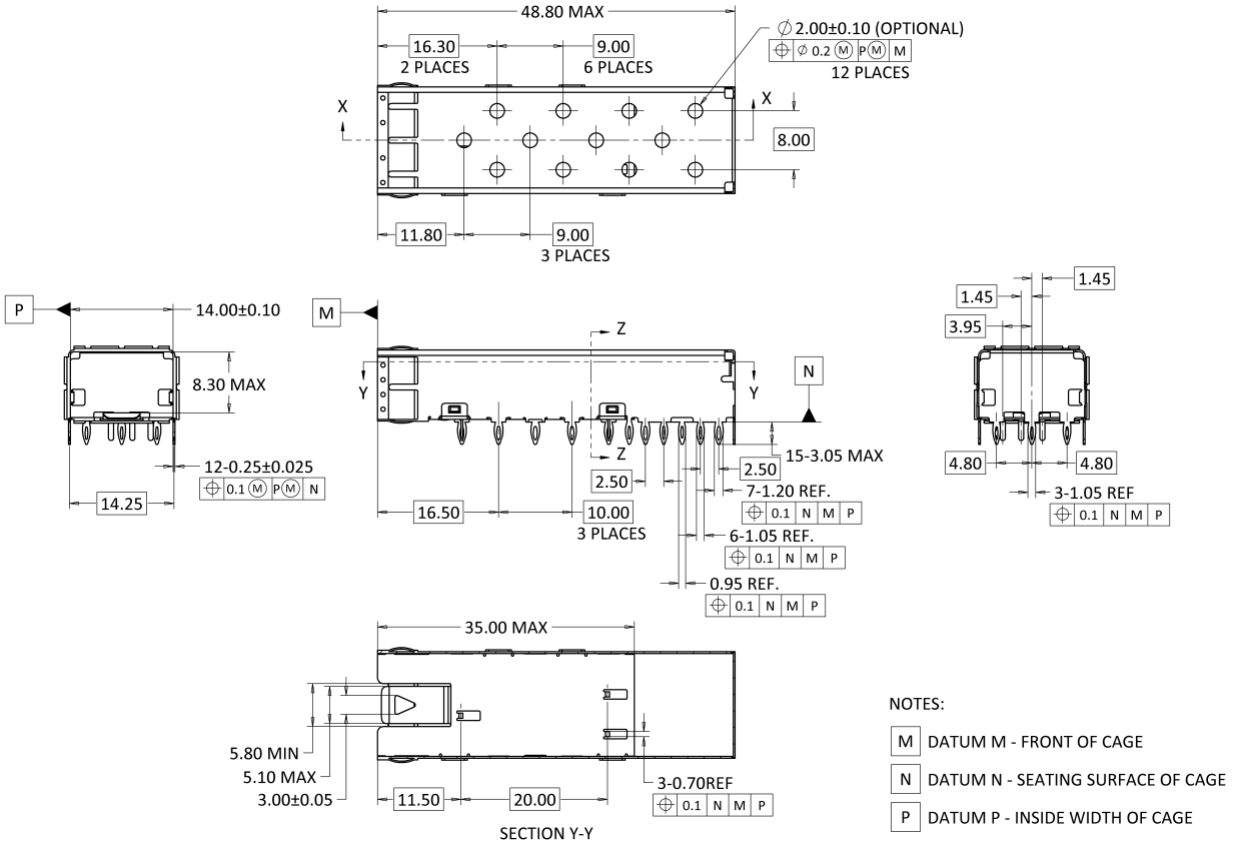

Figure 18: DSFP Press-Fit Style 1x1 Cage

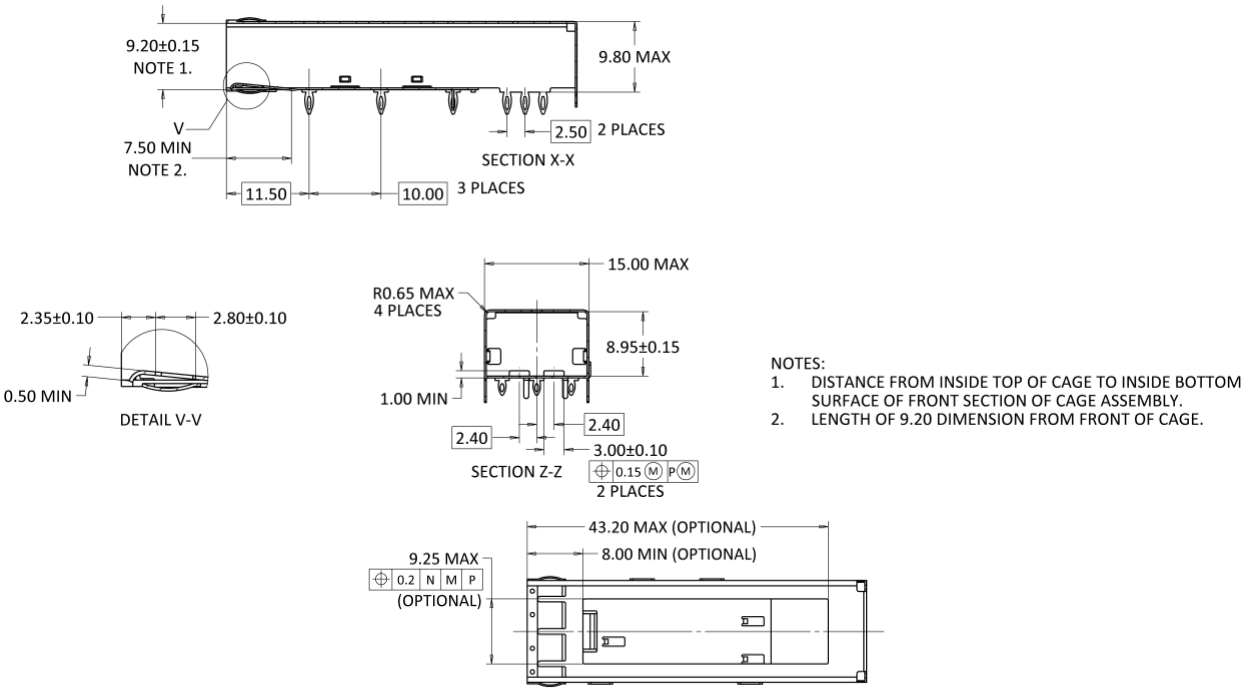

Figure 19: DSFP Cage Latch and Riding Heatsink Details

5.4 Module Mechanical and Edge Card Dimensions

The mechanical outline of the DSFP module compatible with SFP+/SFP28/SFP56 SFF-8432 and shall support both SMT cages as well as stacked cages as shown in Figure 20. DSFP module latch mechanism is compatible with legacy INF-8074i.

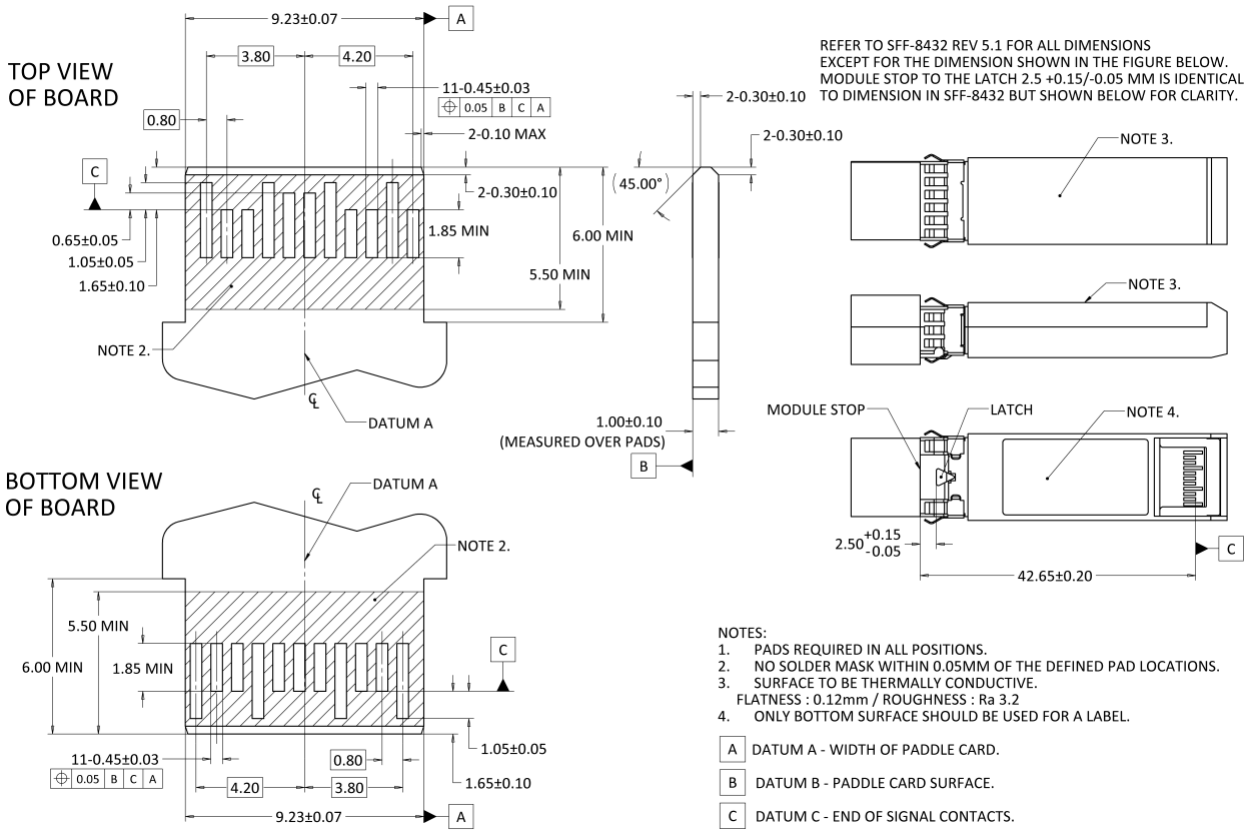

Figure 20: DSFP Module Card Edge and Mechanical

5.5 DSFP SMT Connector

The DSFP connector is a 22-contact right angle connector shown in Figure 21. The DSFP connector can accept and is compatible with INF-8074i modules based on 20-contacts edge card.

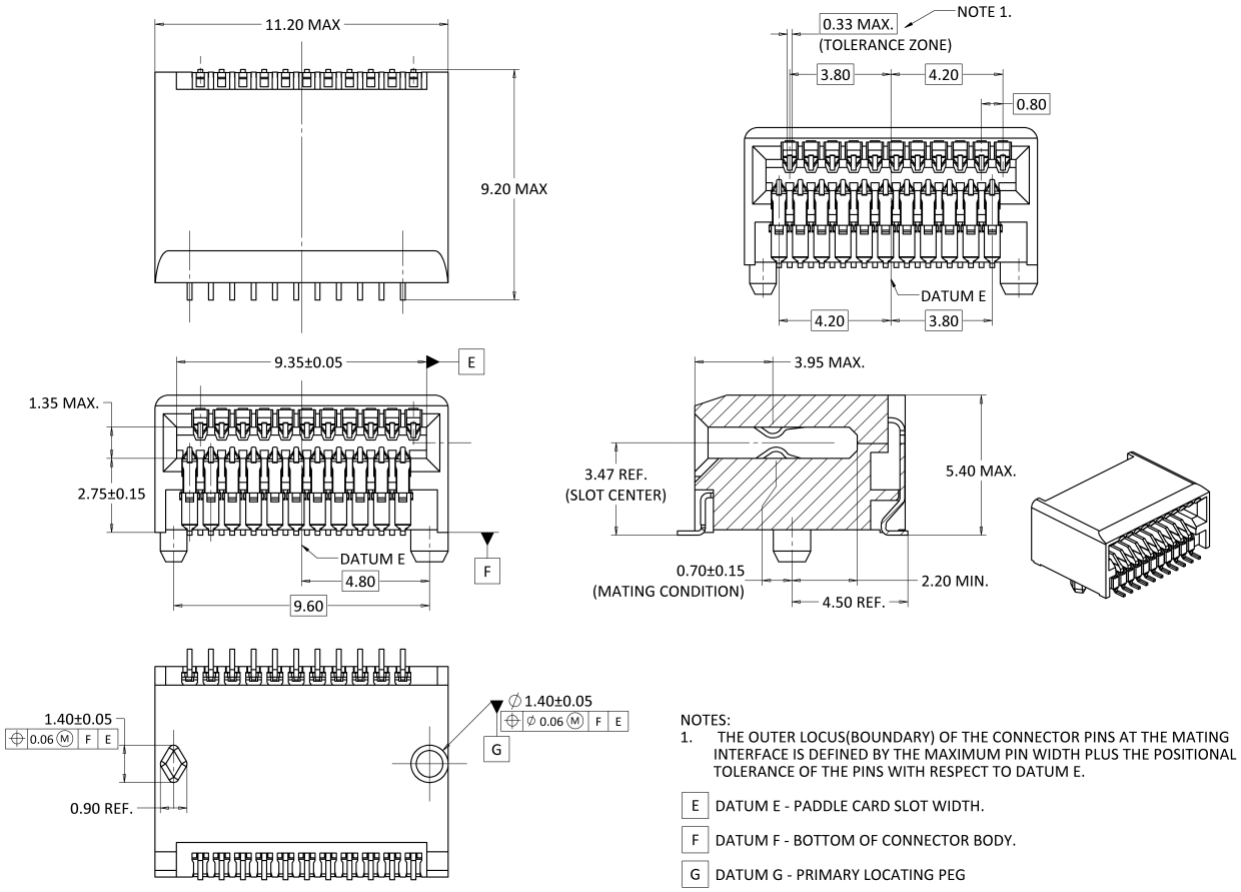

Figure 21: DSFP SMT Connector

5.6 DSFP SMT Connector and Cage Host PCB Layout

Recommended host PCB board layout for attaching DSFP SMT connector and 1x1 cage are shown respectively in Figure 22 and Figure 23. To achieve 25-56 GBd operations pad dimensions and tolerance for signal contacts should be adhered. The recommended host PCB differential traces and contacts impedance is 90-100 Ω to minimize any discontinuities.

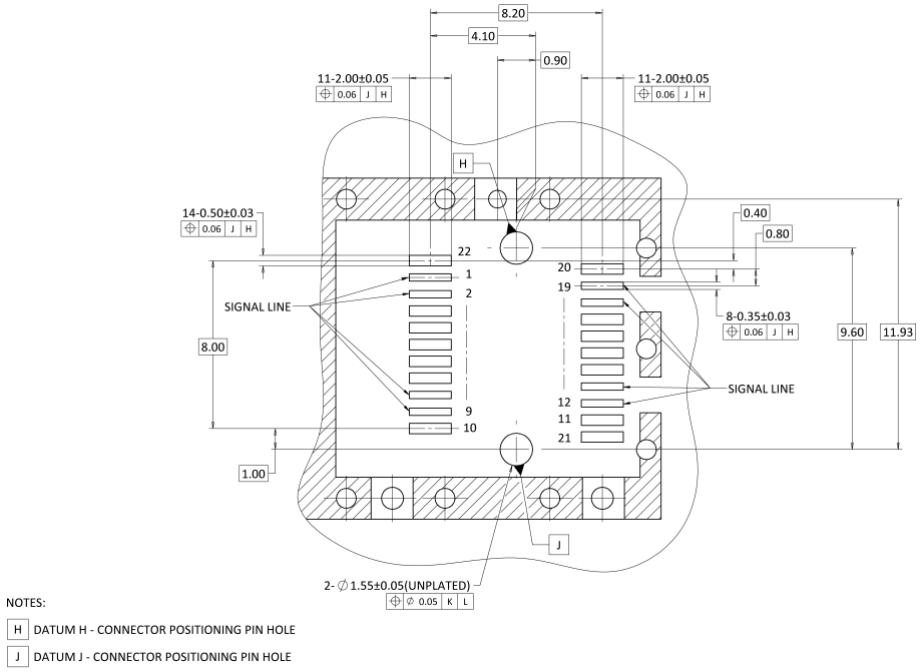

Figure 22: DSFP SMT Connector PCB Layout

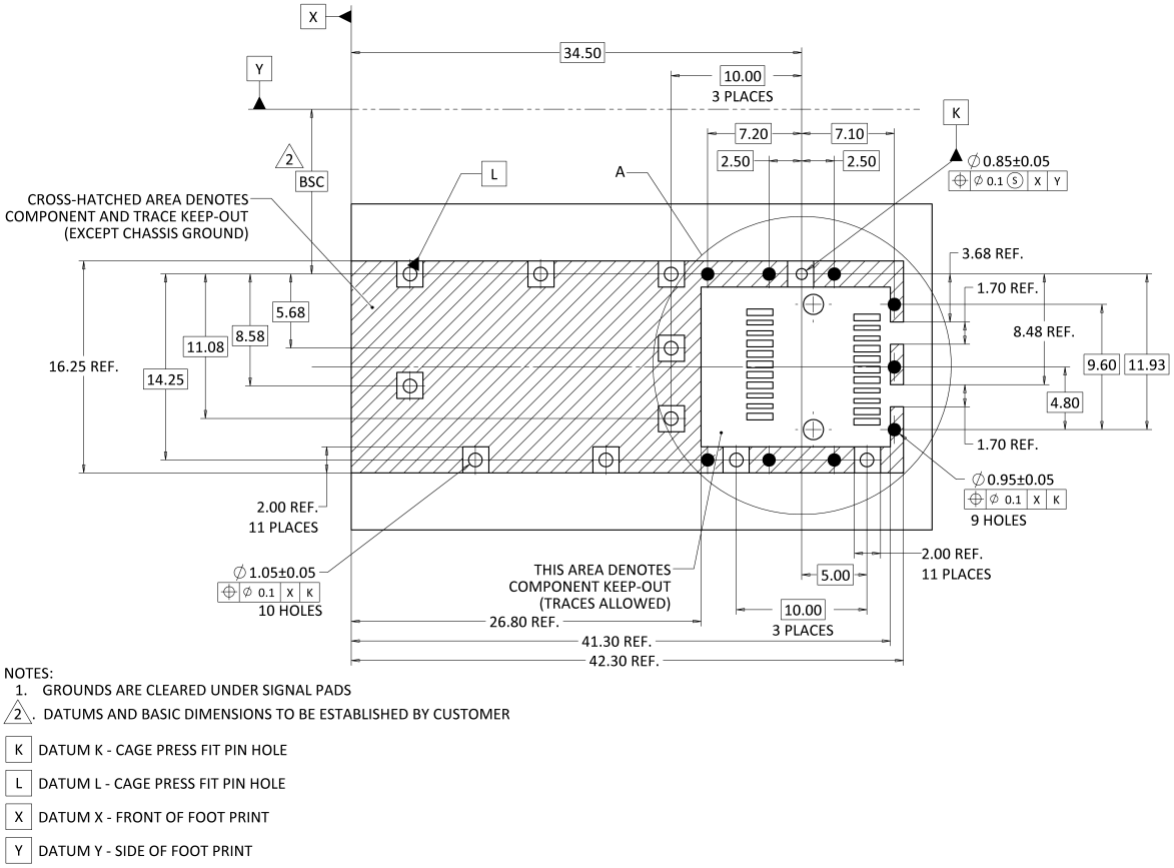

Figure 23: DSFP 1x1 SMT Connector and Cage Layout

5.7 Insertion, Extraction, and Retention Forces for DSFP Module

DSFP module and cage system insertion, extraction, and retentions forces are given in Table 5-2. DSFP connector and cage retention system are designed to withstand excessive force applied through the module or cable. The general requirement as applied to the values in the table is that no functional damage shall occur to the module, connector or cage.

Table 5-2: Insertion, extraction, and retention forces for an DSFP module

Measurement	Min	Max	Units	Comments
DSFP Module Extraction	0	12.5	N	Module extraction force without aid from cage kick-out springs and extraction force shall not increase by more than 5N for a module with riding heat sink
DSFP Module Insertion		18	N	Module insertion force without aid from cage kick-out springs and extraction force shall not increase by more than 5N for a module with riding heat sink (40N max for modules with kick-out springs)
DSFP Module Retention in Cage	90		N	No functional damage to module, connector, or cage
Cage kickout spring force	0	22	N	Optional
Insertion removal cycles connector	100	NA	N	Connector and cage durability
Insertion removal cycles module	50	NA	N	DSFP module durability.