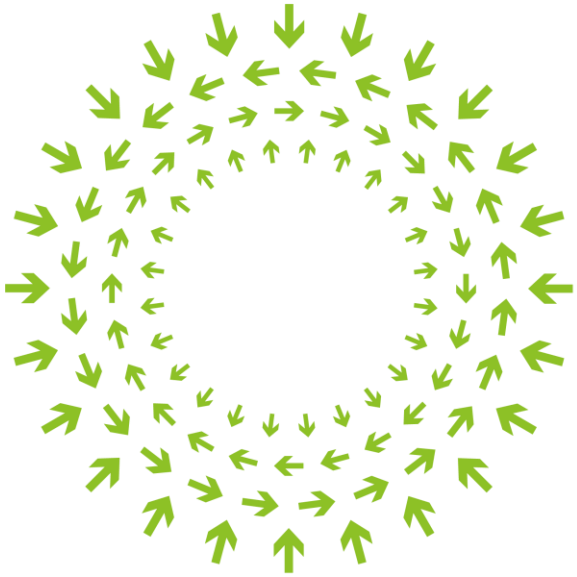

OPEN

Compute Project

CIG CS6436-56P

48 x 25GE + 8 x 100GE Switch

Authors:

Zheng Zhang, System Engineer, CIG

REVISION HISTORY

Date	Version	Author	Description
2/26/2019	0.8	Zhangzheng	Initial draft
4/18/2019	0.9	Zhangzheng	Integrate review comments; add the SONIC link

CONTENTS

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Device	Vendor	Part Number
CPU	Intel	x5-E3940
CPU	Intel	C3758
Switch	Nephos	NP8366
Switch	Marvell	88E6320
BMC	Aspeed	AST2520
CPLD	Lattice	LCMXO3LF-2100C-5BG2256C
CPLD	Lattice	LCMXO3LF-1300C-5BG256C
USB	MicroChip	USB2513
EEPROM	ON	CAT24C128
I2C	TI	PCA9548; PCA9534
LED control	TI	74HC595
Clock	TI	LMK03318
Temperature Sensor	TI	TMP75
Power Control	Lattice	PWR1014a
PSU	Delta	DPS550AB22A AC
PSU	Delta	DPS800AB14A DC
PSU	Suplet	SAC550-220D12 AC

FAN	Silergy	SY6875

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2. Scope

This document outlines the technical specifications for CIG CS6436-56P open switch platform submitted to Open Compute Project Foundation.

3. Overview

This document describes the technical specifications of CS6436-56P Top of Rack switch designed by Cambridge Industries Group (CIG). The CS6436-56P is a cost optimized design focused on the Top of Rack deployments which supports 10G/25G equipment connectivity and providing 100G uplink connections.

The CS6436-56P supports forty eight SFP28 ports, eight QSFP28 ports.

The CS6436-56P is a PHY-Less design with the SFP28 and QSFP28 connections directly attaching to the SerDes interfaces of the Nephos NP8366 switching silicon providing the lowest cost, latency, and power.

3.1 CS6436-56P Feature lists

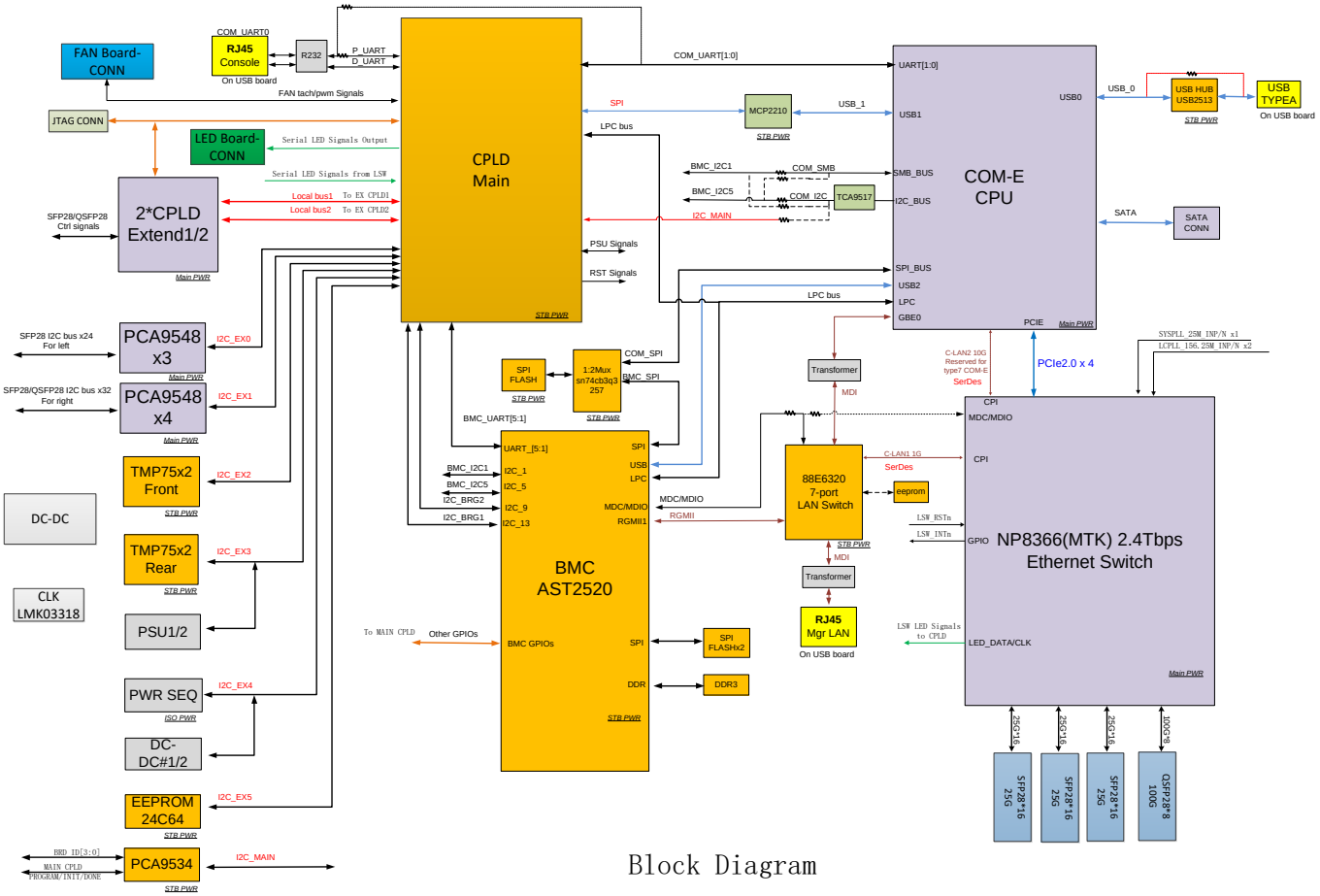
CS6436-56P major features are:

- Nephos NP8366 switch device
  - ✧ The NP8366 is a multiplayer Ethernet designed for data center and enterprise. Multiple 10G, 25G, 40G, 50G and 100G ports are supported to deliver exceptional performance requirements in various environments.
  - ✧ Supports 24 SerDes Macro up to 2.4Tbps
  - ✧ PCIE Gen2/3, 4 lane control interface
- COM-E CPU module option #1
  - ✧ Intel® Atom™ processor x5-E3940
  - ✧ Four Core, 1.8GHz,
  - ✧ TDP 9.5W
  - ✧ 8GB DDR3L SODIMM with ECC
- COM-E CPU module option #2
  - ✧ Intel Atom® Processor C3758
  - ✧ 8 cores, 2.2GHz
  - ✧ TDP 25W
  - ✧ 16MB L2 cache
  - ✧ Integrated Intel® QuickAssist Technology
  - ✧ 32GB DDR4 SODIMM with ECC
  - ✧ support 4 x 10GbE interfaces
-
- Network interface
  - ✧ 48 SFP28 25GE + 8 QSFP28 40GE/100GE
- Front panel management and debug interface
  - ✧ 10/100/1000 RJ45 GE management
  - ✧ RJ45 console port
  - ✧ Type-A USB2.0 port
- FAN tray
  - ✧ Five (4+1) redundant fan-tray on rear pane, hot swappable
  - ✧ Support for “Front to Back” or “Back to Front” air flow direction

- ✧ Screw-less design
- Power
  - ✧ Dual redundant PSU (1+1)

3.2 Block diagram

The following figure illustrates the functional block diagram of CS6436-56P system.



Block Diagram

Figure 1: CS6436-56P block diagram

3.3 Physical Overview

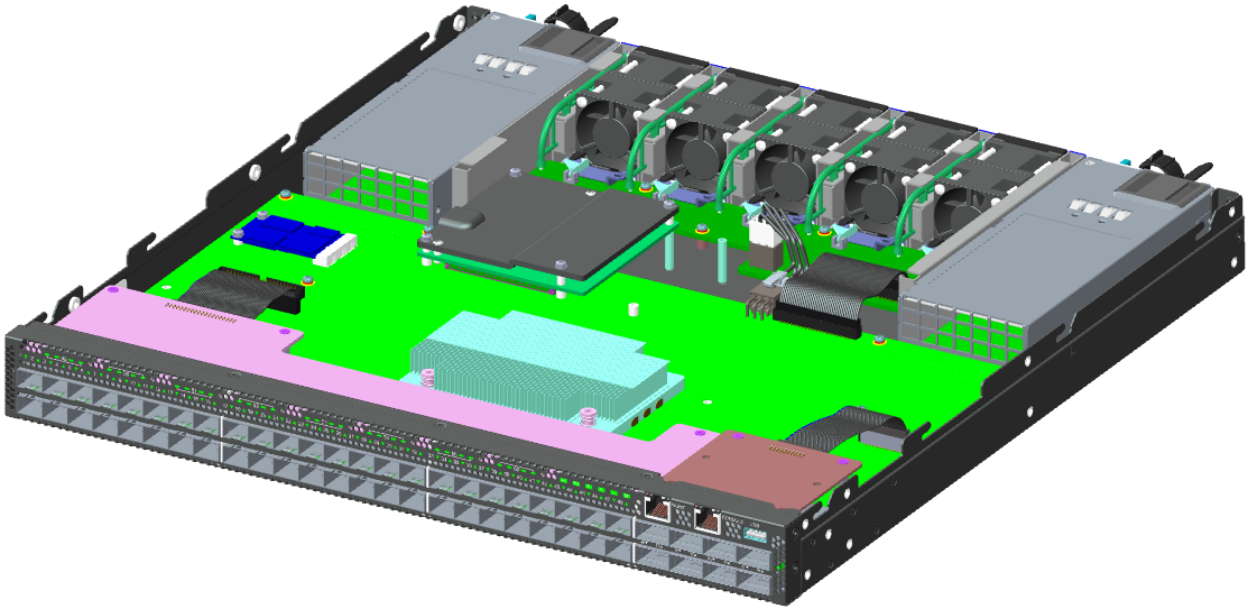


Figure 2: ISO view of standard 19-inch SKU

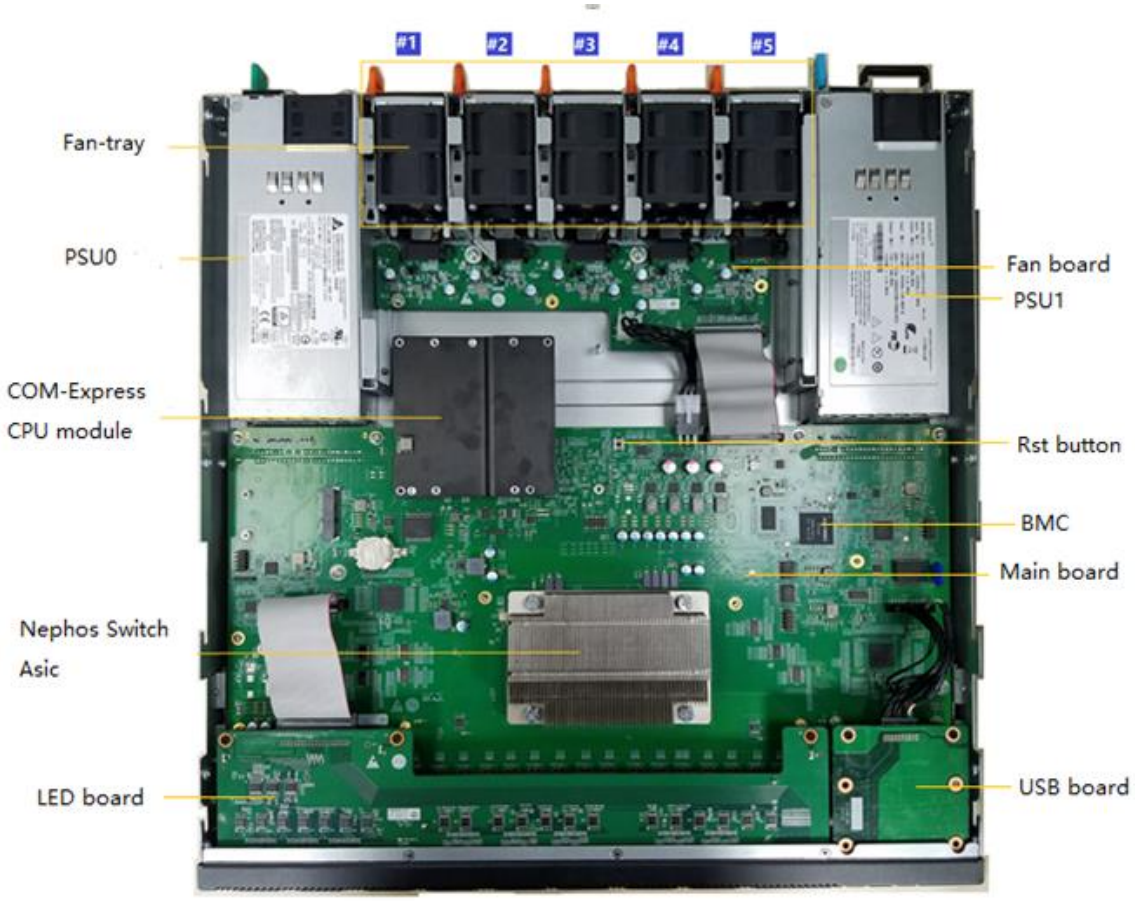


Figure 3: Top view of standard 19-inch SKU

4. CS6436 Mechanical Specification

4.1 Chassis Dimension

Height: 43.6mm (maximum)

Width: 442mm

Depth: 450mm

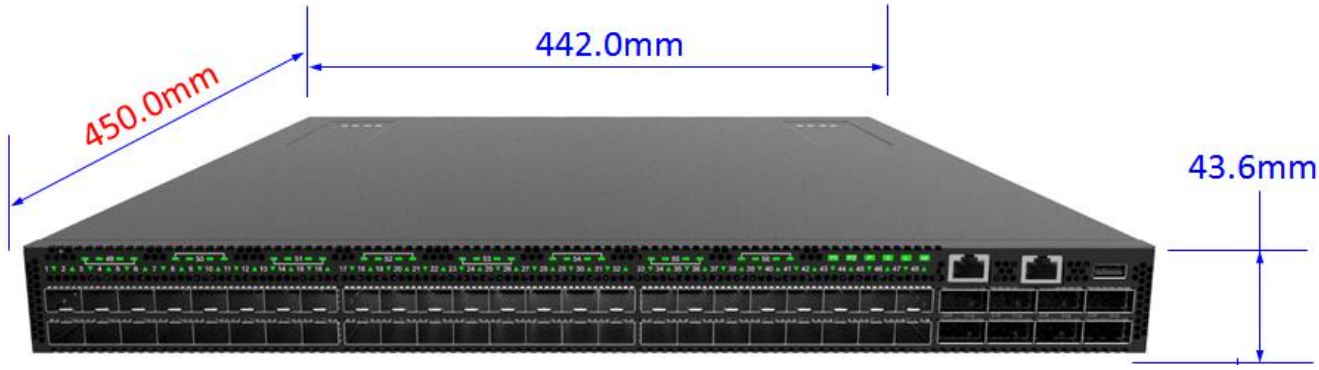


Figure 4: Chassis dimension

4.2 COM-E PCB Dimension

The following two figures show the detail of the COM-E PCB dimension. Its dimension is as below:

Option #1: 95mm(L) * 95mm(W) * 2.0mm(H)

Option #2: 95mm(L) * 125mm(W) * 2.0mm(H)

COM-E CPU module can be used in different platforms and systems.

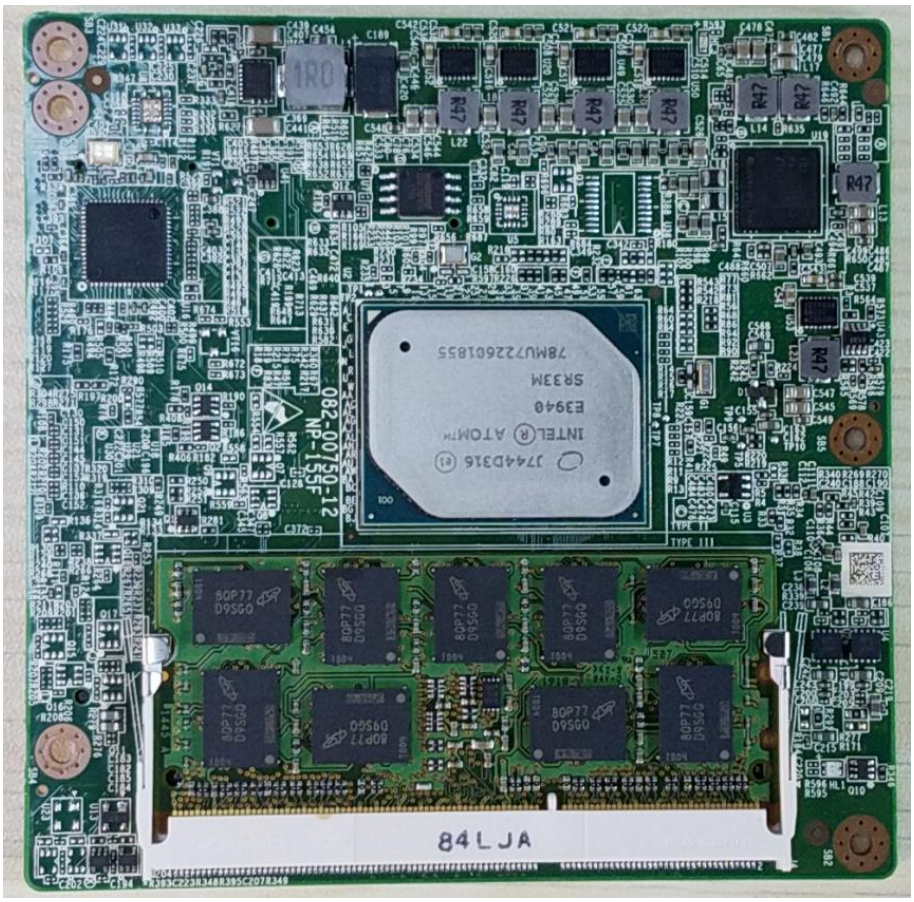


Figure 5: Option #1 COM-E CPU module top side

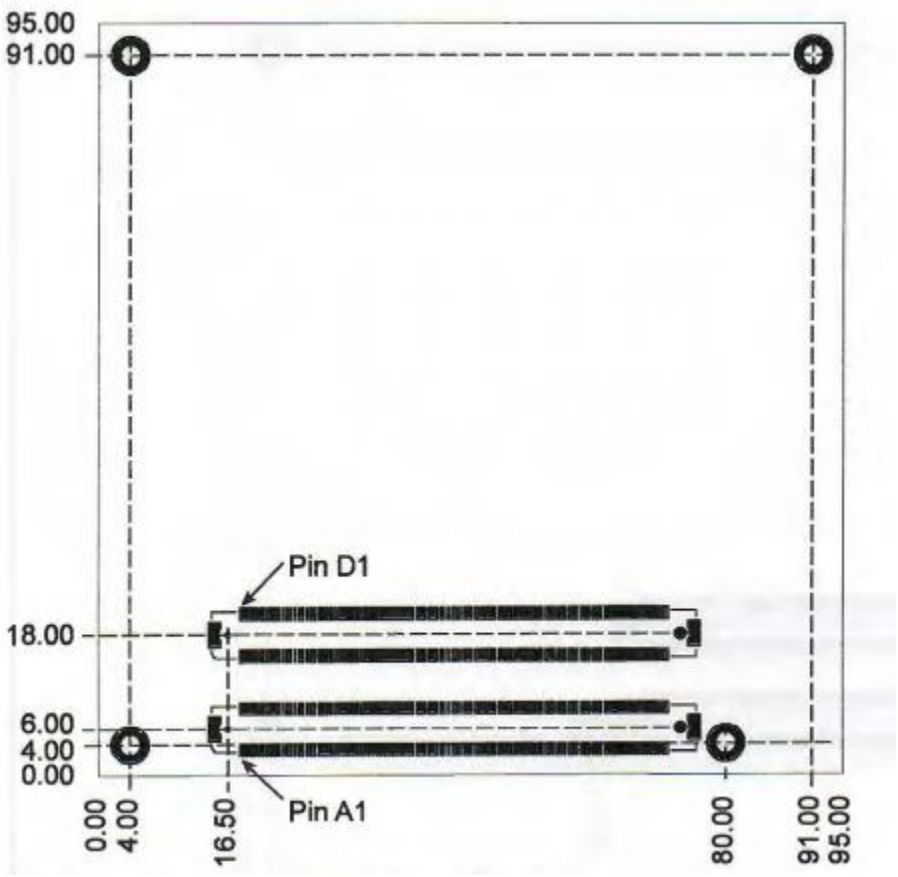


Figure 6: Option #1 COM-E CPU module dimension

All dimensions are shown in millimeters.

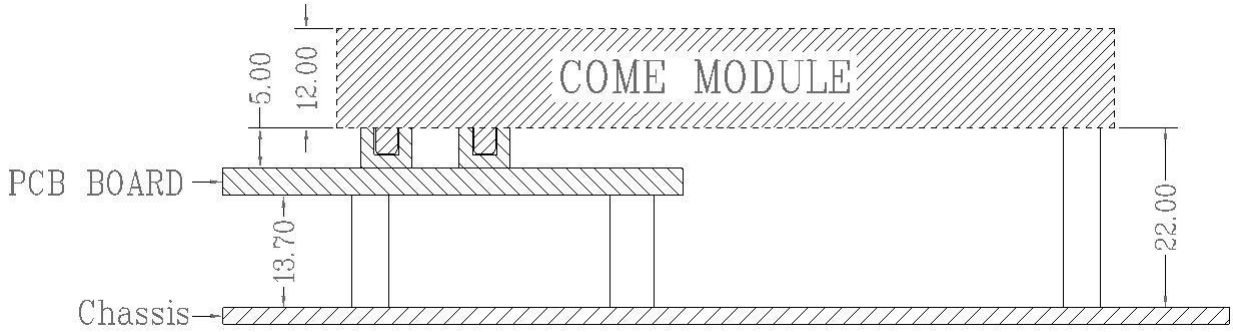


Figure 7: COM-E CPU module mounting profile

4.3 PSU

CS6436-56P can use the following PSU from DELTA or SUPLET power solutions:

- SUPLET SAC550-220D12-12: AC input PSU, 550W;

- DELTA DPS550AB22A: AC input PSU, 550W;
- DELTA DPS800AB14A: DC input PSU, 800W;

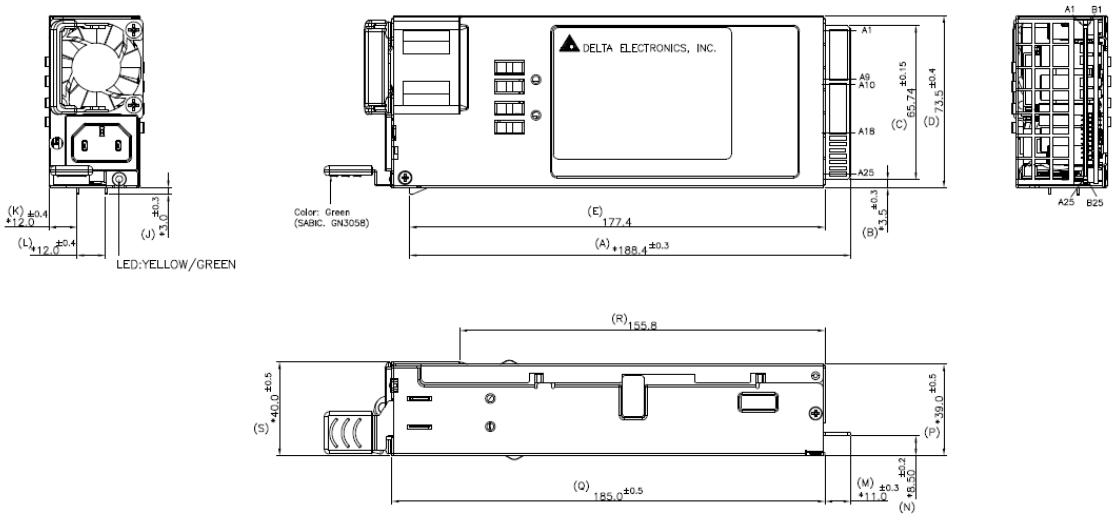


Figure 8: PSU mechanic drawing

4.3.1 PSU output

The following table shows the output ratings of PSU:

Input	Output	Voltage (V)	Current (A)	Power (W)	Ambient Temp Range	Model
90~264Vac	+12V	12	46	550W	0~50℃	SAC550-220D12-12
	+12VSB	12	2.1			
90~264Vac	+12V	12	45.8	550W	0~50℃	DPS550AB22A
	+12VSB	12	2.1			
-40~-72Vdc	+12V	12	65	800W	0~50℃	DPS800AB14A
	+12VSB	12	2			

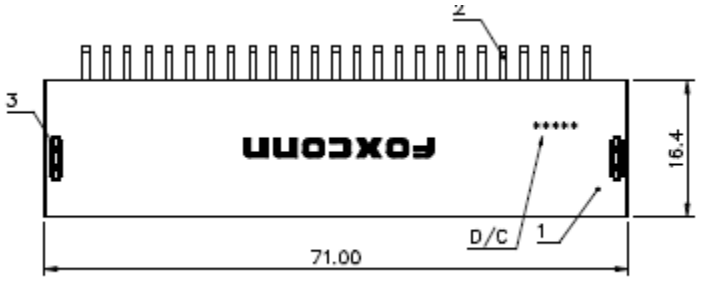
Table1: PSU output

4.3.2 PSU output connector

PSU side: golden finger. The following figure shows the output pin assignment.

PIN	SIGNAL NAME	PIN	SIGNAL NAME
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V
A17	+12V	B17	+12V
A18	+12V	B18	+12V
A19	SDA	B19	A0
A20	SCL	B20	A1
A21	PSON#	B21	+12VSB
A22	SMBAlert#	B22	Smart_On
A23	RS−	B23	+12VLS
A24	RS+	B24	N/C
A25	PWOK	B25	N/C

Chassis side: FOXCONN P/N: 2ES1253-D88NL-4F



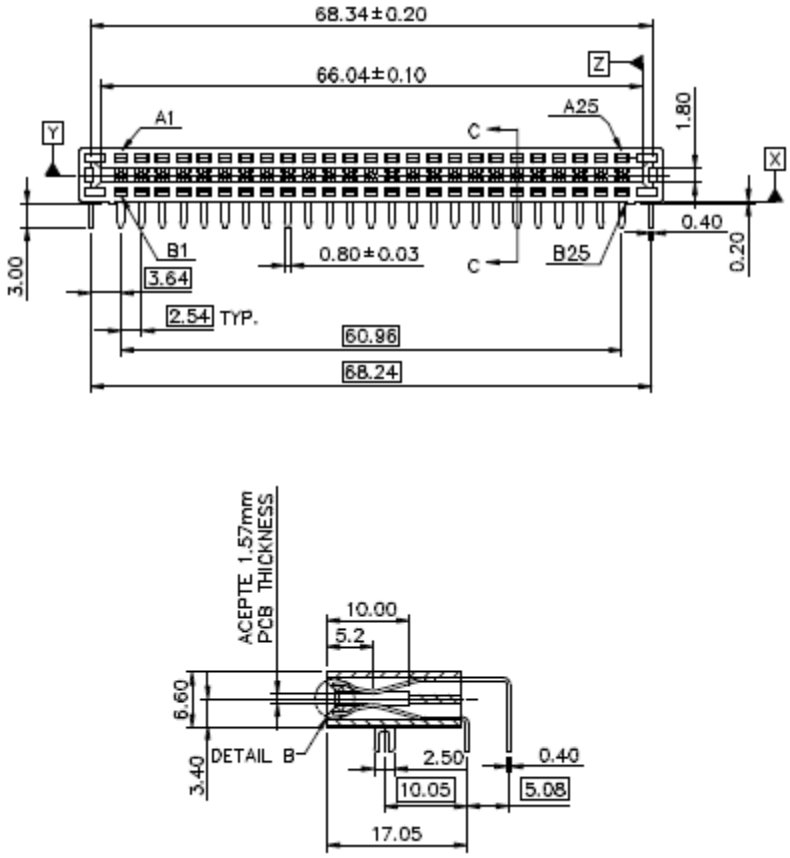


Figure 9: PSU connector

4.3.3 PSU airflow direction

The AC PSUs support bi-airflow directions. The normal airflow (air out) means the air enters the PSU at DC output side and exits through the AC inlet side. The reverse airflow (air in) means the air enters the PSU at AC inlet side and exit through the DC output side.

4.3.4 PSU I2c address

A0 and A1 signals are used to set the I2c address of the PSU.

A0	A1	EEPROM Address	MCU Address
0	0	0x50	0x58
0	1	0x51	0x59
1	0	0x52	0x5a
1	1	0x53	0x5b

Table2: PSU I2c address

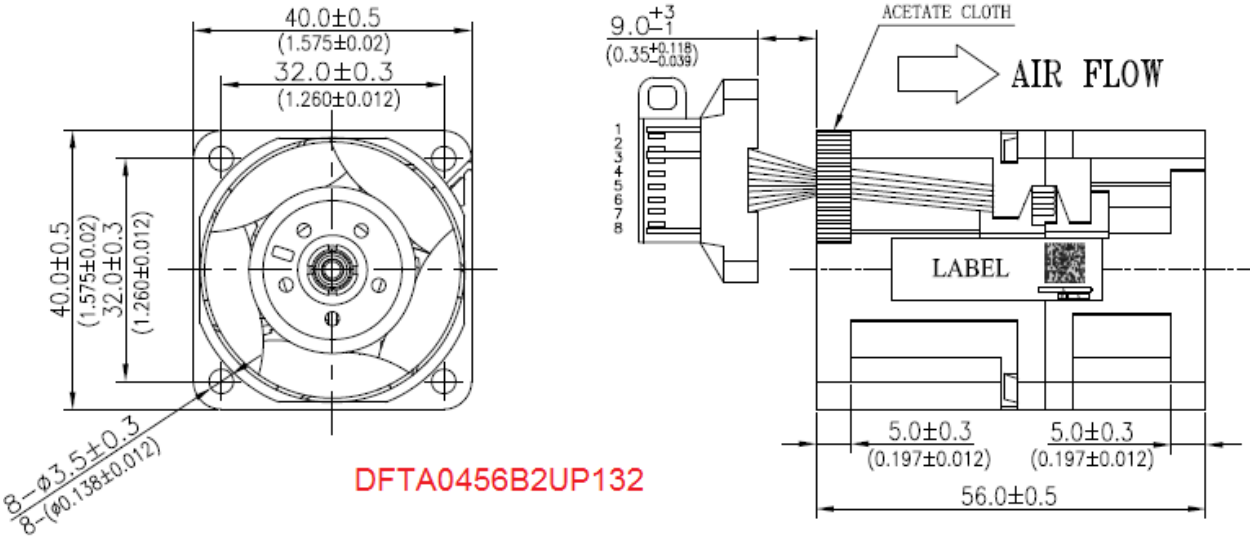
On CS6436-56P, PSU0 I2c is 0x52 for EEPROM and 0x5a for MCU. PSU1 I2c is 0x53 for EEPROM and 0x5b for MCU.

4.4 Fan tray

CS6436-56P supports 5 hot-swap fan trays. The air flow can be selected between air in and air out.

Figure 10: Fan tray

Fan tray use AVC fan DFTA0456B2UP132 (air out) or DFTA0456B2UP138 (air in).



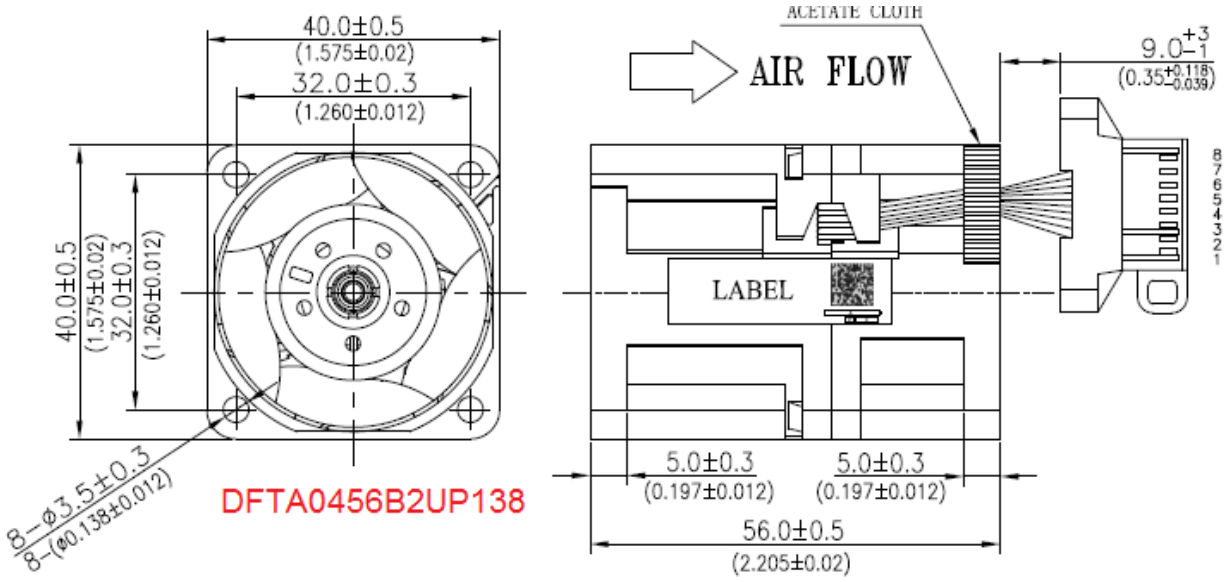


Figure 11: Fan tray mechanic drawing

(AT Ta=25°C)

ITEM	SPEC.		
RATED VOLTAGE	12		VDC
OPERATION VOLTAGE	7.0 ~ 13.2		VDC
RATED CURRENT (IN FREE AIR)	1.45 (1.70 MAX.)		A (AVERAGE)
CURRENT ON LABEL	1.70 A		
RATED POWER (IN FREE AIR)	17.40(19.20 MAX.)		W
SPEED (IN FREE AIR)	4033	21000±10%	R.P.M
	4023	19000±10%	R.P.M
SPEED CONTROL TYPE	PWM CONTROLLER		
SIGNAL OUTPUT	FREQUENCY GENERATOR (FG)		
MAX. AIR FLOW (AT ZERO STATIC PRESSURE)	0.92 (0.83 MIN.)		M^3/MIN
	32.48 (29.23 MIN.)		CFM
MAX. AIR PRESSURE (AT ZERO FLOW)	101.16(81.94 MIN.)		mm−H_2O
	3.98 (3.22 MIN.)		inch−H_2O
ACOUSTICAL NOISE	67.5 (71.5 MAX.)		dB−A

Table3: Fan Specification

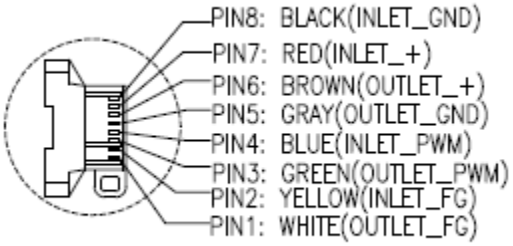


Figure12: Fan pin definition

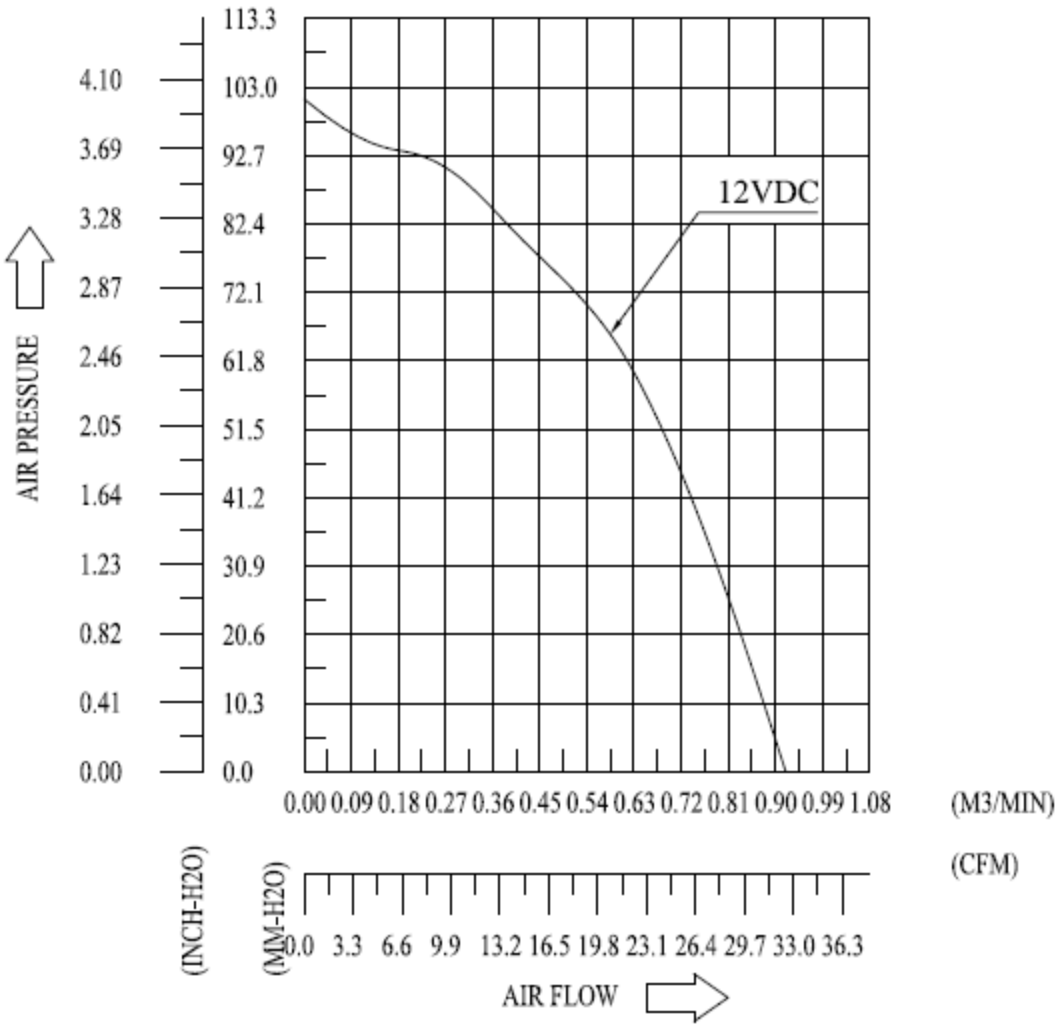


Figure13: Fan PQ Curve

4.5 CS6436 PLACEMENT AND LAYOUT

4.5.1 Top View

The CS6436-56P has five boards. The following picture shows their locations in the system.

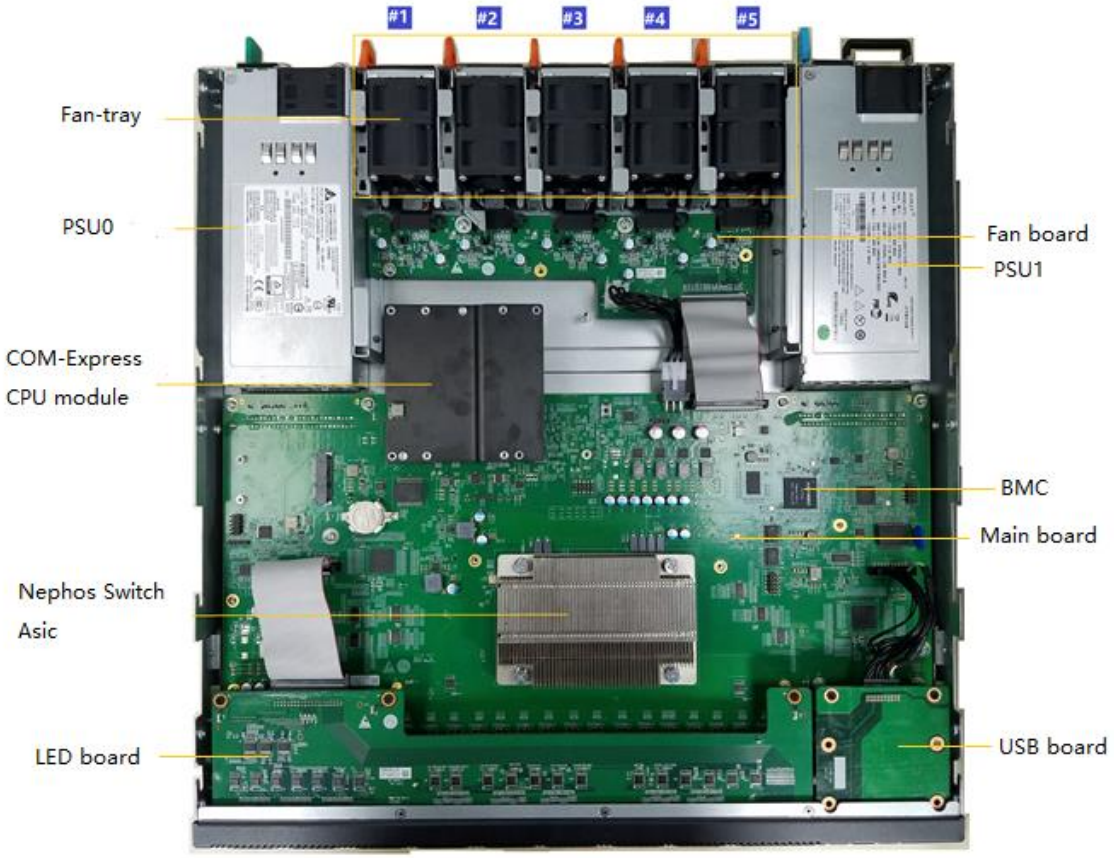


Figure 14: Top view of CS6436-56P

4.5.2 Front View

Figure 15: Front view of CS6436-56P

The front panel view of the CS6436-56P includes the following key components:

- Forty Eight SFP28 Ports
- Eight QSFP28 ports
- System LEDS： P1/P2/F/S/L/M
- RJ45 100/1000 Ethernet management port

- RJ45 RS232 management port
- USB 2.0 type A port

4.5.3 Rear View

Air Out:

Air In:

Figure 16: Rear view of CS6436-56P

The rear view of the CS6436-56P includes the following key components:

- Five (4+1) redundant hot swappable fan modules
  - LED per fan module to indicate status
- Two redundant hot swappable power supply modules
  - LED per power supply to indicate status

5. CS6436-56P THERMAL

5.1 Operational Ambient Temperatures

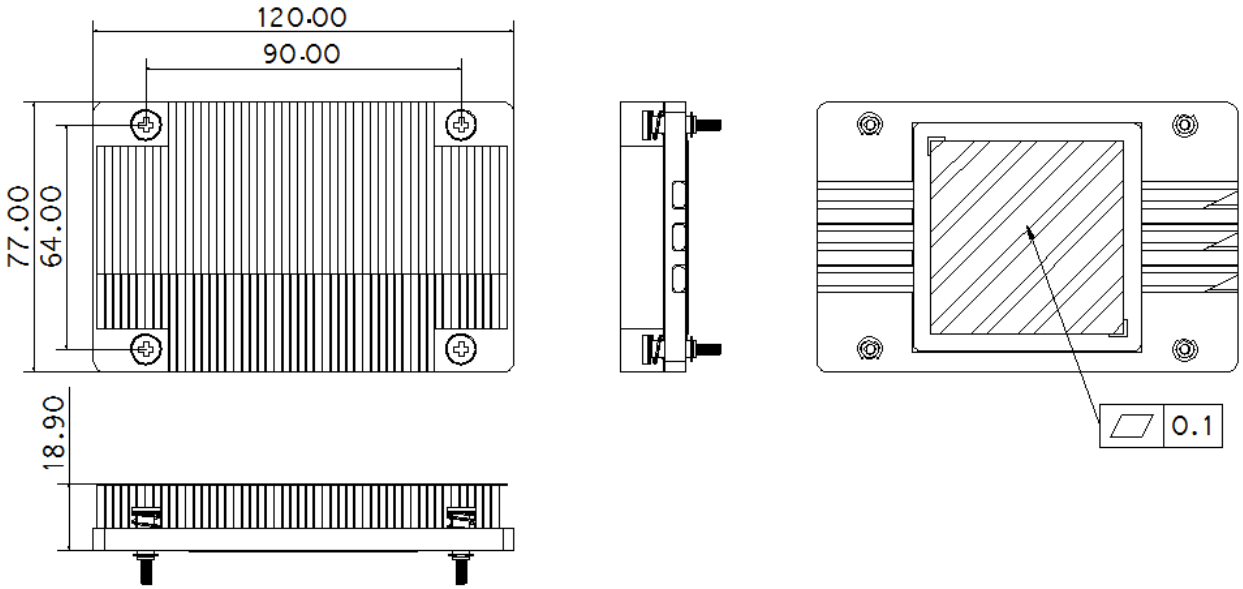
The operational ambient temperatures for CS6436-56P are:

- 0C to 45C, normal operation with 70C case-temperature SFP28 optics
- 0C to 45C, normal operation with 70C case-temperature QSFP28 optics

5.2 NP8366 THERMAL DESIGN

NP8366 consumes about 107w under typical condition and worst scenario. It is required for NP8366 to use advanced heat sink to support 107w operation at the ambient temperature of 0 - 70C. The heat sink could be the following design:

- Solder fin design
- Alumina base with embedded copper heat-pipe. 3 heat-pipe design is recommended.
- Proper heatsink mounting design to avoid tilting of heatsink during shock and vibration



5.3 TEMPERATURE SENSORS

There are four temperature sensors in CS6436-56P, and the locations are shown in the picture below. CPU can access the sensor via I2C bus. NP8366's junction temperature can also be read by CPU.

The temperature sensor solution is TMP75.

Figure 17: Temp sensor locations

6. CS6436 Main Board Electrical Specification

6.1 Switch NP8366

6.1.1 Switch Diagram

Switch NP8366 is used to support 48x25G and 8x100G ports. CPU can use PICe x4 to access this switching device. Serial LED signal is connected to CPLD, which can add some bits and transmit serial LED data to 74HC595s.

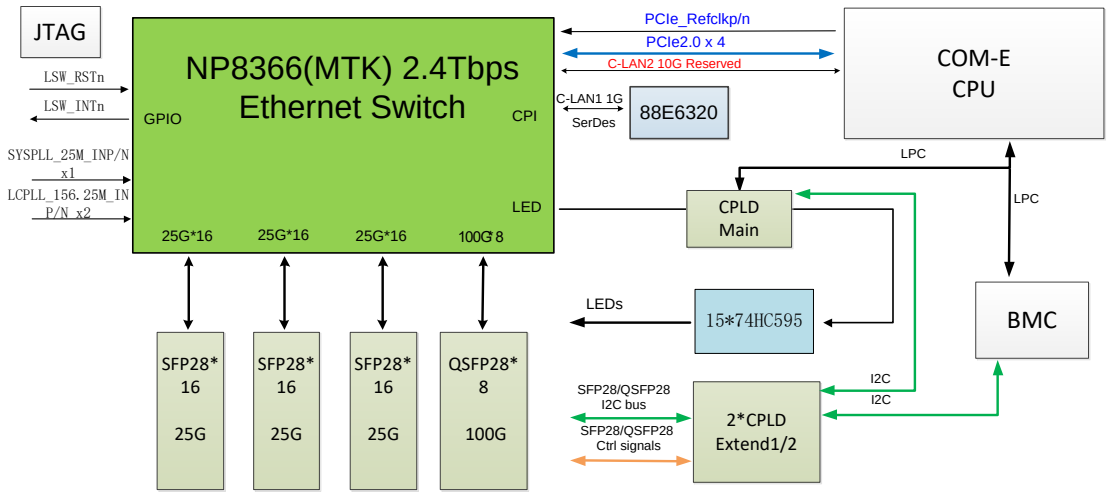


Figure 18: NP8366 diagram

6.1.2 NP8366 Switch Port Map

The lower left port is the first port; the port map is illustrated in the following figure:

25G port:

Front SFP28 port	NP8366 pin number	NP8366 pin name	net name
Port1	PIN_L10	ETHC02_RXP0	PORT0_ETHC02_RXP0
	PIN_L9	ETHC02_RXN0	PORT0_ETHC02_RXN0
	PIN_L4	ETHC02_TXP0	PORT0_ETHC02_TXP0
	PIN_L3	ETHC02_TXN0	PORT0_ETHC02_TXN0
Port2	PIN_L6	ETHC02_RXP1	PORT1_ETHC02_RXP1
	PIN_L7	ETHC02_RXN1	PORT1_ETHC02_RXN1
	PIN_M1	ETHC02_TXP1	PORT1_ETHC02_TXP1
	PIN_M2	ETHC02_TXN1	PORT1_ETHC02_TXN1
Port3	PIN_N10	ETHC02_RXP2	PORT2_ETHC02_RXP2
	PIN_N9	ETHC02_RXN2	PORT2_ETHC02_RXN2
	PIN_N4	ETHC02_TXP2	PORT2_ETHC02_TXP2
	PIN_N3	ETHC02_TXN2	PORT2_ETHC02_TXN2
Port4	PIN_N6	ETHC02_RXP3	PORT3_ETHC02_RXP3
	PIN_N7	ETHC02_RXN3	PORT3_ETHC02_RXN3
	PIN_P1	ETHC02_TXP3	PORT3_ETHC02_TXP3
	PIN_P2	ETHC02_TXN3	PORT3_ETHC02_TXN3
Port5	PIN_R6	ETHC03_RXP2	PORT4_ETHC03_RXP2
	PIN_R7	ETHC03_RXN2	PORT4_ETHC03_RXN2
	PIN_T1	ETHC03_TXP2	PORT4_ETHC03_TXP2
	PIN_T2	ETHC03_TXN2	PORT4_ETHC03_TXN2
Port6	PIN_R10	ETHC03_RXP3	PORT5_ETHC03_RXP3
	PIN_R9	ETHC03_RXN3	PORT5_ETHC03_RXN3
	PIN_R4	ETHC03_TXP3	PORT5_ETHC03_TXN3

	PIN_R3	ETHC03_TXN3	PORT5_ETHC03_TXP3
Port7	PIN_U6	ETHC03_RXP0	PORT6_ETHC03_RXP0
	PIN_U7	ETHC03_RXN0	PORT6_ETHC03_RXN0
	PIN_V1	ETHC03_TXP0	PORT6_ETHC03_TXP0
	PIN_V2	ETHC03_TXN0	PORT6_ETHC03_TXN0
Port8	PIN_U10	ETHC03_RXP1	PORT7_ETHC03_RXP1
	PIN_U9	ETHC03_RXN1	PORT7_ETHC03_RXN1
	PIN_U4	ETHC03_TXP1	PORT7_ETHC03_TXP1
	PIN_U3	ETHC03_TXN1	PORT7_ETHC03_TXN1
Port9	PIN_W10	ETHC04_RXP0	PORT8_ETHC04_RXP0
	PIN_W9	ETHC04_RXN0	PORT8_ETHC04_RXN0
	PIN_W4	ETHC04_TXP0	PORT8_ETHC04_TXP0
	PIN_W3	ETHC04_TXN0	PORT8_ETHC04_TXN0
Port10	PIN_W6	ETHC04_RXP1	PORT9_ETHC04_RXP1
	PIN_W7	ETHC04_RXN1	PORT9_ETHC04_RXN1
	PIN_Y1	ETHC04_TXP1	PORT9_ETHC04_TXP1
	PIN_Y2	ETHC04_TXN1	PORT9_ETHC04_TXN1
Port11	PIN_AA10	ETHC04_RXP2	PORT10_ETHC04_RXP2
	PIN_AA9	ETHC04_RXN2	PORT10_ETHC04_RXN2
	PIN_AA4	ETHC04_TXP2	PORT10_ETHC04_TXP2
	PIN_AA3	ETHC04_TXN2	PORT10_ETHC04_TXN2
Port12	PIN_AA6	ETHC04_RXP3	PORT11_ETHC04_RXP3
	PIN_AA7	ETHC04_RXN3	PORT11_ETHC04_RXN3
	PIN_AB1	ETHC04_TXP3	PORT11_ETHC04_TXP3
	PIN_AB2	ETHC04_TXN3	PORT11_ETHC04_TXN3
Port13	PIN_AC10	ETHC05_RXP3	PORT12_ETHC05_RXP3
	PIN_AC9	ETHC05_RXN3	PORT12_ETHC05_RXN3
	PIN_AD1	ETHC05_TXP2	PORT12_ETHC05_TXP2
	PIN_AD2	ETHC05_TXN2	PORT12_ETHC05_TXN2
Port14	PIN_AC6	ETHC05_RXP2	PORT13_ETHC05_RXP2
	PIN_AC7	ETHC05_RXN2	PORT13_ETHC05_RXN2
	PIN_AC4	ETHC05_TXP3	PORT13_ETHC05_TXP3
	PIN_AC3	ETHC05_TXN3	PORT13_ETHC05_TXN3
Port15	PIN_AE6	ETHC05_RXP1	PORT14_ETHC05_RXP1
	PIN_AE7	ETHC05_RXN1	PORT14_ETHC05_RXN1
	PIN_AF2	ETHC05_TXP0	PORT14_ETHC05_TXP0
	PIN_AF1	ETHC05_TXN0	PORT14_ETHC05_TXN0
Port16	PIN_AE10	ETHC05_RXP0	PORT15_ETHC05_RXP0
	PIN_AE9	ETHC05_RXN0	PORT15_ETHC05_RXN0
	PIN_AE4	ETHC05_TXP1	PORT15_ETHC05_TXP1
	PIN_AE3	ETHC05_TXN1	PORT15_ETHC05_TXN1
Port17	PIN_AR10	ETHC08_RXP0	PORT16_ETHC08_RXP0
	PIN_AR9	ETHC08_RXN0	PORT16_ETHC08_RXN0
	PIN_AR3	ETHC08_TXP3	PORT16_ETHC08_TXP3
	PIN_AR4	ETHC08_TXN3	PORT16_ETHC08_TXN3
Port18	PIN_AT2	ETHC08_TXP2	PORT17_ETHC08_TXP2
	PIN_AT1	ETHC08_TXN2	PORT17_ETHC08_TXN2
	PIN_AR6	ETHC08_RXP3	PORT17_ETHC08_RXP3
	PIN_AR7	ETHC08_RXN3	PORT17_ETHC08_RXN3
Port19	PIN_AV1	ETHC08_TXP1	PORT18_ETHC08_TXP1
	PIN_AV2	ETHC08_TXN1	PORT18_ETHC08_TXN1
	PIN_AU9	ETHC08_RXP2	PORT18_ETHC08_RXP2
	PIN_AU10	ETHC08_RXN2	PORT18_ETHC08_RXN2
Port20	PIN_AU3	ETHC08_TXP0	PORT19_ETHC08_TXP0
	PIN_AU4	ETHC08_TXN0	PORT19_ETHC08_TXN0
	PIN_AU6	ETHC08_RXP1	PORT19_ETHC08_RXP1
	PIN_AU7	ETHC08_RXN1	PORT19_ETHC08_RXN1
Port21	PIN_BJ3	ETHC10_RXP0	PORT20_ETHC10_RXP0
	PIN_BH3	ETHC10_RXN0	PORT20_ETHC10_RXN0

	PIN_BP4	ETHC10_TXP2	PORT20_ETHC10_TXP2
	PIN_BN4	ETHC10_TXN2	PORT20_ETHC10_TXN2
Port22	PIN_BE3	ETHC10_RXP3	PORT21_ETHC10_RXP3
	PIN_BF3	ETHC10_RXN3	PORT21_ETHC10_RXN3
	PIN_BL3	ETHC10_TXP3	PORT21_ETHC10_TXP3
	PIN_BM3	ETHC10_TXN3	PORT21_ETHC10_TXN3
Port23	PIN_BH5	ETHC10_RXP2	PORT22_ETHC10_RXP2
	PIN_BJ5	ETHC10_RXN2	PORT22_ETHC10_RXN2
	PIN_BN6	ETHC10_TXP0	PORT22_ETHC10_TXP0
	PIN_BP6	ETHC10_TXN0	PORT22_ETHC10_TXN0
Port24	PIN_BE5	ETHC10_RXP1	PORT23_ETHC10_RXP1
	PIN_BF5	ETHC10_RXN1	PORT23_ETHC10_RXN1
	PIN_BL5	ETHC10_TXP1	PORT23_ETHC10_TXP1
	PIN_BM5	ETHC10_TXN1	PORT23_ETHC10_TXN1
Port25	PIN_BJ11	ETHC12_RXP0	PORT24_ETHC12_RXP0
	PIN_BH11	ETHC12_RXN0	PORT24_ETHC12_RXN0
	PIN_BP12	ETHC12_TXP2	PORT24_ETHC12_TXP2
	PIN_BN12	ETHC12_TXN2	PORT24_ETHC12_TXN2
Port26	PIN_BE11	ETHC12_RXP3	PORT25_ETHC12_RXP3
	PIN_BF11	ETHC12_RXN3	PORT25_ETHC12_RXN3
	PIN_BL11	ETHC12_TXP3	PORT25_ETHC12_TXP3
	PIN_BM11	ETHC12_TXN3	PORT25_ETHC12_TXN3
Port27	PIN_BH13	ETHC12_RXP2	PORT26_ETHC12_RXP2
	PIN_BJ13	ETHC12_RXN2	PORT26_ETHC12_RXN2
	PIN_BN14	ETHC12_TXP0	PORT26_ETHC12_TXP0
	PIN_BP14	ETHC12_TXN0	PORT26_ETHC12_TXN0
Port28	PIN_BE13	ETHC12_RXP1	PORT27_ETHC12_RXP1
	PIN_BF13	ETHC12_RXN1	PORT27_ETHC12_RXN1
	PIN_BL13	ETHC12_TXP1	PORT27_ETHC12_TXP1
	PIN_BM13	ETHC12_TXN1	PORT27_ETHC12_TXN1
Port29	PIN_BJ19	ETHC14_RXP0	PORT28_ETHC14_RXP0
	PIN_BH19	ETHC14_RXN0	PORT28_ETHC14_RXN0
	PIN_BP20	ETHC14_TXP2	PORT28_ETHC14_TXP2
	PIN_BN20	ETHC14_TXN2	PORT28_ETHC14_TXN2
Port30	PIN_BE19	ETHC14_RXP3	PORT29_ETHC14_RXP3
	PIN_BF19	ETHC14_RXN3	PORT29_ETHC14_RXN3
	PIN_BL19	ETHC14_TXP3	PORT29_ETHC14_TXP3
	PIN_BM19	ETHC14_TXN3	PORT29_ETHC14_TXN3
Port31	PIN_BH21	ETHC14_RXP2	PORT30_ETHC14_RXP2
	PIN_BJ21	ETHC14_RXN2	PORT30_ETHC14_RXN2
	PIN_BN22	ETHC14_TXP0	PORT30_ETHC14_TXP0
	PIN_BP22	ETHC14_TXN0	PORT30_ETHC14_TXN0
Port32	PIN_BE21	ETHC14_RXP1	PORT31_ETHC14_RXP1
	PIN_BF21	ETHC14_RXN1	PORT31_ETHC14_RXN1
	PIN_BL21	ETHC14_TXP1	PORT31_ETHC14_TXP1
	PIN_BM21	ETHC14_TXN1	PORT31_ETHC14_TXN1
Port33	PIN_BH30	ETHC16_RXP2	PORT32_ETHC16_RXP2
	PIN_BJ30	ETHC16_RXN2	PORT32_ETHC16_RXN2
	PIN_BN29	ETHC16_TXP0	PORT32_ETHC16_TXP0
	PIN_BP29	ETHC16_TXN0	PORT32_ETHC16_TXN0
Port34	PIN_BE30	ETHC16_RXP1	PORT33_ETHC16_RXP1
	PIN_BF30	ETHC16_RXN1	PORT33_ETHC16_RXN1
	PIN_BL30	ETHC16_TXP1	PORT33_ETHC16_TXP1
	PIN_BM30	ETHC16_TXN1	PORT33_ETHC16_TXN1
Port35	PIN_BJ32	ETHC16_RXP0	PORT34_ETHC16_RXP0
	PIN_BH32	ETHC16_RXN0	PORT34_ETHC16_RXN0
	PIN_BP31	ETHC16_TXP2	PORT34_ETHC16_TXP2
	PIN_BN31	ETHC16_TXN2	PORT34_ETHC16_TXN2
Port36	PIN_BE32	ETHC16_RXP3	PORT35_ETHC16_RXP3

	PIN_BF32	ETHC16_RXN3	PORT35_ETHC16_RXN3
	PIN_BL32	ETHC16_TXP3	PORT35_ETHC16_TXP3
	PIN_BM32	ETHC16_TXN3	PORT35_ETHC16_TXN3
Port37	PIN_BH34	ETHC17_RXP2	PORT36_ETHC17_RXP2
	PIN_BJ34	ETHC17_RXN2	PORT36_ETHC17_RXN2
	PIN_BN33	ETHC17_TXP0	PORT36_ETHC17_TXP0
	PIN_BP33	ETHC17_TXN0	PORT36_ETHC17_TXN0
Port38	PIN_BE34	ETHC17_RXP1	PORT37_ETHC17_RXP1
	PIN_BF34	ETHC17_RXN1	PORT37_ETHC17_RXN1
	PIN_BL34	ETHC17_TXP1	PORT37_ETHC17_TXP1
	PIN_BM34	ETHC17_TXN1	PORT37_ETHC17_TXN1
Port39	PIN_BJ36	ETHC17_RXP0	PORT38_ETHC17_RXP0
	PIN_BH36	ETHC17_RXN0	PORT38_ETHC17_RXN0
	PIN_BP35	ETHC17_TXP2	PORT38_ETHC17_TXP2
	PIN_BN35	ETHC17_TXN2	PORT38_ETHC17_TXN2
Port40	PIN_BE36	ETHC17_RXP3	PORT39_ETHC17_RXP3
	PIN_BF36	ETHC17_RXN3	PORT39_ETHC17_RXN3
	PIN_BL36	ETHC17_TXP3	PORT39_ETHC17_TXP3
	PIN_BM36	ETHC17_TXN3	PORT39_ETHC17_TXN3
Port41	PIN_BH38	ETHC18_RXP2	PORT40_ETHC18_RXP2
	PIN_BJ38	ETHC18_RXN2	PORT40_ETHC18_RXN2
	PIN_BN37	ETHC18_TXP0	PORT40_ETHC18_TXP0
	PIN_BP37	ETHC18_TXN0	PORT40_ETHC18_TXN0
Port42	PIN_BE38	ETHC18_RXP1	PORT41_ETHC18_RXP1
	PIN_BF38	ETHC18_RXN1	PORT41_ETHC18_RXN1
	PIN_BL38	ETHC18_TXP1	PORT41_ETHC18_TXP1
	PIN_BM38	ETHC18_TXN1	PORT41_ETHC18_TXN1
Port43	PIN_BJ40	ETHC18_RXP0	PORT42_ETHC18_RXP0
	PIN_BH40	ETHC18_RXN0	PORT42_ETHC18_RXN0
	PIN_BP39	ETHC18_TXP2	PORT42_ETHC18_TXP2
	PIN_BN39	ETHC18_TXN2	PORT42_ETHC18_TXN2
Port44	PIN_BE40	ETHC18_RXP3	PORT43_ETHC18_RXP3
	PIN_BF40	ETHC18_RXN3	PORT43_ETHC18_RXN3
	PIN_BL40	ETHC18_TXP3	PORT43_ETHC18_TXP3
	PIN_BM40	ETHC18_TXN3	PORT43_ETHC18_TXN3
Port45	PIN_BH42	ETHC19_RXP2	PORT44_ETHC19_RXP2
	PIN_BJ42	ETHC19_RXN2	PORT44_ETHC19_RXN2
	PIN_BN41	ETHC19_TXP0	PORT44_ETHC19_TXP0
	PIN_BP41	ETHC19_TXN0	PORT44_ETHC19_TXN0
Port46	PIN_BE42	ETHC19_RXP1	PORT45_ETHC19_RXP1
	PIN_BF42	ETHC19_RXN1	PORT45_ETHC19_RXN1
	PIN_BL42	ETHC19_TXP1	PORT45_ETHC19_TXP1
	PIN_BM42	ETHC19_TXN1	PORT45_ETHC19_TXN1
Port47	PIN_BJ44	ETHC19_RXP0	PORT46_ETHC19_RXP0
	PIN_BH44	ETHC19_RXN0	PORT46_ETHC19_RXN0
	PIN_BP43	ETHC19_TXP2	PORT46_ETHC19_TXP2
	PIN_BN43	ETHC19_TXN2	PORT46_ETHC19_TXN2
Port48	PIN_BE44	ETHC19_RXP3	PORT47_ETHC19_RXP3
	PIN_BF44	ETHC19_RXN3	PORT47_ETHC19_RXN3
	PIN_BL44	ETHC19_TXP3	PORT47_ETHC19_TXP3
	PIN_BM44	ETHC19_TXN3	PORT47_ETHC19_TXN3

100G port:

Front QSFP28 port	QSFP28 channel	NP8366 pin number	NP8366 pin name	net name

Port49	RX CH-N2	PIN_BJ52	ETHC21_RXP0	QSFP0_ETHC21_RXN1
	RX CH-P2	PIN_BH52	ETHC21_RXN0	QSFP0_ETHC21_RXP1
	RX CH-N3	PIN_BE50	ETHC21_RXP1	QSFP0_ETHC21_RXN2
	RX CH-P3	PIN_BF50	ETHC21_RXN1	QSFP0_ETHC21_RXP2
	RX CH-P1	PIN_BH50	ETHC21_RXP2	QSFP0_ETHC21_RXP0
	RX CH-N1	PIN_BJ50	ETHC21_RXN2	QSFP0_ETHC21_RXN0
	RX CH-N4	PIN_BE52	ETHC21_RXP3	QSFP0_ETHC21_RXN3
	RX CH-P4	PIN_BF52	ETHC21_RXN3	QSFP0_ETHC21_RXP3
	TX CH-P3	PIN_BN49	ETHC21_TXP0	QSFP0_ETHC21_TXP2
	TX CH-N3	PIN_BP49	ETHC21_TXN0	QSFP0_ETHC21_TXN2
	TX CH-P2	PIN_BL50	ETHC21_TXP1	QSFP0_ETHC21_TXP1
	TX CH-N2	PIN_BM50	ETHC21_TXN1	QSFP0_ETHC21_TXN1
	TX CH-P1	PIN_BP51	ETHC21_TXP2	QSFP0_ETHC21_TXP0
	TX CH-N1	PIN_BN51	ETHC21_TXN2	QSFP0_ETHC21_TXN0
	TX CH-P4	PIN_BL52	ETHC21_TXP3	QSFP0_ETHC21_TXP3
	TX CH-N4	PIN_BM52	ETHC21_TXN3	QSFP0_ETHC21_TXN3
Port50	RX CH-P1	PIN_BJ48	ETHC20_RXP0	QSFP1_ETHC20_RXP0
	RX CH-N1	PIN_BH48	ETHC20_RXN0	QSFP1_ETHC20_RXN0
	RX CH-P2	PIN_BE46	ETHC20_RXP1	QSFP1_ETHC20_RXP1
	RX CH-N2	PIN_BF46	ETHC20_RXN1	QSFP1_ETHC20_RXN1
	RX CH-P3	PIN_BH46	ETHC20_RXP2	QSFP1_ETHC20_RXP2
	RX CH-N3	PIN_BJ46	ETHC20_RXN2	QSFP1_ETHC20_RXN2
	RX CH-P4	PIN_BE48	ETHC20_RXP3	QSFP1_ETHC20_RXP3
	RX CH-N4	PIN_BF48	ETHC20_RXN3	QSFP1_ETHC20_RXN3
	TX CH-P1	PIN_BN45	ETHC20_TXP0	QSFP1_ETHC20_TXP0
	TX CH-N1	PIN_BP45	ETHC20_TXN0	QSFP1_ETHC20_TXN0
	TX CH-P2	PIN_BL46	ETHC20_TXP1	QSFP1_ETHC20_TXP1
	TX CH-N2	PIN_BM46	ETHC20_TXN1	QSFP1_ETHC20_TXN1
	TX CH-P3	PIN_BP47	ETHC20_TXP2	QSFP1_ETHC20_TXP2
	TX CH-N3	PIN_BN47	ETHC20_TXN2	QSFP1_ETHC20_TXN2
	TX CH-P4	PIN_BL48	ETHC20_TXP3	QSFP1_ETHC20_TXP3
	TX CH-N4	PIN_BM48	ETHC20_TXN3	QSFP1_ETHC20_TXN3
Port51	RX CH-N3	PIN_AR45	ETHC23_RXP0	QSFP2_ETHC23_RXN2
	RX CH-P3	PIN_AR46	ETHC23_RXN0	QSFP2_ETHC23_RXP2
	RX CH-N2	PIN_AU49	ETHC23_RXP1	QSFP2_ETHC23_RXN1
	RX CH-P2	PIN_AU48	ETHC23_RXN1	QSFP2_ETHC23_RXP1
	RX CH-N1	PIN_AU46	ETHC23_RXP2	QSFP2_ETHC23_RXN0
	RX CH-P1	PIN_AU45	ETHC23_RXN2	QSFP2_ETHC23_RXP0
	RX CH-N4	PIN_AR49	ETHC23_RXP3	QSFP2_ETHC23_RXN3
	RX CH-P4	PIN_AR48	ETHC23_RXN3	QSFP2_ETHC23_RXP3
	TX CH-P4	PIN_AU52	ETHC23_TXP0	QSFP2_ETHC23_TXP3
	TX CH-N4	PIN_AU51	ETHC23_TXN0	QSFP2_ETHC23_TXN3
	TX CH-P3	PIN_AV54	ETHC23_TXP1	QSFP2_ETHC23_TXP2
	TX CH-N3	PIN_AV53	ETHC23_TXN1	QSFP2_ETHC23_TXN2
	TX CH-P2	PIN_AT53	ETHC23_TXP2	QSFP2_ETHC23_TXP1
	TX CH-N2	PIN_AT54	ETHC23_TXN2	QSFP2_ETHC23_TXN1
	TX CH-P1	PIN_AR52	ETHC23_TXP3	QSFP2_ETHC23_TXP0
	TX CH-N1	PIN_AR51	ETHC23_TXN3	QSFP2_ETHC23_TXN0
Port52	RX CH-P1	PIN_AW45	ETHC22_RXP0	QSFP3_ETHC22_RXP0
	RX CH-N1	PIN_AW46	ETHC22_RXN0	QSFP3_ETHC22_RXN0
	RX CH-P2	PIN_BA49	ETHC22_RXP1	QSFP3_ETHC22_RXP1
	RX CH-N2	PIN_BA48	ETHC22_RXN1	QSFP3_ETHC22_RXN1
	RX CH-P3	PIN_BA46	ETHC22_RXP2	QSFP3_ETHC22_RXP2
	RX CH-N3	PIN_BA45	ETHC22_RXN2	QSFP3_ETHC22_RXN2
	RX CH-P4	PIN_AW49	ETHC22_RXP3	QSFP3_ETHC22_RXP3
	RX CH-N4	PIN_AW48	ETHC22_RXN3	QSFP3_ETHC22_RXN3
	TX CH-P2	PIN_BA52	ETHC22_TXP0	QSFP3_ETHC22_TXP1
	TX CH-N2	PIN_BA51	ETHC22_TXN0	QSFP3_ETHC22_TXN1
	TX CH-P1	PIN_AW52	ETHC22_TXP1	QSFP3_ETHC22_TXP0

	TX CH-N1	PIN_AW51	ETHC22_TXN1	QSFP3_ETHC22_TXN0
	TX CH-P3	PIN_BB53	ETHC22_TXP2	QSFP3_ETHC22_TXP2
	TX CH-N3	PIN_BB54	ETHC22_TXN2	QSFP3_ETHC22_TXN2
	TX CH-P4	PIN_AY54	ETHC22_TXP3	QSFP3_ETHC22_TXP3
	TX CH-N4	PIN_AY53	ETHC22_TXN3	QSFP3_ETHC22_TXN3
Port53	RX CH-N3	PIN_W45	ETHC27_RXP0	QSFP4_ETHC27_RXN2
	RX CH-P3	PIN_W46	ETHC27_RXN0	QSFP4_ETHC27_RXP2
	RX CH-N4	PIN_W49	ETHC27_RXP1	QSFP4_ETHC27_RXN3
	RX CH-P4	PIN_W48	ETHC27_RXN1	QSFP4_ETHC27_RXP3
	RX CH-P1	PIN_AA45	ETHC27_RXP2	QSFP4_ETHC27_RXP0
	RX CH-N1	PIN_AA46	ETHC27_RXN2	QSFP4_ETHC27_RXN0
	RX CH-N2	PIN_AA49	ETHC27_RXP3	QSFP4_ETHC27_RXN1
	RX CH-P2	PIN_AA48	ETHC27_RXN3	QSFP4_ETHC27_RXP1
	TX CH-P1	PIN_W51	ETHC27_TXP0	QSFP4_ETHC27_TXP0
	TX CH-N1	PIN_W52	ETHC27_TXN0	QSFP4_ETHC27_TXN0
	TX CH-P2	PIN_Y54	ETHC27_TXP1	QSFP4_ETHC27_TXP1
	TX CH-N2	PIN_Y53	ETHC27_TXN1	QSFP4_ETHC27_TXN1
	TX CH-P3	PIN_AA51	ETHC27_TXP2	QSFP4_ETHC27_TXP2
	TX CH-N3	PIN_AA52	ETHC27_TXN2	QSFP4_ETHC27_TXN2
	TX CH-P4	PIN_AB54	ETHC27_TXP3	QSFP4_ETHC27_TXP3
	TX CH-N4	PIN_AB53	ETHC27_TXN3	QSFP4_ETHC27_TXN3
Port54	RX CH-P3	PIN_AE45	ETHC26_RXP0	QSFP5_ETHC26_RXP2
	RX CH-N3	PIN_AE46	ETHC26_RXN0	QSFP5_ETHC26_RXN2
	RX CH-P2	PIN_AE49	ETHC26_RXP1	QSFP5_ETHC26_RXP1
	RX CH-N2	PIN_AE48	ETHC26_RXN1	QSFP5_ETHC26_RXN1
	RX CH-P4	PIN_AC49	ETHC26_RXP2	QSFP5_ETHC26_RXP3
	RX CH-N4	PIN_AC48	ETHC26_RXN2	QSFP5_ETHC26_RXN3
	RX CH-P1	PIN_AC45	ETHC26_RXP3	QSFP5_ETHC26_RXP0
	RX CH-N1	PIN_AC46	ETHC26_RXN3	QSFP5_ETHC26_RXN0
	TX CH-P1	PIN_AF53	ETHC26_TXP0	QSFP5_ETHC26_TXP0
	TX CH-N1	PIN_AF54	ETHC26_TXN0	QSFP5_ETHC26_TXN0
	TX CH-P2	PIN_AE51	ETHC26_TXP1	QSFP5_ETHC26_TXP1
	TX CH-N2	PIN_AE52	ETHC26_TXN1	QSFP5_ETHC26_TXN1
	TX CH-P3	PIN_AD54	ETHC26_TXP2	QSFP5_ETHC26_TXP2
	TX CH-N3	PIN_AD53	ETHC26_TXN2	QSFP5_ETHC26_TXN2
	TX CH-P4	PIN_AC51	ETHC26_TXP3	QSFP5_ETHC26_TXP3
	TX CH-N4	PIN_AC52	ETHC26_TXN3	QSFP5_ETHC26_TXN3
Port55	RX CH-N3	PIN_L45	ETHC29_RXP0	QSFP6_ETHC29_RXN2
	RX CH-P3	PIN_L46	ETHC29_RXN0	QSFP6_ETHC29_RXP2
	RX CH-N4	PIN_L49	ETHC29_RXP1	QSFP6_ETHC29_RXN3
	RX CH-P4	PIN_L48	ETHC29_RXN1	QSFP6_ETHC29_RXP3
	RX CH-P1	PIN_N45	ETHC29_RXP2	QSFP6_ETHC29_RXP0
	RX CH-N1	PIN_N46	ETHC29_RXN2	QSFP6_ETHC29_RXN0
	RX CH-N2	PIN_N49	ETHC29_RXP3	QSFP6_ETHC29_RXN1
	RX CH-P2	PIN_N48	ETHC29_RXN3	QSFP6_ETHC29_RXP1
	TX CH-P1	PIN_L51	ETHC29_TXP0	QSFP6_ETHC29_TXP0
	TX CH-N1	PIN_L52	ETHC29_TXN0	QSFP6_ETHC29_TXN0
	TX CH-P2	PIN_M54	ETHC29_TXP1	QSFP6_ETHC29_TXP1
	TX CH-N2	PIN_M53	ETHC29_TXN1	QSFP6_ETHC29_TXN1
	TX CH-P3	PIN_N51	ETHC29_TXP2	QSFP6_ETHC29_TXP2
	TX CH-N3	PIN_N52	ETHC29_TXN2	QSFP6_ETHC29_TXN2
	TX CH-P4	PIN_P54	ETHC29_TXP3	QSFP6_ETHC29_TXP3
	TX CH-N4	PIN_P53	ETHC29_TXN3	QSFP6_ETHC29_TXN3
Port56	RX CH-P3	PIN_U49	ETHC28_RXP0	QSFP7_ETHC28_RXP2
	RX CH-N3	PIN_U48	ETHC28_RXN0	QSFP7_ETHC28_RXN2
	RX CH-P4	PIN_U45	ETHC28_RXP1	QSFP7_ETHC28_RXP3
	RX CH-N4	PIN_U46	ETHC28_RXN1	QSFP7_ETHC28_RXN3
	RX CH-P1	PIN_R49	ETHC28_RXP2	QSFP7_ETHC28_RXP0
	RX CH-N1	PIN_R48	ETHC28_RXN2	QSFP7_ETHC28_RXN0

	RX CH-P2	PIN_R45	ETHC28_RXP3	QSFP7_ETHC28_RXP1
	RX CH-N2	PIN_R46	ETHC28_RXN3	QSFP7_ETHC28_RXN1
	TX CH-P1	PIN_V54	ETHC28_TXP0	QSFP7_ETHC28_TXP0
	TX CH-N1	PIN_V53	ETHC28_TXN0	QSFP7_ETHC28_TXN0
	TX CH-P2	PIN_U51	ETHC28_TXP1	QSFP7_ETHC28_TXP1
	TX CH-N2	PIN_U52	ETHC28_TXN1	QSFP7_ETHC28_TXN1
	TX CH-P3	PIN_T54	ETHC28_TXP2	QSFP7_ETHC28_TXP2
	TX CH-N3	PIN_T53	ETHC28_TXN2	QSFP7_ETHC28_TXN2
	TX CH-P4	PIN_R51	ETHC28_TXP3	QSFP7_ETHC28_TXP3
	TX CH-N4	PIN_R52	ETHC28_TXN3	QSFP7_ETHC28_TXN3

6.2 PCIE BUS

We use PCIe bus from COM-e to the switch NP8366. PCIe Lane [0:3] is used as PCIe x4.

PCIe clock input of the switch is driven by the PCIe clock from the COM-e module.

6.3 LPC BUS

LPC Bus is designed for managing CPLD and BMC.

6.4 MDI

The LAN interface of the COM Express Module consists of 4 pairs of low voltage differential pair signals designated from 'GBE0_MDI0' (+ and -) to 'GBE0_MDI3' (+ and -) plus additional control signals for link activity indicators. These signals are used to connect to 88E6320 on the main board.

6.5 SATA

One SATA interface is optional to be used for COM-E module external storage. The mSATA connector （CNN74）is located on the main board.

6.6 I2C AND SMBUS

COM-E’s I2C is connected to BMC’s I2C5. SMBus is connected to BMC’s I2C1.

COM-E’s I2C can also be used to update CPLD.

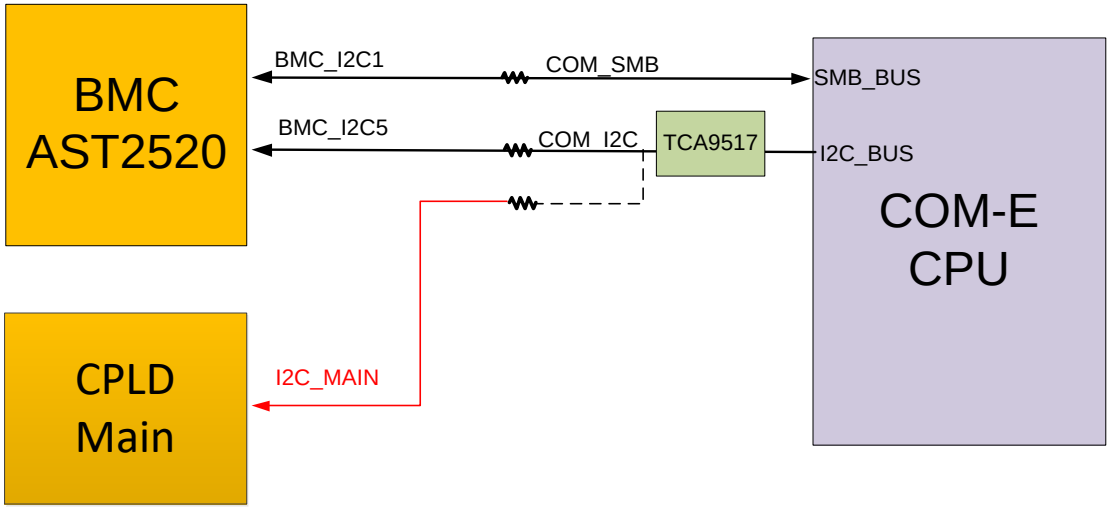


Figure 19: CS6436-56P main I2C

6.7 UART

Both two UART serial ports are connected to CPLD. CPU or BMC can access the CPLD, and decide which port is used as the console port or debug port in the front panel. UART0 is used as the console port by default, and UART1 is used for debug.

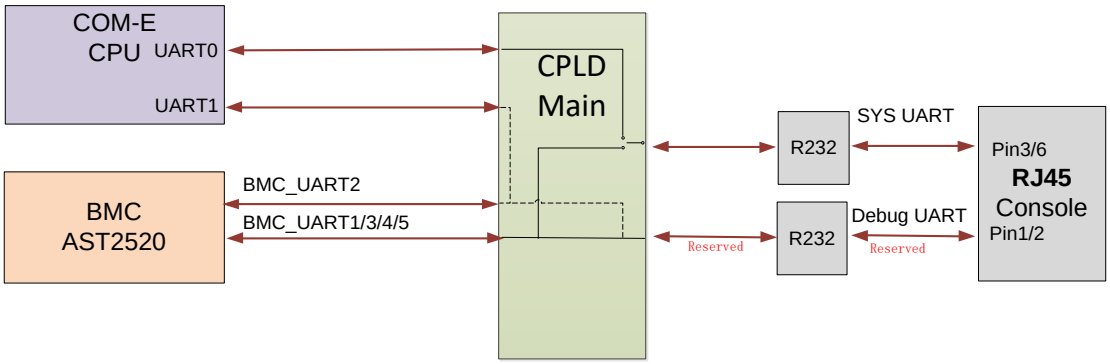


Figure 20: CS6436-56P UART

6.8 USB

USB0+/- is connected to a USB connector of the front panel used as USB2.0.

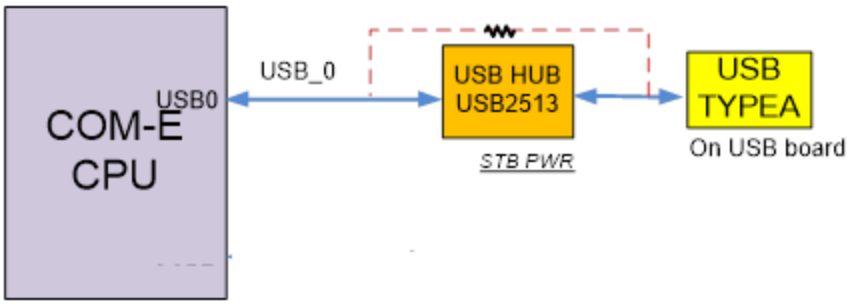


Figure 21: CS6436-56P USB

6.9 SPI

SPI port is used for accessing the SPI flash on the main board, which stores the BIOS file for CPU.

6.10 CPLD

There are 3 CPLDs. The main CPLD is used for RESET/FAN controlling, LED lighting and I2C extender. CPU can access the main CPLD through LPC bus. The other two CPLDs are used as extended GPIOs to connect 56 ports' status and control signals.

One main CPLD's Mfr. Part Number: LCMXO3LF-2100C-5BG256C.

Two extended CPLD's Mfr. Part Number: LCMXO3LF-1300C-5BG256C.

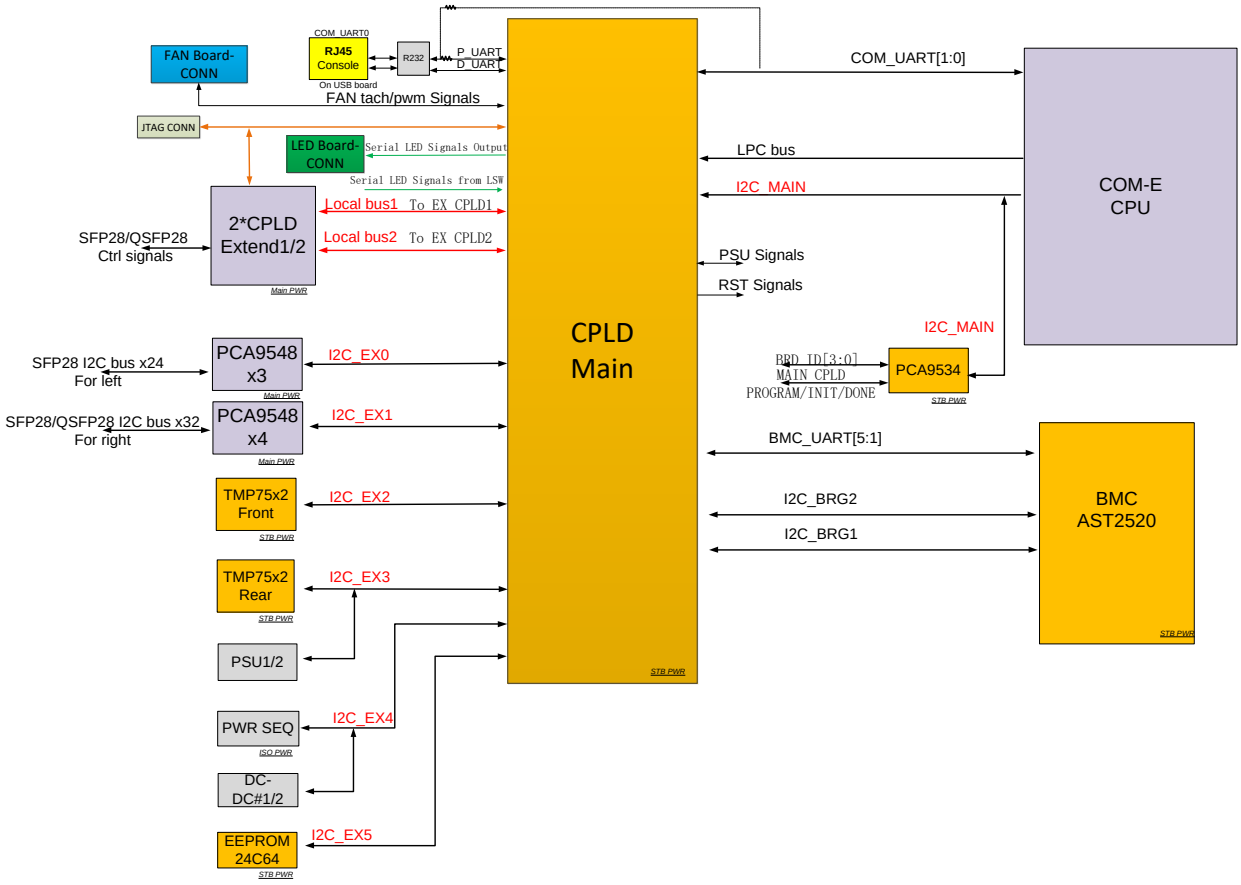


Figure 22: CS6436-56P CPLD

CPLD have two programing and configuration interfaces: 1149.1 JTAG and I2C.

J3 is the JTAG connector, using lattice programing cable to download the file.

Software can use I2C bus to update the CPLD.

6.10.1 I2C BUS EXTENDER

CS6436-56P uses the main CPLD to extend I2C bus. CPU can access the registers, which are used to control I2C write or read operation. The registers are listed in the following table:

Address	Bit	Name	Description
0x80	7-0	reg_bus_sel	select I2C BUS，0x0-0x5
0x81	7-0	reg_device_addr	I2C slave device 7-bit address + R/W# flag
0x83	7-0	reg_byte_count	transaction byte count
0x84	7-0	reg_command	command register
0x85	7-0	reg_status	status register
0x86	7-0	reg_data_rx1	Data read from I2C（read operation）
0x87	7-0	reg_data_rx2	Data read from I2C（read operation）
0x88	7-0	reg_data_rx3	Data read from I2C（read operation）

0x89	7-0	reg_data_rx4	Data read from I2C（read operation）
0x8a	7-0	reg_data_tx1	Data transfer to I2C（write operation）
0x8b	7-0	reg_data_tx2	Data transfer to I2C（write operation）
0x8c	7-0	reg_data_tx3	Data transfer to I2C（write operation）
0x8d	7-0	reg_data_tx4	Data transfer to I2C（write operation）

I2C address map:

bus select	chips	slave device address（7bit））	
CPLD_I2C0	PCA9548(U18)	0x71	port1-8 slave address = 0x50/51
	PCA9548(U19)	0x72	port9-16 I2C slave address = 0x50/51
	PCA9548(U21)	0x73	port17-24 I2C slave address = 0x50/51
	PCA9548(U20)	0x74	port25-32 I2C slave address = 0x50/51
CPLD_I2C1	PCA9548(U22)	0x75	port33-40 I2C slave address = 0x50/51
	PCA9548(U23)	0x76	port41-48 I2C slave address = 0x50/51
	PCA9548(U24)	0x77	port49-56 I2C slave address = 0x50/51
CPLD_I2C2	TMP75(U13) front	0x48	
	TMP75(U12) front	0x49	
CPLD_I2C3	TMP75(U15) rear	0x4a	
	TMP75(U16) rear	0x4b	
	PSU0	EEPROM = 0x52 MCU = 0x5a	
	PSU1	EEPROM = 0x53 MCU = 0x5b	
CPLD_I2C4	P1014A(U39)	0x30	voltage monitor
CPLD_I2C5	EEPROM(U9)	0x57	

6.10.2 RESET OPERATION

All chips in the system can be reset separately. When the CPU sends out WDT signal, the main CPLD will generate reset signal to CPU. The address of reset registers range from 0x10 to 0x12.

6.10.3 LED CONTROLLER

The front system LEDs and rear FAN LEDs are controlled by the LED registers. They range from 0x30 to 0x31.

6.10.4 FAN CONTROLLER

There are 5 fan modules in the system. The main CPLD can enable fan modules, set and read fan speed. The addresses of fan register range from 0x40 to 0x4c.

6.10.5 UART SELECTION

CPU's two UARTs and BMC's five UARTs converge to the main CPLD. The default system UART is CPU_UART0. The debug UART can be set by the UART selection register, which address is 0x50.

6.10.6 STATUS INFORMATION

PSU/USB/SFP28/QSFP28 status can be accessed through the registers from 0x60 to 0x7c.

6.11 BMC

BMC module of CS6436-56P is optional. The LPC bus works in the slave mode, designed for BMC functions (I/O and memory or firmware read/write cycles). The SPI bus can update the BIOS of the system, by writing the SPI flash on the main board.

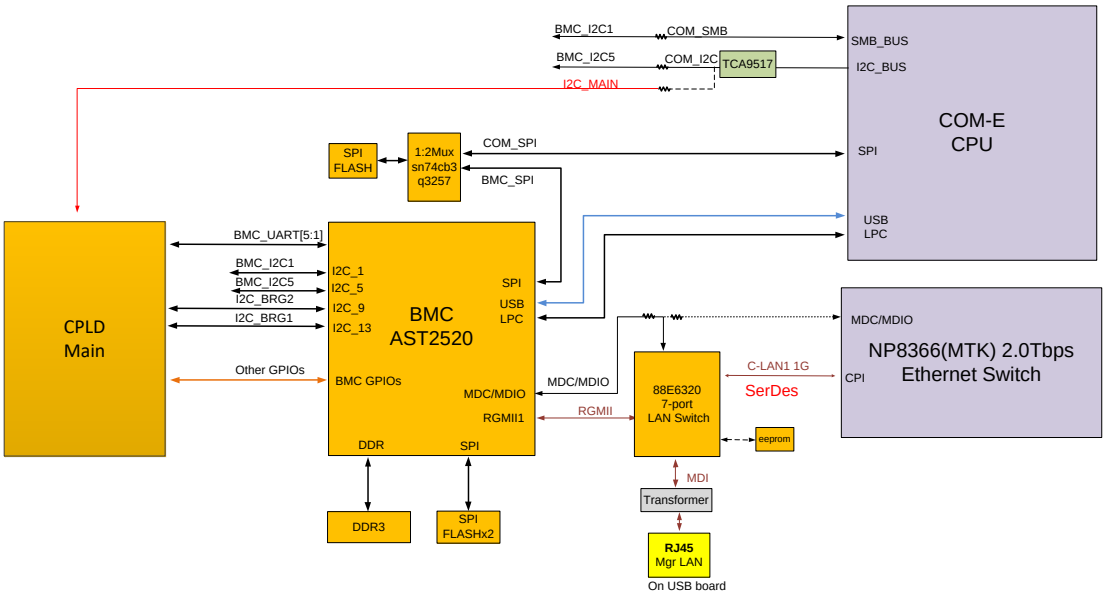


Figure 23: CS6436-56P BMC

6.12 CLOCK DIAGRAM

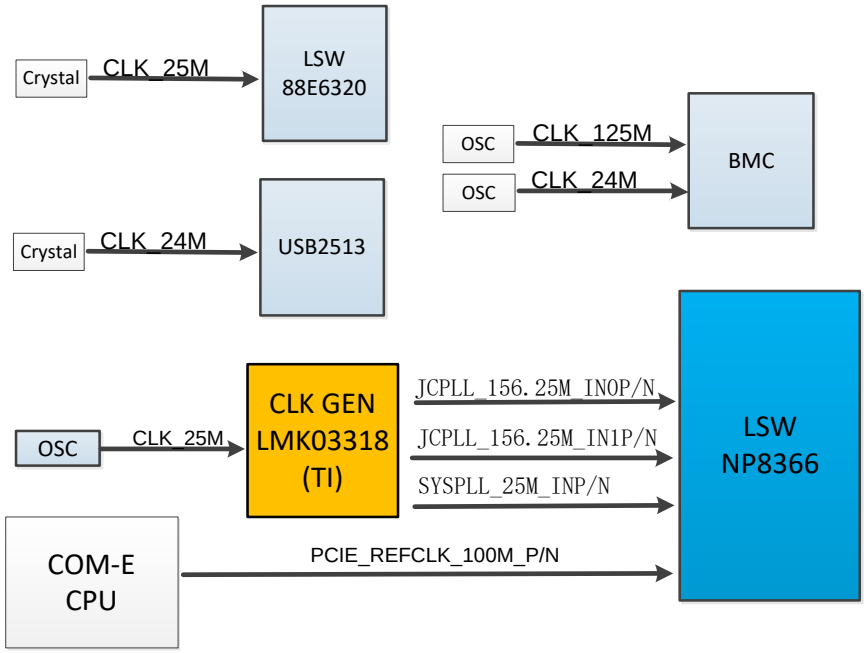


Figure 24: CS6436-56P clock tree

6.13 LED

Figure 25: CS6436-56P front LED

6.13.1 SYSTEM LED DEFINITION

LED(from left to right)	Color	Description
P1	Red	PSU1 Error/Failure/Bad
	Green	PSU1 Good
	Off	PSU1 Not present
P2	Red	PSU2 Error/Failure/Bad
	Green	PSU2 Good
	Off	PSU2 Not present
F	Red	FAN Error/Failure/Bad
	Green	FAN Good
S	Red	Critical system failure detected (overheat, >1 FANs failed, CPU crash, etc.)
	Green	System is initialized and operating in good condition
	Amber	Major system failure detected (1xFAN failed; 1xPSU failed, etc.)
	Blinking Amber	Updating system
	Blinking Green	System is booting
L	Blinking Green	Reserved
	Green	Reserved
	Red	Reserved
	Off	Reserved
M	Green	Management Port link up,100/1000M
	Blinking Green	Management Port ,TX/RX Activity,
	Off	Port down

6.13.2 PORT LED DEFINITION

Location	LED Number	Color	Description
LED port1~48 （25Gbps）	LED	Green	Link up with 25G speed
		Blinking Green	TX/RX Activity, with 25G speed
		Amber	Link up with 10G speed
		Blinking Amber	TX/RX Activity, with 10G speed

		Off	link down
		Red	Fault
LED port49~56 （100Gbps）	LED1	Green	Link up with 100G speed
		Blinking Green	TX/RX Activity, with 100G speed
		Off	link down
	LED2/LED3/LED4	Off	not use
LED port49~56 （40Gbps）	LED1	Amber	Link up with 40G speed
		Blinking Amber	TX/RX Activity, with 40G speed
		Off	link down
	LED2/LED3/LED4	Off	not use
LED port49~56 （4x25Gbps）	LED1/LED2 /LED3/LED4	Green	Link up with 25G speed
		Blinking Green	TX/RX Activity, with 25G speed
		Off	link down
		Red	Fault
LED port49~56 （4x10Gbps）	LED1/LED2 /LED3/LED4	Amber	Link up with 10G speed
		Blinking Amber	TX/RX Activity, with 10G speed
		Off	link down
		Red	Fault

Note：Only two ports in ports through 49 to 56 can be set to 4 x 25G or 4 x10G mode.

6.13.3 FAN MODULE LED DEFINITION (REAR, PER FAN MODULE)

LED	Color	Description
LED	Red	Error/Failure/Bad
	Green	FAN Good

6.13.4 PSU LED (REAR)

LED	Color	Description
LED	Off	No power to PSU
	Green	12V Output ON and OK
	1Hz Blinking Green	only 12VSB or PSU in cold redundant state
	Amber/ Blinking Amber	Error/Failure/Bad

6.14 ON BOARD POWER DESIGN

NP8366 0.9V core voltage 90A rail:

- IR3581 + 4x IR3555 four phase design
- Power stage IR3555

- Inductor

CS6436-56P 3.3V main power 50A rail:

- IR3581 + 3x IR3555 three phase design
- Power stage IR3555
- Inductor

Voltage rails with small current can use MPQ8363 (20A), MP1495 (3A).

6.14.1 POWER BUDGET

The power budget of CS6436-56P with 12V DC input is estimate to be 363W, assuming all 48 SFP28 ports have 1.5W 25G optic module mounted, and 8 QSFP28 ports have 3.5W 100G optic module mounted. The following shows the summary of estimated power.

	Quantity	Unit Power (W)	Power (W)
COM-e	1	33	33
NP8366	1	92	92
SFP28	48	1.5	72
QSFP28	8	3.5	28
Fan tray	5	21.6	108
Others	1	30	30
Total Power			363

6.14.2 VOLTAGE RAIL CONTROL AND MONITOR

In order to ensure proper operation of all power rails at all times, CS6436 need to support the following voltage rail control and monitor functions

- The power up and power sequence of all voltage rails need to be controlled in sub-ms delay.
- All voltage rails need to be closely monitored; under-voltage threshold and over-voltage threshold need to be specified by design and can be adjustable by software if needed.
- All voltage rails need to be measured in reasonable accuracy.

Lattice semiconductor programmable power controller PWR1014a is recommended to implement all these three functions. Power control and status information can be accessed via I2C interface.

P1014A pin	Power rail	Voltage
VMON1	12V_MON	12V
VMON2	IR_5V	5V
VMON3	STB_5V	5V
VMON4	STB_3V3	3.3V
VMON5	STB_1V35	1.35V
VMON6	STB_1V15	1.15V

VMON7	VDD_0V9	0.9V
VMON8	VDD_1V8	1.8V
VMON9	VDD_3V3	3.3V
VMON10	VDD_1V2	1.2V

6.14.3 POWER SEQUENCER AND MONITOR

We use PWR1014A to control the power sequence. PWR1014A is also used to monitor the voltage rails, and it can be accessed via I2C bus.

All power sequence: 12V → IR_5V→ STB_5V/STB_3V3/STB_1V35/STB_1V5/STB_1V1→STB_1V15→

M_0V9→M_1V8→M_3V3→M_1V2→12V_COMe

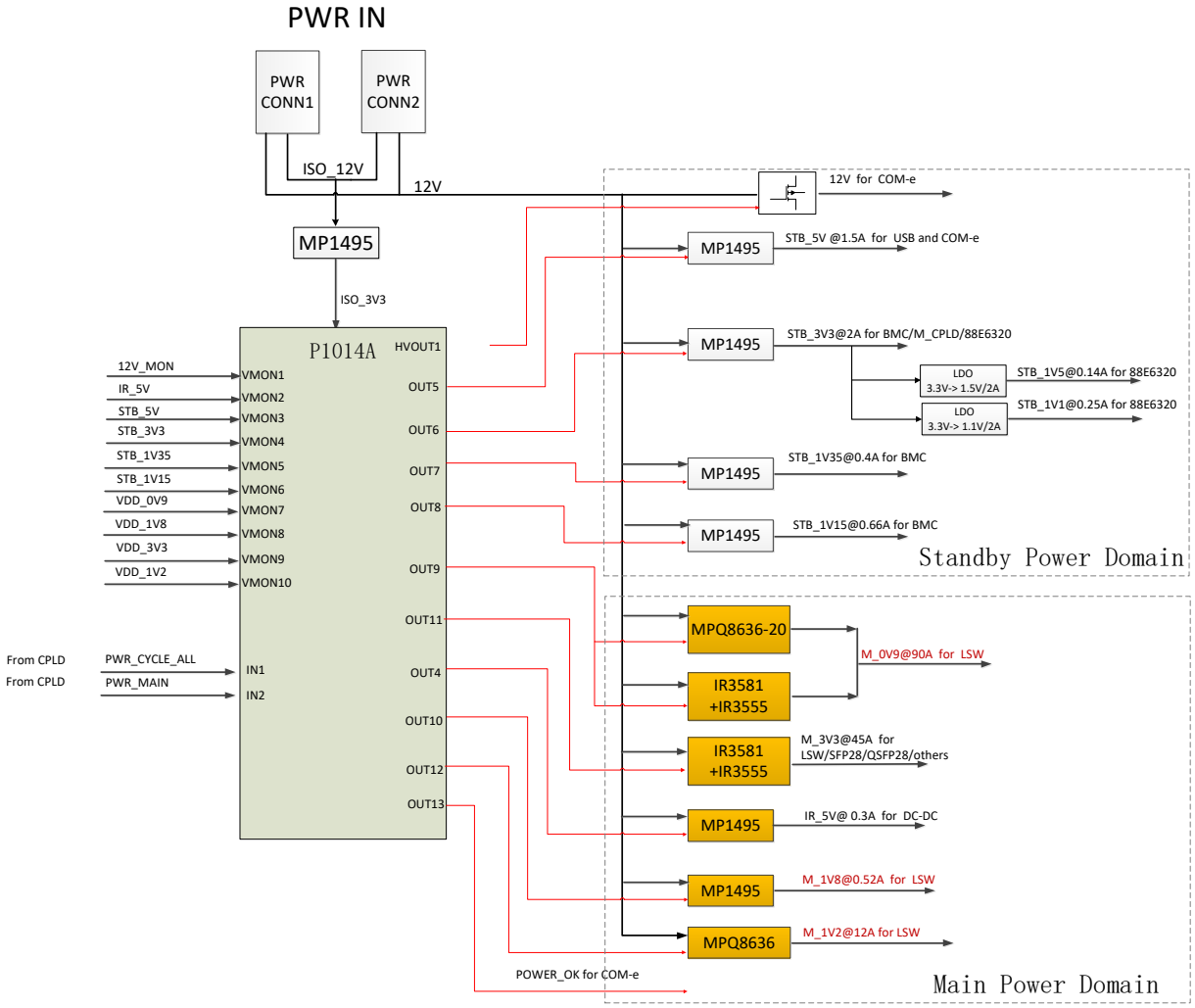


Figure 26: CS6436-56P power tree

6.15 RESET AND PWR CONTROL

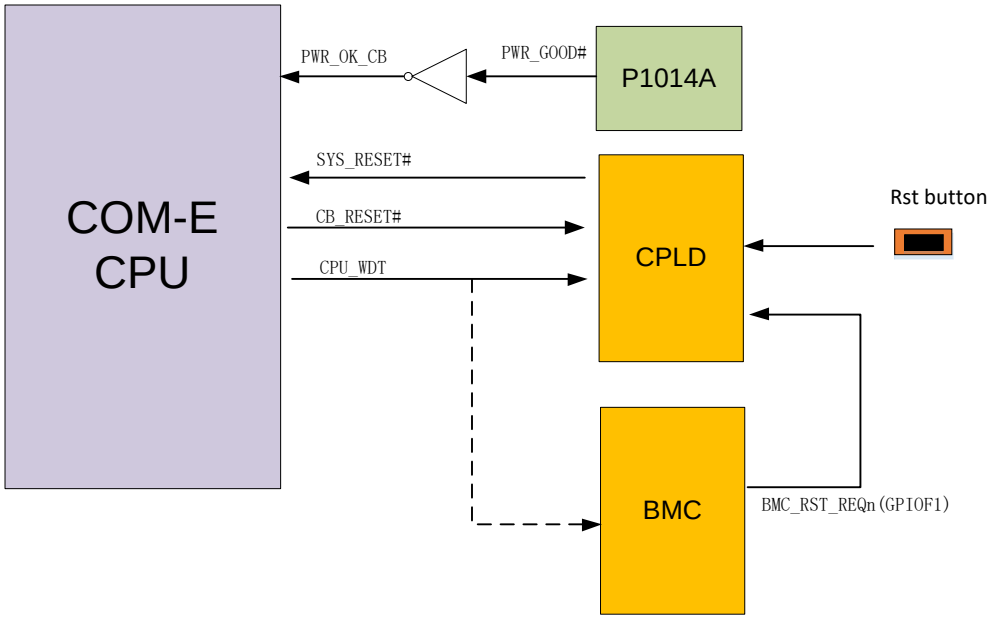


Figure 27: CS6436-56P reset tree

Power OK is from the P1014A on the main board. A high value indicates that the power is good and the module can start its on board power sequencing.

CPU will output WDT to CPLD or BMC, indicating that a watchdog time-out event has occurred. CPLD will output SYS_RESET# to reset CPU, when CPLD receives CPU_WDT. Or BMC tells the CPLD to reset CPU.

7. COM-E MODULE

A COM-e CPU module is used as the control plane CPU in CS6436-56P.

7.1 COM-E DIAGRAM

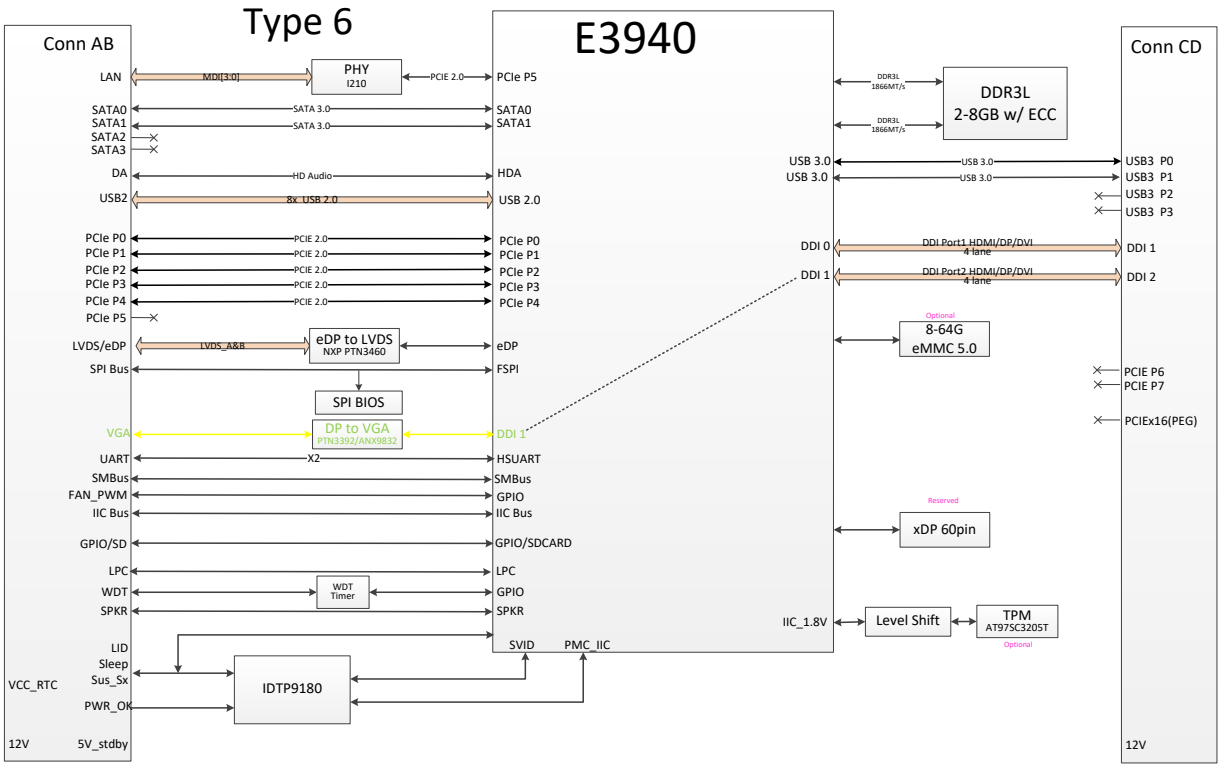


Figure 28: CS6436-56P COM-E diagram

7.2 FEATURE SET

1	Platform	
1-1	PICMG COM.0: Rev 2.1	COM Express® Type 6 Module
1-2	CPU	Intel® Atom™ x5-E3940, 4C, 1.6 / 1.8 GHz, 9.5 W TDP
1-3	Main Memory	Up to 8 GB DDR3L 1600 / 1867 Memory with ECC
1-4	Flash on board	eMMC 5.0 on board flash up to 64 GByte
1-5	BIOS	Phoenix Secure Core UEFI/AMI Aptio5 UEFI BIOS
2	**Interface**	
2-1	SATA	1 x SATA 3.0 6Gb/s
2-2	USB	2 x USB3.0(0,1), 6 x USB2.0(2,3,4,5,6,7)
2-3	Serial	2x serial interface (RX/TX only)
2-4	GPIO	4 x GPI, 4 x GPO
2-5	eMMC	eMMC5.0(8/16/32/64GB optional)
2-6	Ethernet	1x 10/100/1000 MBit Ethernet
6-1	PCI Express	Up to 5 PCIe x1 Gen2; Configurable to x2, x4 (port 0-3)
3	**Power**	The main board supply 12V/max2.5A,5V/max0.5A
4	Dimensions (H x W)	Compact size (95 x 95 mm)

7.3 PIN DEFINITION OF COM-E CONNECTOR

COM-E module uses a type 6 connector which has two parts: row AB and row CD. For CS6436-56P application, row CD has no interface to be connected except 12V power pins and GND pins; interfaces used between COM-E and main board are mainly located on row AB. The following table shows signals of row AB connected to main board, and signals with "*" mean they're not used in CS6436-56P design.

Pin#	A		B	
1	GND(FIXED)	Required	GND(FIXED)	Required
2	GBE0_MDI3-	Required	GBE0_ACT#	Required
3	GBE0_MDI3+	Required	LPC_FRAME#	Required
4	*GBE0_LINK100#	Not required	LPC_AD0	Required
5	*GBE0_LINK1000#	Not required	LPC_AD1	Required
6	GBE0_MDI2-	Required	LPC_AD2	Required
7	GBE0_MDI2+	Required	LPC_AD3	Required
8	GBE0_LINK#	Required	LPC_DRQ0#	Required
9	GBE0_MDI1-	Required	LPC_DRQ1#	Required
10	GBE0_MDI1+	Required	LPC_CLK	Required
11	GND(FIXED)	Required	GND(FIXED)	Required
12	GBE0_MDI0-	Required	PWRBTN#	Pull up
13	GBE0_MDI0+	Required	*SMB_CK	Not required
14	*GBE0_CTREF	Not required	*SMB_DAT	Not required
15	*SUS_S3#	Not required	*SMB_ALERT#	Not required
16	SATA0_TX+	Required	*SATA1_TX+	Not required
17	SATA0_TX-	Required	*SATA1_TX-	Not required
18	*SUS_S4#	Not required	*SUS_STAT#	Not required
19	SATA0_RX+	Required	*SATA1_RX+	Not required
20	SATA0_RX-	Required	*SATA1_RX-	Not required
21	GND(FIXED)	Required	GND(FIXED)	Required
22	*SATA2_TX+	Not required	*SATA3_TX+	Not required
23	*SATA2_TX-	Not required	*SATA3_TX-	Not required
24	*SUS_S5#	Not required	PWR_OK	Required
25	*SATA2_RX+	Not required	*SATA3_RX+	Not required
26	*SATA2_RX-	Not required	*SATA3_RX-	Not required
27	*BATLOW#	Not required	WDT	Required
28	* (S)ATA_ACT#	Not required	*AC/HDA_SDIN2	Not required
29	*AC/HDA_SYNC	Not required	*AC/HDA_SDIN1	Not required
30	*AC/HDA_RST#	Not required	*AC/HDA_SDIN0	Not required
31	GND(FIXED)	Required	GND(FIXED)	Required
32	*AC/HDA_BITCLK	Not required	*SPKR	Not required
33	*AC/HDA_SDOUT	Not required	I2C_CK	Required
34	*BIOS_DIS0#	Not required	I2C_DAT	Required
35	*THRMTRIP#	Not required	*THRM#	Not required
36	*USB6-	Not required	*USB7-	Not required

37	*USB6+	Not required	*USB7+	Not required
38	*USB_6_7_OC#	Not required	*USB_4_5_OC#	Not required
39	*USB4-	Not required	*USB5-	Not required
40	*USB4+	Not required	*USB5+	Not required
41	GND(FIXED)	Required	GND(FIXED)	Required
42	*USB2-	Not required	*USB3-	Not required
43	*USB2+	Not required	*USB3+	Not required
44	*USB_2_3_OC#	Not required	*USB_0_1_OC#	Not required
45	USB0-	Required	*USB1-	Not required
46	USB0+	Required	*USB1+	Not required
47	*VCC_RTC	Not required	*EXCD1_PERST#	Not required
48	*EXCD0_PERST#	Not required	*EXCD1_CPPE#	Not required
49	*EXCD0_CPPE#	Not required	SYS_RESET#	Required
50	LPC_SERIRQ	Required	CB_RESET#	Required
51	GND(FIXED)	Required	GND(FIXED)	Required
52	*PCIE_TX5+	Not required	*PCIE_RX5+	Not required
53	*PCIE_TX5-	Not required	*PCIE_RX5-	Not required
54	GPI0	Required	GPO1	Required
55	PCIE_TX4+	Required	PCIE_RX4+	Required
56	PCIE_TX4-	Required	PCIE_RX4-	Required
57	GND	Required	GPO2	Required
58	PCIE_TX3+	Required	PCIE_RX3+	Required
59	PCIE_TX3-	Required	PCIE_RX3-	Required
60	GND(FIXED)	Required	GND(FIXED)	Required
61	PCIE_TX2+	Required	PCIE_RX2+	Required
62	PCIE_TX2-	Required	PCIE_RX2-	Required
63	GPI1	Required	GPO3	Required
64	PCIE_TX1+	Required	PCIE_RX1+	Required
65	PCIE_TX1-	Required	PCIE_RX1-	Required
66	GND	Required	*WAKE0#	Not required
67	GPI2	Required	*WAKE1#	Not required
68	PCIE_TX0+	Required	PCIE_RX0+	Required
69	PCIE_TX0-	Required	PCIE_RX0-	Required
70	GND(FIXED)	Required	GND(FIXED)	Required
71	*LVDS_A0+	Not required	*LVDS_B0+	Not required
72	*LVDS_A0-	Not required	*LVDS_B0-	Not required
73	*LVDS_A1+	Not required	*LVDS_B1+	Not required
74	*LVDS_A1-	Not required	*LVDS_B1-	Not required
75	*LVDS_A2+	Not required	*LVDS_B2+	Not required
76	*LVDS_A2-	Not required	*LVDS_B2-	Not required
77	*LVDS_VDD_EN	Not required	*LVDS_B3+	Not required
78	*LVDS_A3+	Not required	*LVDS_B3-	Not required
79	*LVDS_A3-	Not required	*LVDS_BKLT_EN	Not required
80	GND(FIXED)	Required	GND(FIXED)	Required
81	*LVDS_A_CK+	Not required	*LVDS_B_CK+	Not required
82	*LVDS_A_CK-	Not required	*LVDS_B_CK-	Not required

83	*LVDS_I2C_CK	Not required	*LVDS_BKLT_CTRL	Not required
84	*LVDS_I2C_DAT	Not required	VCC_5V_SBY	Required
85	GPI3	Required	VCC_5V_SBY	Required
86	*RSVD	Not required	VCC_5V_SBY	Required
87	*eDP_HPD	Not required	VCC_5V_SBY	Required
88	*PCIE_CLK_REF+	Not required	*BIOS_DIS1#	Not required
89	*PCIE_CLK_REF-	Not required	*VGA_RED	Not required
90	GND(FIXED)	Required	GND(FIXED)	Required
91	SPI_POWER	Required	*VGA_GRN	Not required
92	SPI_MISO	Required	*VGA_BLU	Not required
93	GPO0	Required	*VGA_HSYNC	Not required
94	SPI_CLK	Required	*VGA_VSYNC	Not required
95	SPI_MOSI	Required	*VGA_I2C_CK	Not required
96	*TPM_PP	Not required	*VGA_I2C_DAT	Not required
97	*TYPE10#	Not required	SPI_CS#	Required
98	SER0_TX	Required	*RSVD	Not required
99	SER0_RX	Required	*RSVD	Not required
100	GND(FIXED)	Required	GND(FIXED)	Required
101	SER1_TX	Required	*FAN_PWMOUT	Not required
102	SER1_RX	Required	*FAN_TACHIN	Not required
103	*LID#	Not required	*SLEEP#	Not required
104	VCC_12V	Required	VCC_12V	Required
105	VCC_12V	Required	VCC_12V	Required
106	VCC_12V	Required	VCC_12V	Required
107	VCC_12V	Required	VCC_12V	Required
108	VCC_12V	Required	VCC_12V	Required
109	VCC_12V	Required	VCC_12V	Required
110	GND(FIXED)	Required	GND(FIXED)	Required

8. FAN BOARD

CS6436-56P provides five fan slots, support 4+1 redundant. We use one fan board to provide the power supply and control to fan modules.

The following shows the connectors between the main board and the fan board. The control signals are connected to CPLD. The speed of fans can be modified by CPU, according to the thermal requirement.

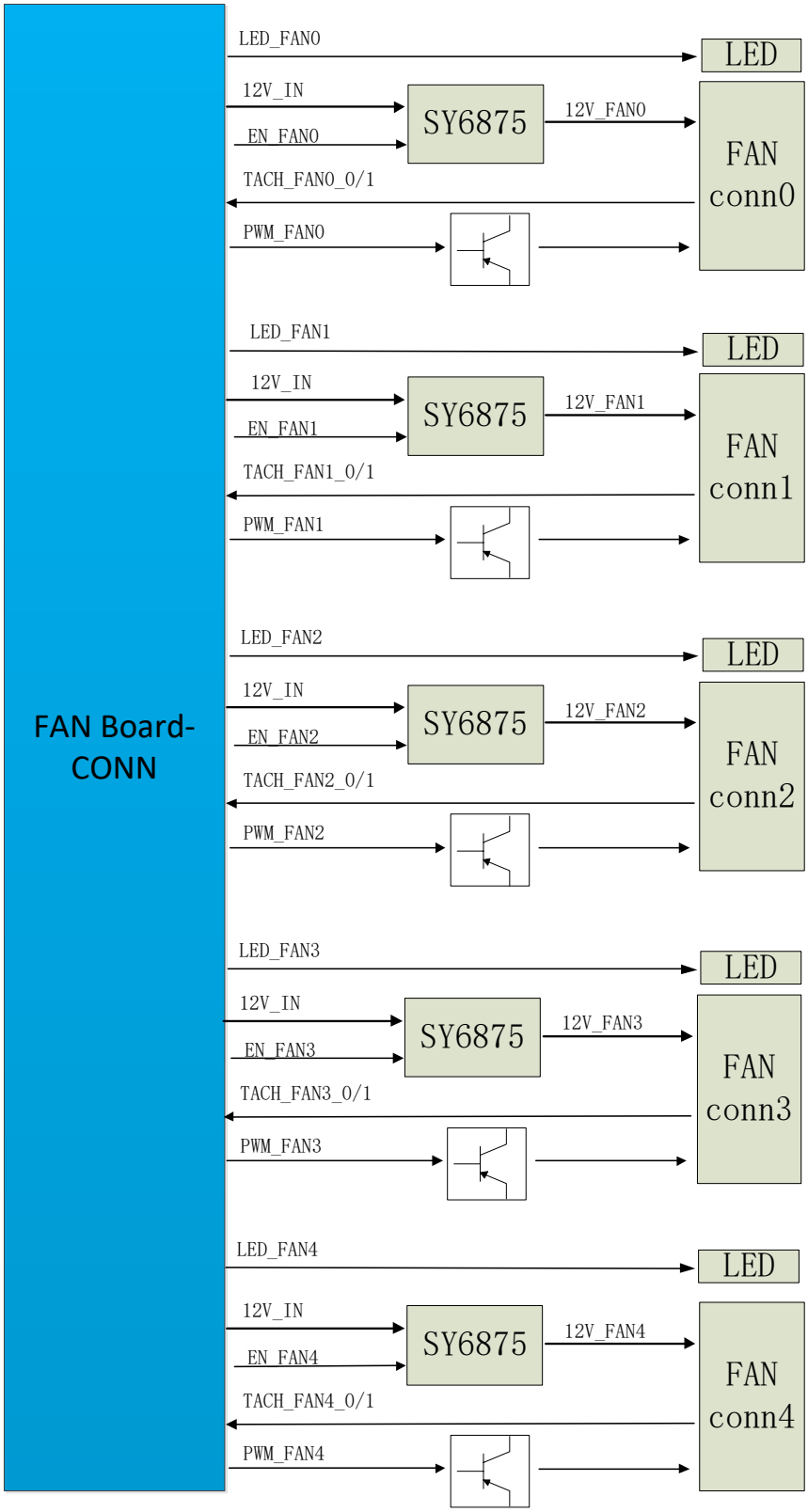


Figure 29: CS6436-56P FAN board diagram

FAN Board CONN pin definition

CNN71 for Fan Board	Pin Net Name	Description
1/2	REVERSAL_FLAG_FAN0 / FAN4	Fan0/4 Direction Signals
3/5	TACH_FAN0_0 /1	Fan0 Speed Signals
4/6	LED_R_REAR_FAN4/ LED_G_REAR_FAN4	Fan4 LED Signals
7	PWM_FAN0	Fan0 Speed Control Signal
8	EN_FAN4	Fan4 Enable Signal
9	EN_FAN0	Fan0 Enable Signal
10	PWM_FAN4	Fan4 Speed Control Signal
11/13	LED_G_REAR_FAN0 / LED_R_REAR_FAN0	Fan0 LED Signals
12/14	TACH_FAN4_1/0	Fan4 Speed Signals
15/16	REVERSAL_FLAG_FAN1 / FAN3	FAN1/3 Direction Signals
17/19	TACH_FAN1_0/1	Fan1 Speed Signals
18/20	LED_R_REAR_FAN3 / LED_G_REAR_FAN3	Fan3 LED Signals
21	PWM_FAN1	Fan1 Speed Control Signal
22	EN_FAN3	Fan3 Enable Signal
23	EN_FAN1	Fan1 Enable Signal
24	PWM_FAN3	Fan3 Speed Control Signal
25/27	LED_G_REAR_FAN1 / LED_R_REAR_FAN1	Fan1 LED Signals
26/28	TACH_FAN3_1/0	Fan3 Speed Signals
29	REVERSAL_FLAG_FAN2	Fan2 Direction Signal
31/33	TACH_FAN2_0/1	Fan2 Speed Signals
32/34	LED_R_REAR_FAN2 / LED_G_REAR_FAN2	Fan2 LED Signals
35	PWM_FAN2	Fan4 Speed Control Signal
36	EN_FAN2	Fan2 Enable Signal
30/37/38	GND	GND
39/40	VDD_3V3_STB	PWR
CNN67 for Fan Board	Pin Net Name	Description
1/2/3	GND	GND
4/5/6	VDD_12V	PWR

9. LED AND USB BOARD

CS6436-56P has one LED daughter-board and one USB daughter-board, which are connected to the main board through the cables.

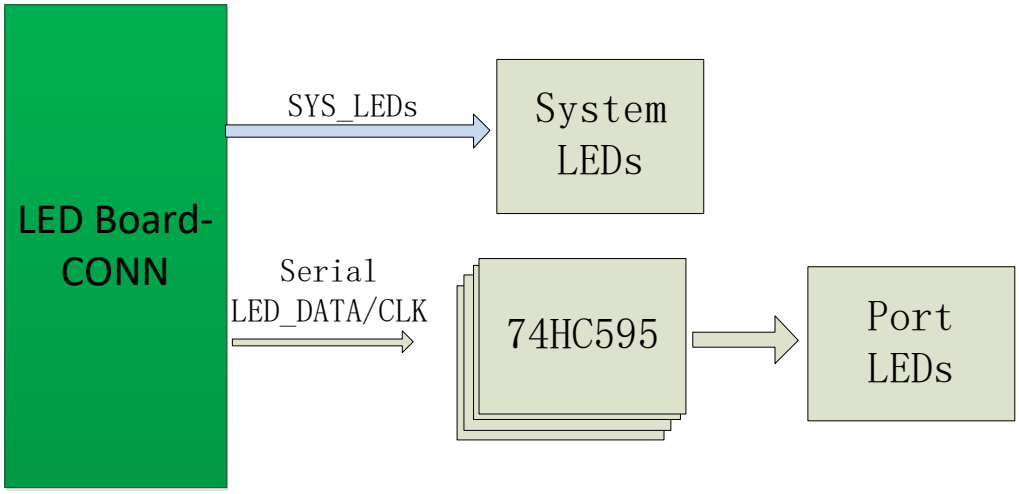


Figure 30: CS6436-56P LED board diagram

The connector signals are defined as the following tables

CNN71 for LED Board	Pin Net Name	Description
1/2	LED_G_MGMT/ LED_R_MGMT	System M dual-color LED
3/4	LED_G_LOCATION/ LED_R_LOCATION	System L dual-color LED
5/6	LED_G_SYS/LED_R_SYS	System S dual-color LED
7/8	LED_G_FAN/LED_R_FAN	System F dual-color LED
9/10	LED_G_PSU1/LED_R_PSU1	System P2 dual-color LED
11/12	LED_G_PSU0/LED_R_PSU0	System P1 dual-color LED
13/14	GND	GND
15	LED_CLK_QSFP28	Serial LED signals for 8 x 100G ports
16	LED_STB_QSFP28	
17	LED_OE_N_QSFP28	
18	LED_DATA_QSFP28	
19/20	GND	GND
21	LED_CLK_SFP28	Serial LED signals for 48 x 25G ports
22	LED_STB_SFP28	
23	LED_OE_N_SFP28	
24	LED_DATA_SFP28	
25-32	GND	GND
33-40	VDD_3V3	PWR

CNN70 for USB Board	Pin Net Name	Description
1	5V_USB	PWR
2	GND	GND
3/4	USB_DN/USB_DP	USB Signals
5/6	GND	GND
7/8	DB_TXD/DB_RXD	Debug RS232
9/10	SYS_TXD/SYS_RXD	System RS232
11/12	NC	Not used
13/14	GE_MXI_P0/N0	100/1000M Management Signals
15/16	GE_MXI_P1/N1	
17/18	GE_MXI_P2/N2	
19/20	GE_MXI_P3/N3	

10. PCB

10.1 MAIN BOARD PCB

The main board size is 428mm*255mm.

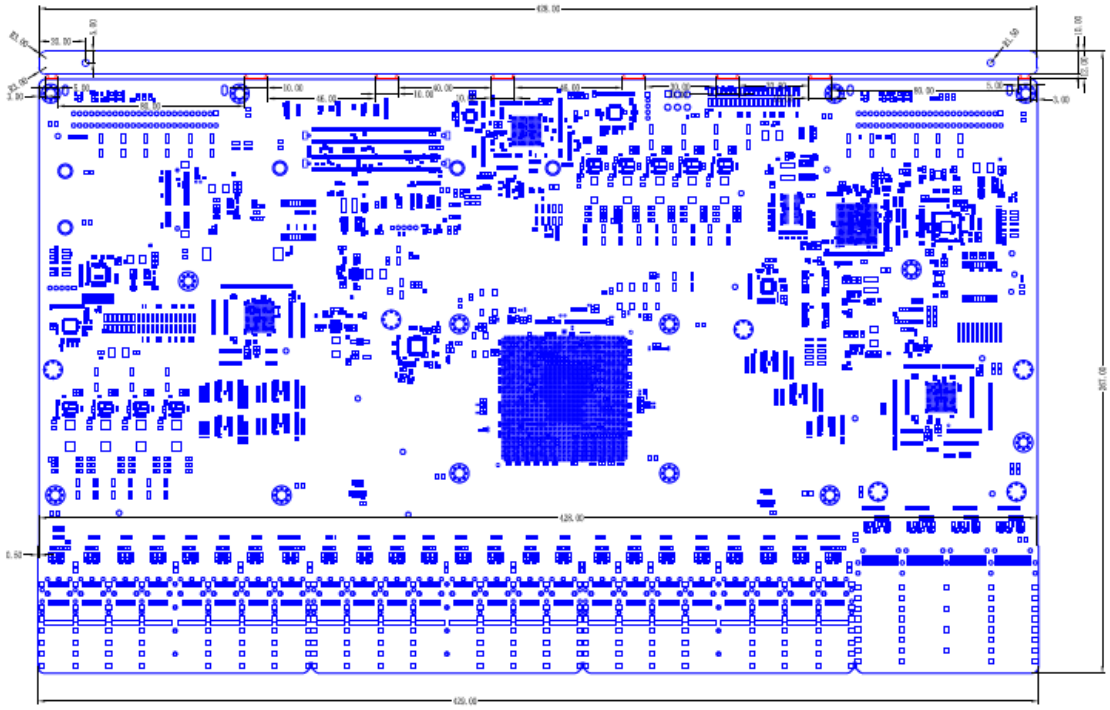


Figure 31: CS6436-56P main board PCB size

PCB material is M6G, the thickness is 3.2mm, and the stack-up of 18-layer is shown as the following table.

Layer Index	Stack up Buildup	PP Name And RC	Dielectric Thickness(Mil/mm)	DK	Finish Cu Thk(oz)	Material Family
L1	Foil(HTE)				1oz	
	PP	PP(1078)RC68	3.282(0.083)	3.10		R5775(G)
L2 L3	Core(HVLP/HVLP)	1*3313	3.937(0.100)	3.30	0.5oz 0.5oz	R5775(G)
	PP PP	PP(1078)RC68 PP(2116)RC54	7.648(0.194)	3.28		R5775(G) R5775(G)
L4 L5	Core(HVLP/HVLP)	1*3313	3.937(0.100)	3.30	0.5oz 0.5oz	R5775(G)
	PP	PP(1078)RC68	7.630(0.194)	3.28		R5775(G)

	PP	PP(2116)RC54				R5775(G)
L6 L7	Core(HVLP/HVLP)	1*3313	3.937(0.100)	3.30	0.5oz 0.5oz	R5775(G)
	PP PP	PP(1078)RC68 PP(2116)RC54	7.748(0.197)	3.28		R5775(G) R5775(G)
L8 L9	Core(RTF/RTF)	1*3313	3.937(0.100)	3.30	0.5oz 2oz	R5775(G)
	PP PP PP PP PP	PP(2116)RC54 PP(2116)RC54 PP(2116)RC54 PP(2116)RC54 PP(2116)RC54	22.304(0.567)	3.40		R5775(G) R5775(G) R5775(G) R5775(G) R5775(G)
L10 L11	Core(RTF/RTF)	1*3313	3.937(0.100)	3.30	2oz 0.5oz	R5775(G)
	PP PP	PP(2116)RC54 PP(1078)RC68	7.659(0.195)	3.28		R5775(G) R5775(G)
L12 L13	Core(HVLP/HVLP)	1*3313	3.937(0.100)	3.30	0.5oz 0.5oz	R5775(G)
	PP PP	PP(2116)RC54 PP(1078)RC68	7.600(0.193)	3.28		R5775(G) R5775(G)
L14 L15	Core(HVLP/HVLP)	1*3313	3.937(0.100)	3.30	0.5oz 0.5oz	R5775(G)
	PP PP	PP(2116)RC54 PP(1078)RC68	7.630(0.194)	3.28		R5775(G) R5775(G)
L16 L17	Core(HVLP/HVLP)	1*3313	3.937(0.100)	3.30	0.5oz 0.5oz	R5775(G)
	PP	PP(1078)RC68	3.287(0.084)	3.10		R5775(G)
L18	Foil(HTE)				1oz	

10.2 FAN BOARD PCB

The fan board size is 241mm*63.8mm. The PCB has 4 layers, and the thickness is 2.4mm.

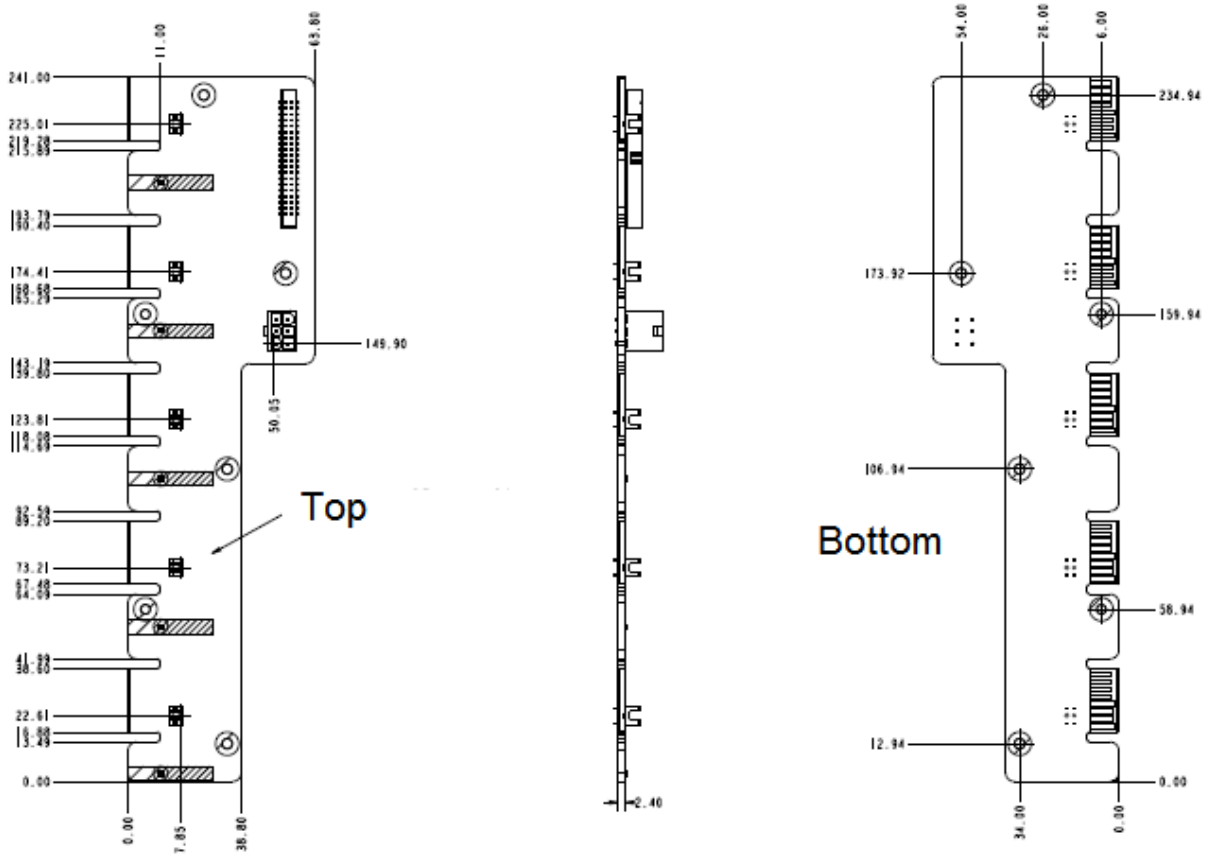


Figure 32: CS6436-56P fan board PCB size

10.3 LED BOARD PCB

The LED board size is 347mm*86.5mm. The PCB has 4 layers, and the thickness is 2.0mm.

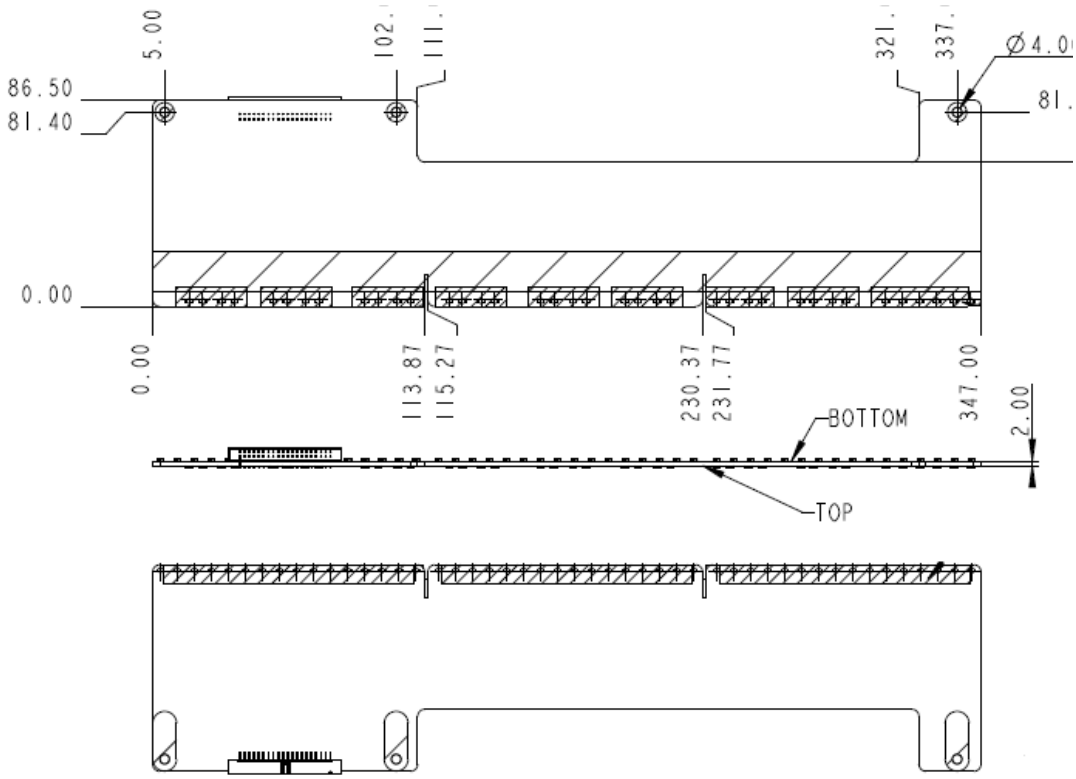


Figure 33: CS6436-56P LED board PCB size

10.4 USB BOARD PCB

The USB board size is 88.25mm*77.3mm. The PCB has 4 layers, and the thickness is 1.6mm.

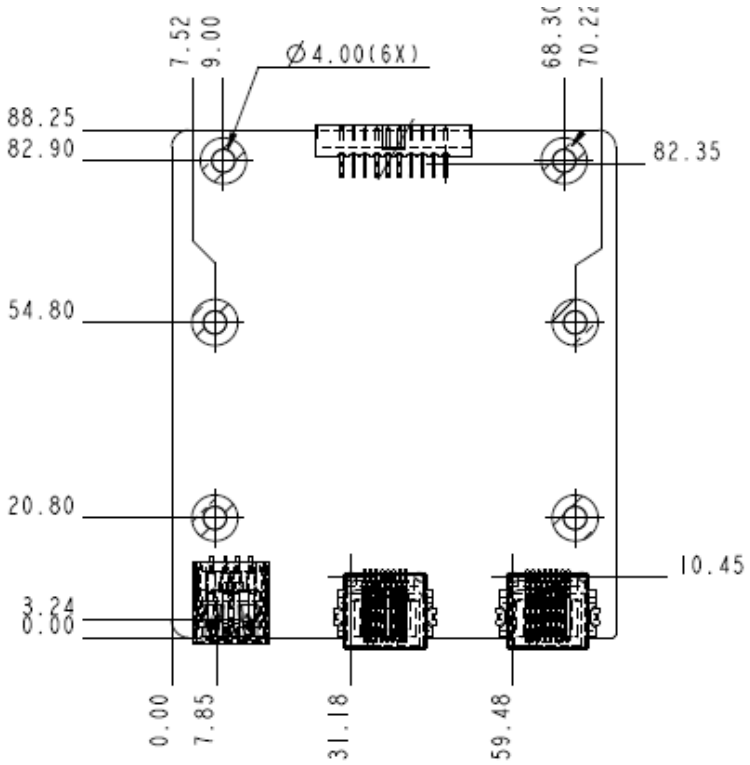


Figure 34: CS6436-56P USB board PCB size

11. Environmental/Agency Certifications

11.1 Environmental

- 0 to 40 °C standard operating range
- -40 to 70 °C storage
- Humidity 5% to 95% non-condensing
- Vibration –ETSI EN 300 019-2-3, IEC 60068-2-64
- Shock –ETSI EN 300 019-2-3, IEC 60068-2-27
- Acoustic Noise Level – Under 65dB in 25 °C

11.2 Safety

The following safety item are planned to be certificated

- UL/ Canada
- CB (Issued by TUV/RH)
- China CCC

11.3 Electromagnetic Compatibility

The following EMC related item are planned to be certificated.

- CE

- EN55022 Class A
- EN55024
- EN61000-3-2
- EN61000-3-3
- FCC Title 47, Part 15, Subpart B Class A
- VCCI Class A
- CCC

11.4 ROHS (6/6) REQUIREMENT

Restriction of Hazardous Substances (6/6): Compliance with Environmental procedure 020499-00, primarily focused on Restriction of Hazardous Substances (ROHS Directive 2002/95/EC) and Waste Electrical and Electronic Equipment (WEEE Directive 2002/96/EC).

12. CS6436 FIRMWARE SUPPORT

The CS6436-56P supports a base software package composed of the following components:

12.1 BIOS

The CS6436-56P supports Phoenix Secure Core UEFI/AMI Aptio5 UEFI BIOS.

12.2 ONIE

See https://github.com/opencomputeproject/onie/tree/master/machine/cig/cig_cs6436_56p

12.3 SONIC

See https://github.com/Azure/sonic-buildimage/tree/master/device/cig

12.4 OPEN NETWORK LINUX

See http://opennetlinux.org/ for latest supported version