OPEN Compute Project

STORDIS Advanced Programmable Switch™ BF6064X-T

Hardware Design Specification

V0.5

Contents

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Reference Documents

1. 10k-AS1-002EA-d.pdf, 10k Device Family Switch Architecture Specification

https://support.barefootnetworks.com/hc/en-us

2. Intel® Xeon® Processor D-1500 Product Family. The documents connect, please contact with Intel Corporation

https://www-ssl.intel.com/content/www/us/en/secure/design/confidential/infodesk/ibp/document-library.html

3. Lattice LCMXO3LF-4300C-5BG400C Programmer and Deployment Tool

http://www.latticesemi.com/Products/DesignSoftwareAndIP/ProgrammingAndConfigurationSw/Programmer.aspx

4. ALTERA Cyclone IV handbook

https://www.altera.com/literature/hb/cyclone-iv/cyclone4-handbook.pdf

5. Intel® Ethernet Controller I210 Data Sheet, Single-Chip 10/100/1000Base-T Gigabit Ethernet Transceiver, Rev.3.0, March, 2017, Intel Corporation

https://www.intel.com/content/www/us/en/embedded/products/networking/ethernet-controller-i210-i211-family- documentation.html

6. FAN controller - Multiple RPM-Based PWM Fan Controller for Five Fans

http://ww1.microchip.com/downloads/en/DeviceDoc/2305.pdf

7. TI TMP75 thermal sensor

http://focus.ti.com/lit/ds/symlink/tmp175.pdf

8. MACRONIX MX25L12835FM2I-10G SPI-Flash 16MB

http://www.macronix.com/en-us/Product/Pages/ProductDetail.aspx?PartNo=MX25L12835F

Version History

Rev	Date	Description	Page
0.1	Nov, 2017	Draft	
0.2	Feb, 2018	1. Update SPEC for EVT1 build 2. Add BMC function, update Section 7.1 I2C 3. Modify Section 3.2.3. Tofino SERDES Configuration.	
0.3	Mar, 2018	1. Modify Section 2.8.1. Correct CPLD vendor to Lattice.	
0.4	Jul, 2018	1. Update SPEC for DVT build 2. Update Section 2.8.1, add one CPLD for clock module. 3. Add Section 2.9 for TPM introduction. 4. Update Section 3.2.3, add CPU port INFO. 6. Due to change Tofino to B0 chip, modify Section 3.3. VDD Voltage Setting. 7. Update Section 7.1.1 I2C Block diagram. 8. Update Section 7.6 Clock Distribution. 9. Update Section 8 for front panel layout change.	
		1. Update SPEC for DVT2 build 2. Section 1.2: Add 1588 Controller, ZL30363GDG2 and I211. 3. Section 1.3: Update block diagram. 4. Section 2.2: Request one more OOB port. Add one I211 to bridge OOB port and Intel PCIE bus. 5. Section 2.4: Add one CPLD, serves as LPC slave, at LPC bus. 6. Section 2.5: Add UART1 connects to 1588 Controller. 7. Section 3.2.3: Update Tofino SERDES Port mapping, add two 10G lanes (ETH64 lane2/3) connects to 1588 Controller.	

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1. STORDIS BF6064X-T Overview

The STORDIS BF6064X-T is a high performance, high density next generation switch with target application for Data Center network. It has Sixty-Five 100GbE QSFP28 ports which support 100GE applications in a compact 2RU form factor.

In addition to the rich bandwidth, the STORDIS BF6064X-T provides comprehensive capability on layer 2 and layer 3 features, including SNMP, Spanning Tree, VLAN, QinQ, Trunk, QoS, RIP, OSPF, IGMP, DVMRP, PIM-DM, PIM-SM, Access Control, etc. This product which aims for Data Center network also supports advanced features such as MPLS, TRILL, PFC, VEPA, QCN, VxLAN and NVGRE to meet the high-demanding Data Center's requirement for high performance, high speed and virtualization requirements.

The processor used on STORDIS BF6064X-T is the Intel® Xeon® Processor Broadwell-DE D1548 which is one of the D-1500 product families. There is also one Integrated Remote Management Processor-AST2520 which is a baseboard management controller (BMC).

1.1. Features

- 6.4Tbps interface bandwidth
- Support Jumbo Frame up to 9KB
- Support up to 256 ports
- 12-Stage Match-Action-Unit (MAU) pipeline up to 1.1GHz
- Alternate Store-Forward (ASF) mode – Cut-through is available to minimize the latency
- Power supply LED / FAN status LED indication
- Extensive system LED and per port LEDs
- Redundant power supply
- Standard 2U chassis height
- 19" rack mountable
- 22MB of packet buffer memory
- 2 x AC or DC Power Supply (one PSU is default, second PSU is optional)
- BSP for third party software porting requirement


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1.2. Main Components

STORDIS BF6064X-T	
CPU	BROADWELL-DE D-1548
BIOS (for CPU)	16MB NOR FLASH
Memory	16GBx2 DDR4 MODULE
Storage	64GB SLC SSD (Innodisk DEM24-64GD72SCAQN-E82)
TPM	ST33HTPH2E32AHA6
MAC	BFN-T10-064Q
Controller	1588 Controller
PLL	ZL30363GDG2
BMC	AST2520A2-GP
BIOS (for BMC)	32MB NOR FLASH
PHY (OOB Port)	WGI210AT *1, I211-AT *1
PSU	DPS-1300AB-6 D (1300W AC PSU) *2
DC FAN	MAX 13200 rpm (Front to Rear)

Table 1: Main Components

1.3. System Block Diagram

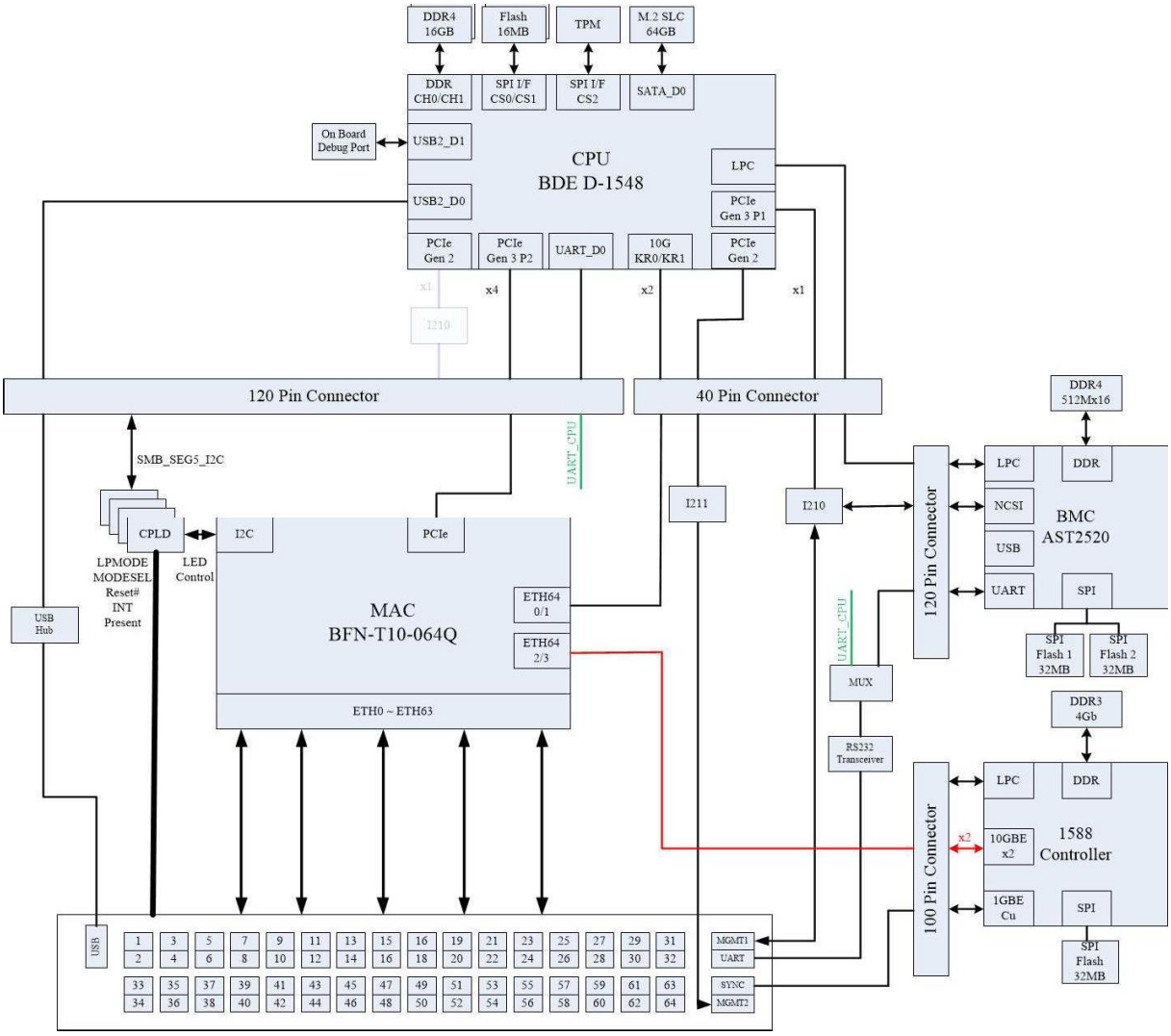

Figure 1: System Block Diagram

2. CPU SUBSYSTEM

Broadwell-DE D-1548

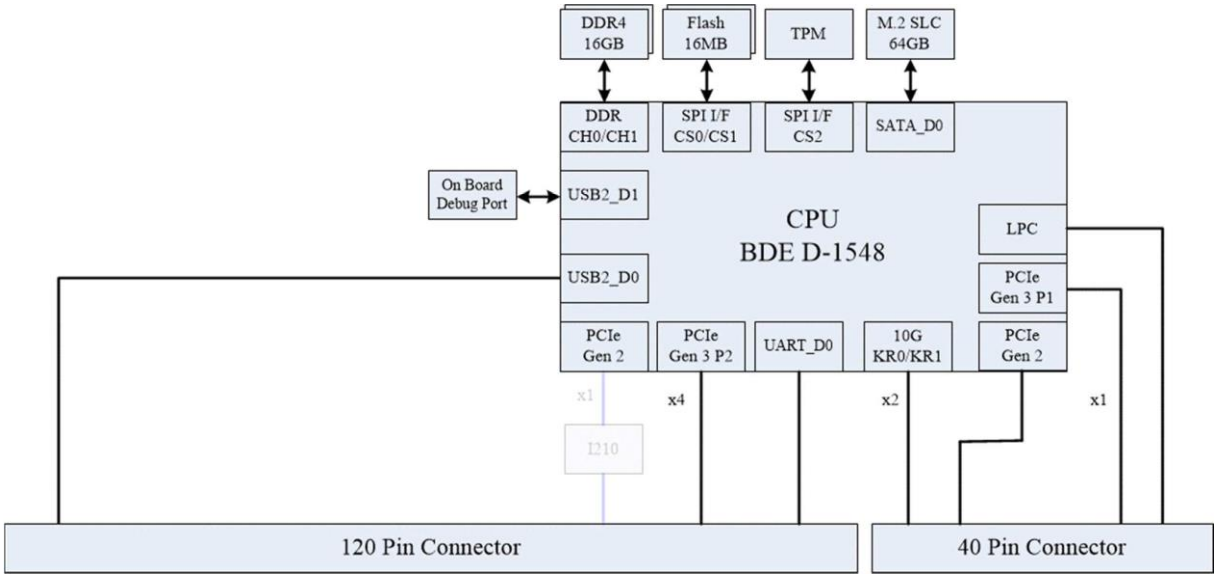

Figure 2: CPU Block Diagram

2.1. Interrupt

Use Broadwell-DE pin PIRQ[A:H]# to do interrupt handle, block diagram are shown as below figure.

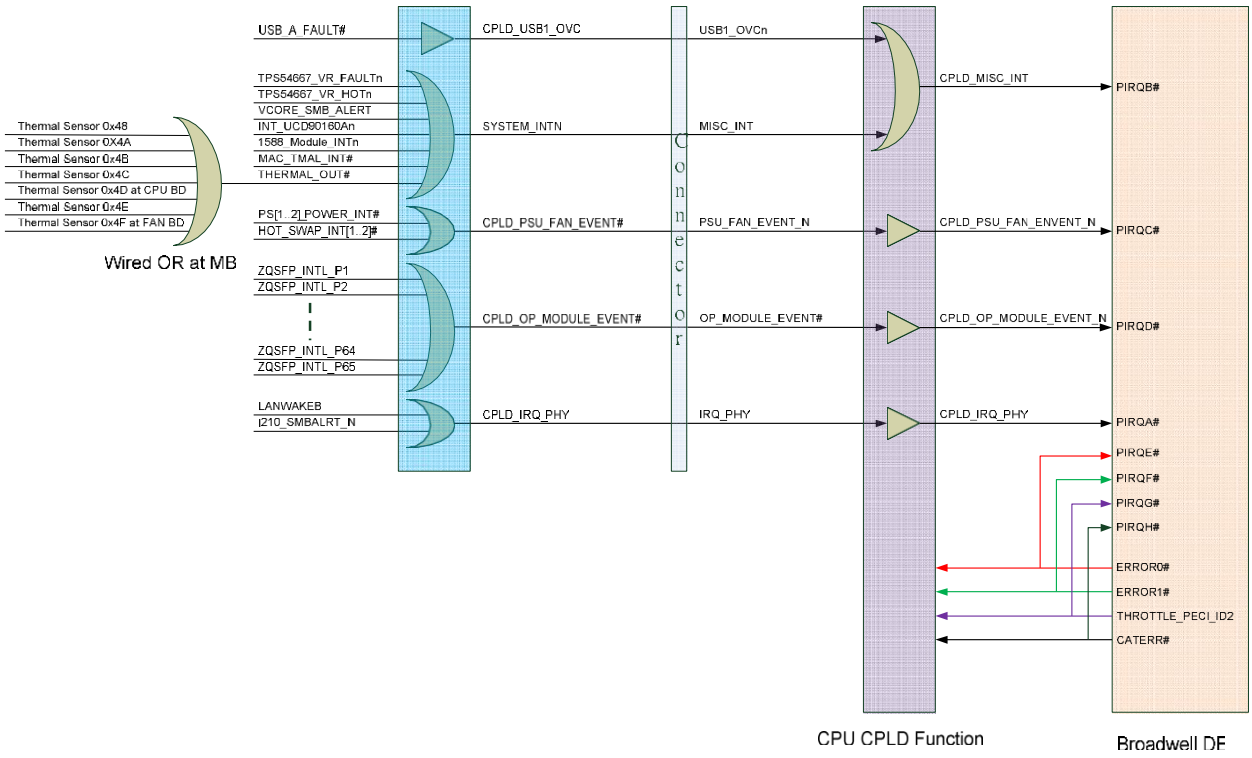

Figure 3: System Interrupt Block Diagram

2.2. PCIE

PCIe	Interface Number	Configs	Net name / Function
PCIE 3.0 Port 1	**PE1_0**	**x1**	**I210 (Gen1 only)**
	PE1_1		
	PE1_2		
	PE1_3		
	PE1_4		
	PE1_5		
	PE1_6		
	PE1_7		
	PE1_8		
	PE1_9		
	PE1_10		
	PE1_11		
	PE1_12		
	PE1_13		
	PE1_14		
	PE1_15		
PCIE 3.0 Port 2	**PE2_0**	**X4**	**BFN-T10-064Q**
	PE2_1		**BFN-T10-064Q**
	PE2_2		**BFN-T10-064Q**
	PE2_3		**BFN-T10-064Q**
	PE2_4		
	PE2_5		
	PE2_6		
	PE2_7		
PCIE 2.0	PCIE_1		
	PCIE_2	**x1**	I211
	PCIE_3		
	PCIE_4		
	PCIE_5		
	PCIE_6		
	PCIE_7		
	PCIE_8		

Table 2: CPU PCIE Configuration Table

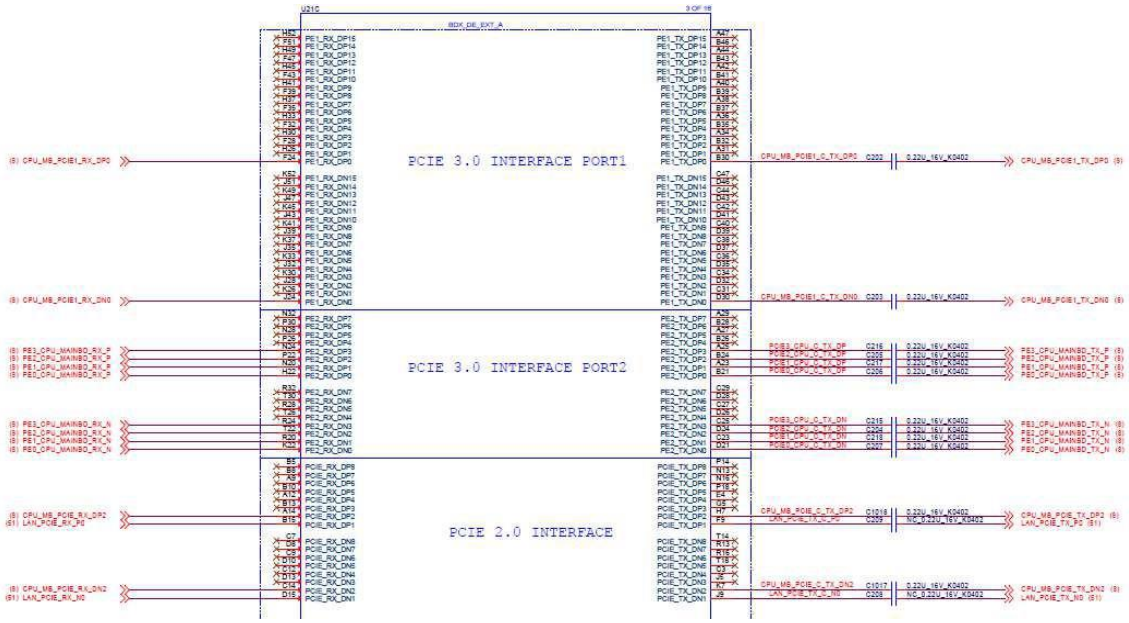

Figure 4: CPU PCIE

2.3. RTC

Intel Broadwell-DE processor (D-1500) The SoC contains a real-time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions:

- Keeping the date and time
- Storing system data in its RAM when the system is powered down

The SoC RTC module requires an external oscillating source of 32.768 kHz.

2.4. LPC

The LPC serves as a PCI-to-ISA bridge to a number of legacy ISA devices integrated in the SoC and to the external LPC-1.1-compliant devices BMC and CPLD connected to the LPC interface pins.

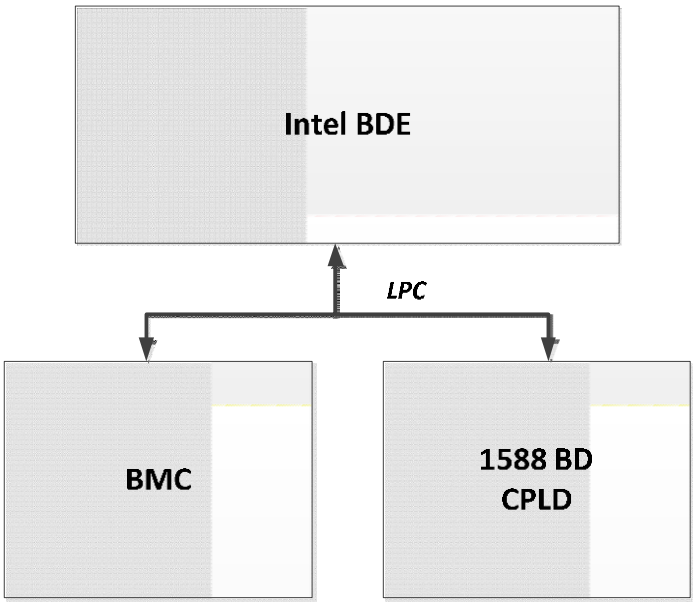

Figure 5: LPC Block Diagram

LPC Device	LPC IO address	Cycle Type
BMC	4Eh, 4Fh	I/O R/W
1588 BD CPLD	62h, 66h	I/O R/W

Table 3: LPC Address Table

2.5. UART

BROADWELL-DE processor (D-1548) contains 2 Universal Asynchronous Receiver/Transmitter (UART) serial ports integrated into the Platform Controller Unit (PCU). The UARTs are controlled by the software using programmed I/O.

2.5.1. UART0

For STORDIS BF6064X-T, UART0 of CPU is used for one of console port source (default) and another is from UART5 of BMC. Console MUX is controlled by CPLD. Both CPU and BMC can generate MUX select trigger signal, a low-high-low pulse with pulse width 100ms minimum, to switch MUX channel.

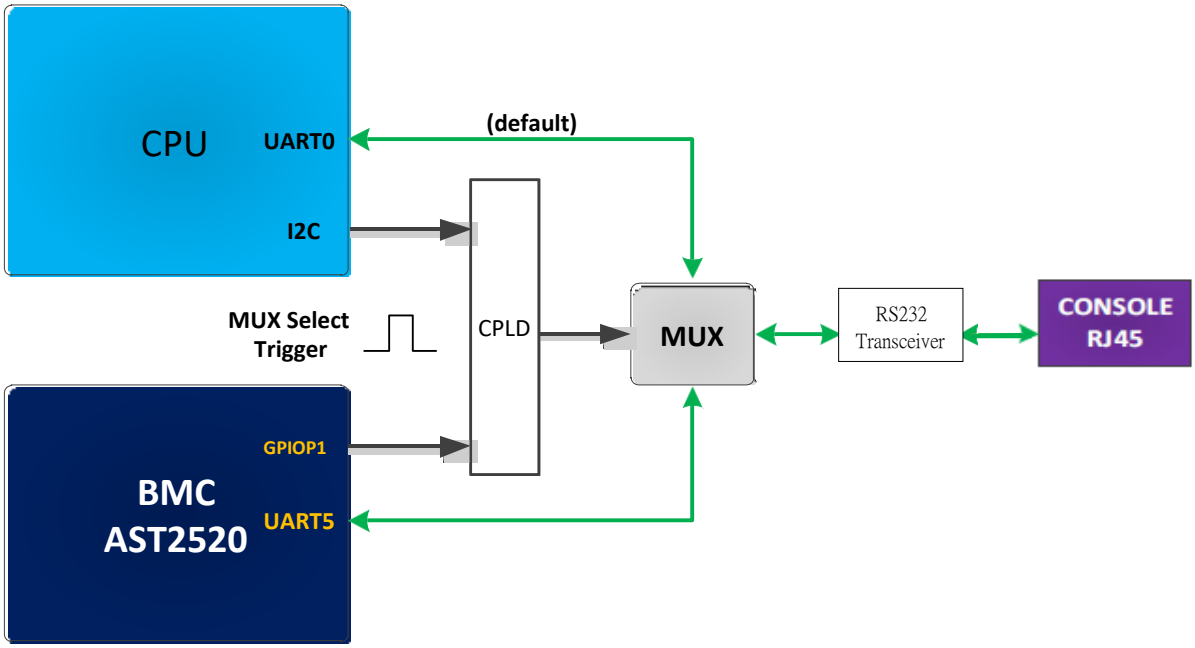

Figure 6: Console Port Option

2.5.2. UART1

1588 Controller UART is connected to UART1 port of Broadwell-DE. Console message could be mirrored to UART0 port. SC16S741AIPW is a slave I2C to UART converter IC, which is providing a debugging interface.

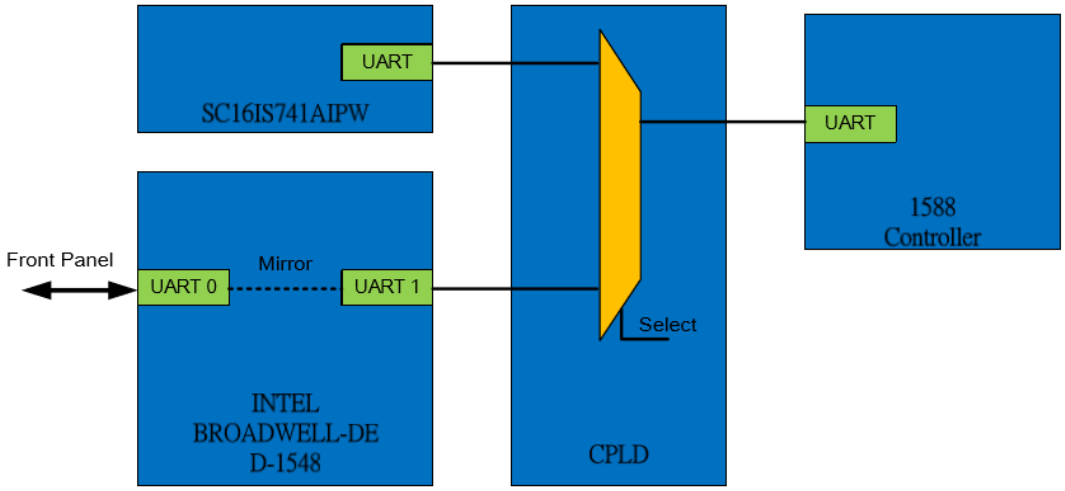

Figure 7: CPU UART1 and 1588 Controller UART

2.6. sVID

Intel BROADWELL-DE Processor is required to follow sVID protocol.

The voltage rails for the cores (VCCIN) and memory (VCCD) supports IMON as defined by the VR12/IMVP7 sVID protocol specification. The sVID controller consists of three signal pins and is defined in the VR12/IMVP7 Pulse Width Modulation, Version 1.61.

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
SVID_ALERT_N	I		VCCIOIN	SVID Alert (Serial Voltage Identification Alert): (active low). Used by VR to signal that the prior request has not reached the requested operating point.
SVID_DATA	I/OD		VCCIOIN	SVID Data (Serial Voltage Identification Data): Bi-Directional signal. Used as data communication interface between the SoC and VR.
SVID_CLK	OD		VCCIOIN	SVID Clock (Serial Voltage Identification Clock): The SoC and VR use this clock for communication on the SVID Data bus. SoC SVID requests are driven out on SVID Data with this clock and are registered in the VR using this for the clock. When the VR responds, it also uses this clock to drive the data.

Table 4: CPU Board, sVID Control Signals

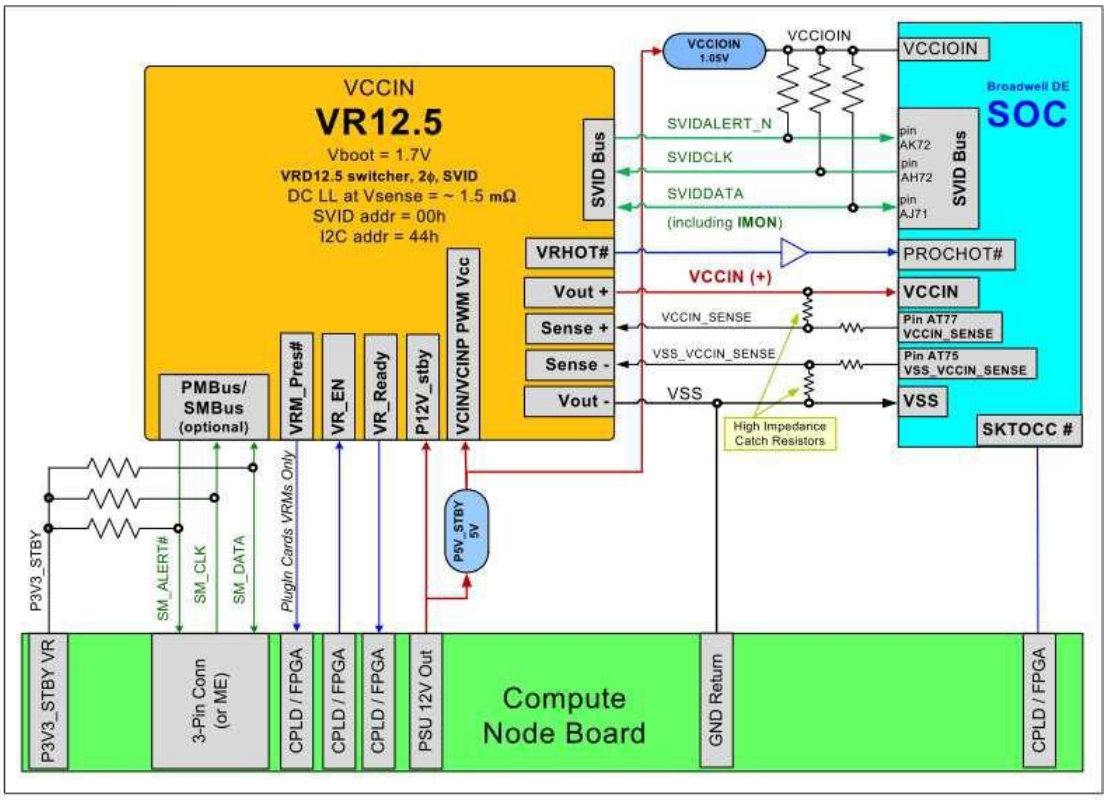

Figure 8: CPU Board VR12.5 Block Diagram

2.7. Reset

Once power on the device, CPLD will run power and reset sequence automatically. After power on stage, CPU can reset peripheral devise through CPLD, detail access method please refer to CPLD design SPEC.

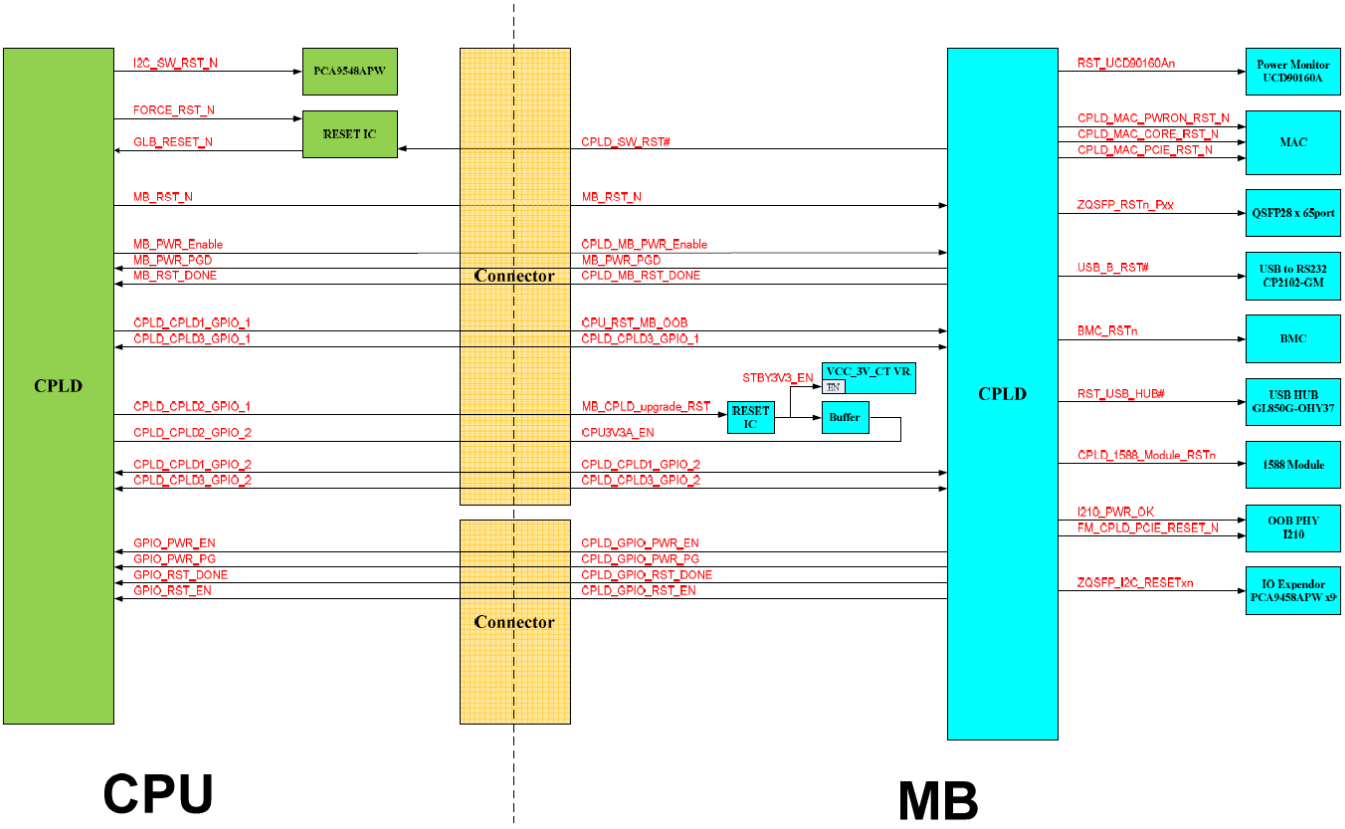

Figure 9: CPU Board, Reset Block Diagram

2.8. CPLD

BROADWELL-DE CPU BOARD contains of a CPLD such as Lattice MachXO and the part number is LCMXO2-1200UHC- 4FTG256C.

2.8.1. In-System Programmable

The CPLD supports In-System Programmable (ISP) to reconfigure the logic and function of a device. ISP devices eliminate limitations associated with traditional programmable devices and deliver benefits in board- and system-level design, manufacturing and programming. With ISP devices, hardware is as flexible and easy to modify as software and design upgrades are simple. Because ISP devices can be treated like any other device on the PCB, no special manufacturing flow is required to program ISP devices; standard logic level programming signals are easily generated by a PC, Sun Workstation, ATE (Automatic Test Equipment) or system embedded microprocessor. In pioneering ISP products, Lattice has developed an integrated solution of silicon, software and applications know-how that make ISP products practical. The CPLD would be programming through 4-pin JTAG which was connected to the CPU GPIO pins.

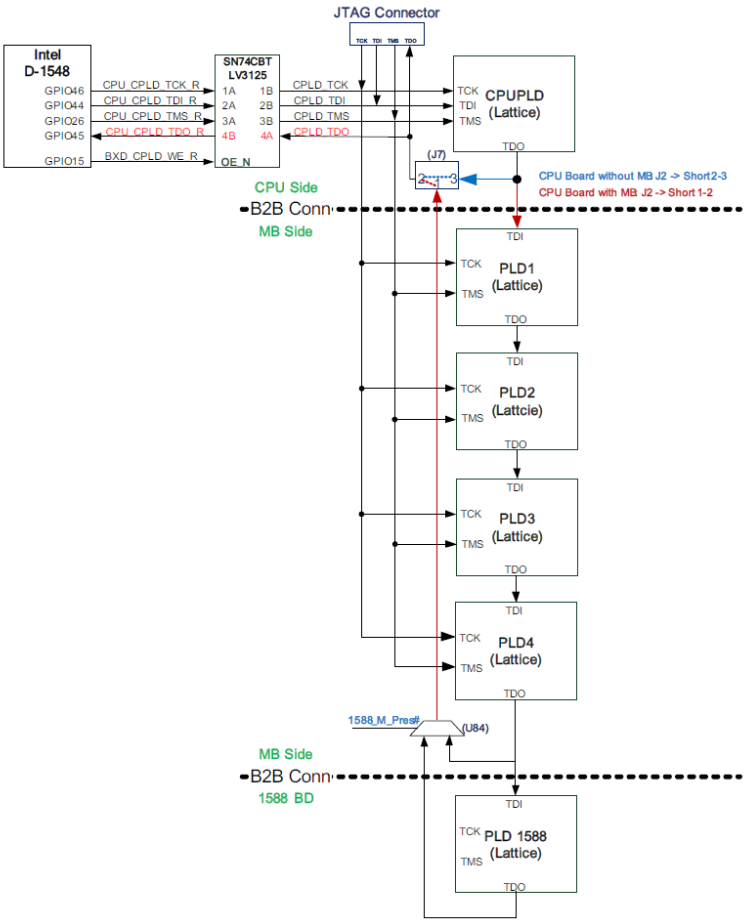

Figure 10: CPLD FW Upgrade from BROADWELL-DE

When the buffer EN is low, the programming bus is controlled by CPU. And when buffer EN is high, the CPLD is programmed by CPLD JTAG tools.

2.9. TPM

BROADWELL-DE CPU BOARD contains of a TPM IC, ST ST33HTPH2E32AHA6, and features are listed below:

- Supporting 2 modes exclusively with either the TPM 1.2 or the TPM 2.0 command set.
- Supporting dynamic switch from one mode to anther and capability to lock irreversibly one node.
- For TPM 1.2, compliant with Trusted Computing Group (TCG) Trusted Platform Module (TPM) Main specifications 1.2, Level 2 Revision 116 and TCG PC Client Specific TPM Interface Specifications 1.3
- For TPM 2.0, compliant with Trusted Computing Group (TCG) Trusted Platform Module (TPM) Library specifications 2.0, Level 0, Revision 116 and TCG PC Client Specific TPM Platform Specifications 0.43
- TPM firmware code can be upgraded thanks to persistent Application Flash Loader to support new standard evolutions
- Common Criteria certification according to the TPM 1.2 and TPM 2.0 protections profiles at EAL4+

3. SWITCH SUBSYSTEM

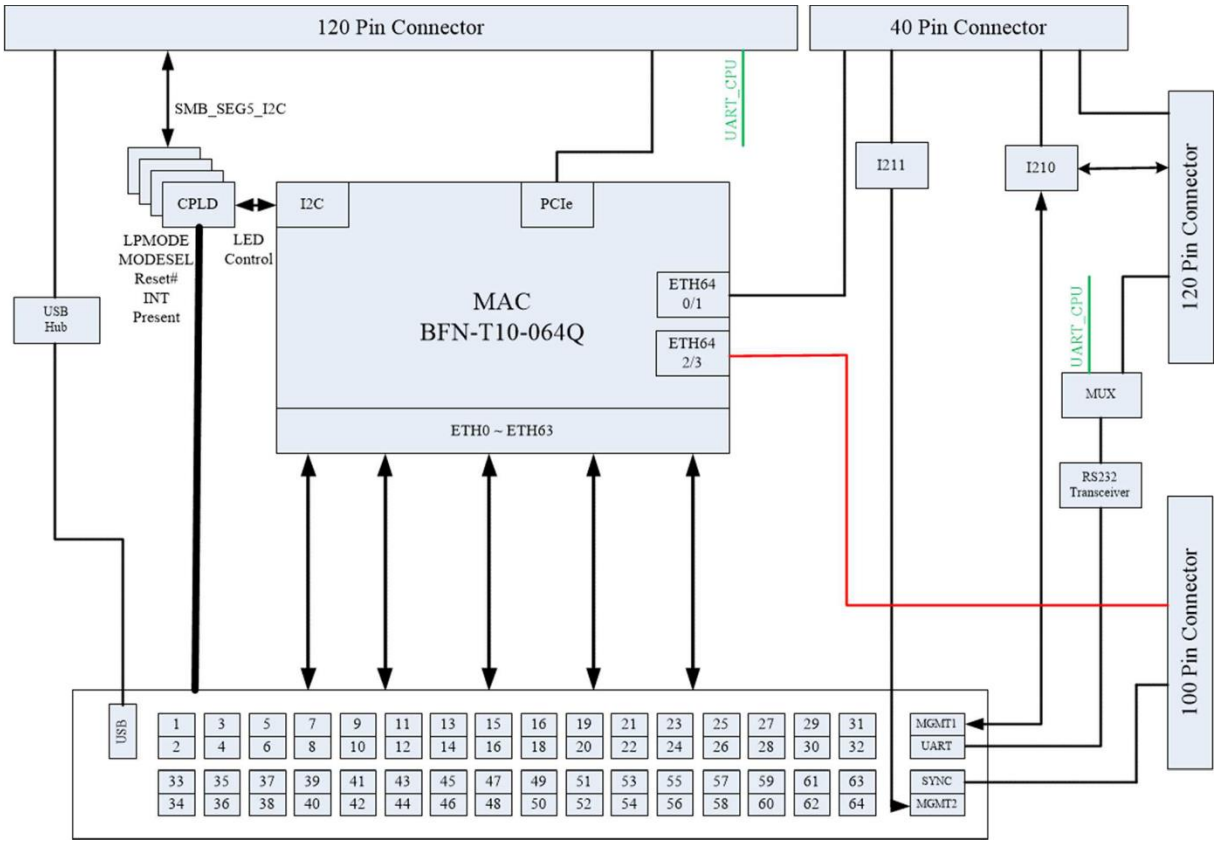

Figure 11: Switch Block Diagram

3.1. Switch Engine

The 10k-series is a family of highly integrated, flexible packet forwarding devices, which are programmed using the P4 programming language. The 10k family can be used in a number of different applications such as ultra-high density top-of-rack systems, multi-chip chassis based systems, or as fabric interconnection devices. The programmable nature of the 10k-series pipeline combined with the match-action forwarding model allows for end users to easily define new protocols, features, and forwarding functionality in the field.

Highlights:

- 6.4Tbps single chip Ethernet switch
- User specified forwarding model using P4 language allowing for flexibility and advanced use cases:
    - Flexible resource allocation
    - Data plane liveness detection, fault handling, and failover
    - Packet trace history/coalescing
- Optimized for 100GE/50GE/40GE/25GE
- High speed CPU interface

- 22MB unified packet buffer
- Line rate packet generator with user defined triggers

3.2. STORDIS BF6064X-T Port Allocation

3.2.1. Front Panel Port Number

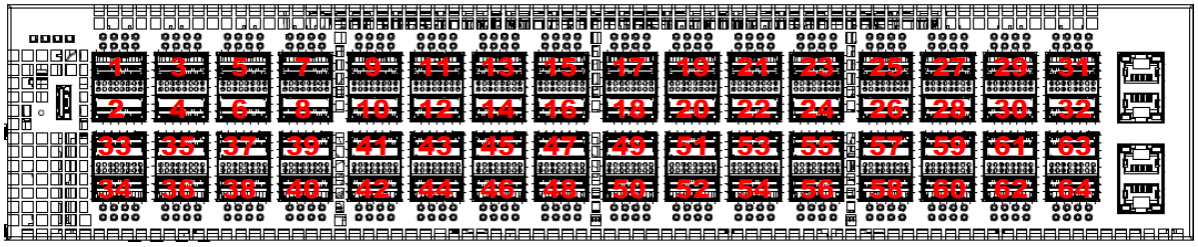

Figure 12: Port Number on Front Panel

3.2.2. Front Port and MAC Port Mapping

Port No	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
MAC No	3	63	59	55	15	11	7	51	47	31	27	23	19	43	39	35
MAC No	2	62	58	54	14	10	6	50	46	30	26	22	18	42	38	34
Port No	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32
PCB																
Port No	33	35	37	39	41	43	45	47	49	51	53	55	57	59	61	63
MAC No	0	60	56	52	12	8	4	48	44	28	24	20	16	40	36	32
MAC No	1	61	57	53	13	9	5	3	45	29	25	21	17	41	37	33
Port No	34	36	38	40	42	44	46	48	50	52	54	56	58	60	62	64

Figure 13: Port Mapping Summary

3.2.3. Tofino SERDES Configuration

3.2.3.1. Front Panel QSFP Port Configuration

QSFPPort#	QSFP Lane #	ETH # of Tofino	TX Lane	TX PN Swap	RX Lane	RX PN Swap
1	0	3	0	Y	0	N
	1		1	N	1	Y
	2		2	Y	2	Y
	3		3	N	3	Y
2	0	2	0	Y	0	Y
	1		1	Y	1	N
	2		2	Y	2	N
	3		3	Y	3	Y
3	0	63	0	Y	0	Y
	1		1	N	1	Y
	2		2	Y	2	N
	3		3	N	3	Y
4	0	62	2	Y	2	Y
	1		3	Y	3	N
	2		0	Y	0	N
	3		1	Y	1	N
5	0	59	1	N	1	N
	1		0	N	0	Y
	2		2	N	2	Y
	3		3	Y	3	Y
6	0	58	1	N	1	Y
	1		0	Y	0	Y
	2		3	N	3	N
	3		2	Y	2	N
7	0	55	1	Y	1	Y
	1		0	N	0	N
	2		3	Y	3	Y
	3		2	N	2	Y
8	0	54	1	Y	1	Y
	1		0	N	0	Y
	2		3	Y	3	Y
	3		2	N	2	N
9	0	15	0	N	0	Y
	1		1	Y	1	Y
	2		2	N	2	N
	3		3	Y	3	Y
10	0	14	1	N	1	Y
	1		0	Y	0	Y
	2		3	N	3	N
	3		2	Y	2	N
11	0	11	0	N	0	Y
	1		1	Y	1	Y
	2		3	N	3	N
	3		2	N	2	N
12	0	10	1	Y	1	Y
	1		0	Y	0	N
	2		3	N	3	N
	3		2	Y	2	N
13	0	7	0	N	0	Y
	1		1	Y	1	Y
	2		3	N	3	Y
	3		2	N	2	N
14	0	6	1	Y	1	Y
	1		0	Y	0	Y
	2		3	N	3	Y
	3		2	Y	2	N
15	0	51	1	N	1	N
	1		0	N	0	N
	2		3	N	3	Y
	3		2	N	2	N
16	0	50	1	Y	1	Y
	1		0	Y	0	Y
	2		2	Y	2	Y
	3		3	Y	3	N

QSFPPort#	QSFP Lane #	ETH # of Tofino	TX Lane	TX PN Swap	RX Lane	RX PN Swap
17	0	47	1	N	1	Y
	1		0	N	0	Y
	2		2	N	2	N
	3		3	N	3	Y
18	0	46	0	Y	0	Y
	1		1	Y	1	N
	2		3	Y	3	N
	3		2	Y	2	N
19	0	31	1	Y	1	N
	1		0	N	0	Y
	2		3	N	3	Y
	3		2	N	2	N
20	0	30	0	Y	0	Y
	1		1	N	1	Y
	2		2	Y	2	N
	3		3	Y	3	N
21	0	27	0	Y	0	N
	1		1	N	1	Y
	2		2	N	2	N
	3		3	N	3	Y
22	0	26	0	Y	0	Y
	1		1	Y	1	N
	2		3	Y	3	N
	3		2	N	2	N
23	0	23	1	N	1	N
	1		0	N	0	N
	2		3	N	3	Y
	3		2	N	2	N
24	0	22	1	Y	1	Y
	1		0	N	0	N
	2		2	Y	2	N
	3		3	Y	3	Y
25	0	19	0	Y	0	Y
	1		1	N	1	Y
	2		2	Y	2	N
	3		3	N	3	Y
26	0	18	0	Y	0	Y
	1		1	N	1	N
	2		3	Y	3	N
	3		2	N	2	N
27	0	43	1	N	1	Y
	1		0	N	0	N
	2		2	N	2	N
	3		3	Y	3	Y
28	0	42	0	N	0	Y
	1		1	Y	1	N
	2		3	N	3	N
	3		2	Y	2	N
29	0	39	1	Y	1	Y
	1		0	N	0	Y
	2		2	Y	2	N
	3		3	N	3	Y
30	0	38	0	Y	0	Y
	1		1	N	1	N
	2		2	Y	2	N
	3		3	N	3	Y
31	0	35	0	N	0	N
	1		1	N	1	Y
	2		2	Y	2	Y
	3		3	N	3	Y
32	0	34	1	Y	1	Y
	1		0	Y	0	Y
	2		2	Y	2	N
	3		3	Y	3	N

QSFPPort#	QSFP Lane #	ETH # of Tofino	TX Lane	TX PN Swap	RX Lane	RX PN Swap
33	0	0	0	Y	0	Y
	1		1	N	1	Y
	2		2	N	2	N
	3		3	N	3	N
34	0	1	2	Y	2	N
	1		3	N	3	N
	2		1	N	1	Y
	3		0	Y	0	Y
35	0	60	2	N	2	Y
	1		3	N	3	N
	2		0	N	0	N
	3		1	N	1	N
36	0	61	3	Y	3	N
	1		2	N	2	Y
	2		0	N	0	N
	3		1	N	1	Y
37	0	56	3	Y	3	Y
	1		2	N	2	Y
	2		1	Y	1	N
	3		0	Y	0	Y
38	0	57	0	N	0	N
	1		1	N	1	Y
	2		3	Y	3	Y
	3		2	N	2	N
39	0	52	2	N	2	Y
	1		3	N	3	Y
	2		1	N	1	N
	3		0	Y	0	Y
40	0	53	3	N	3	N
	1		2	Y	2	N
	2		1	N	1	N
	3		0	Y	0	Y
41	0	12	1	Y	1	Y
	1		0	N	0	Y
	2		3	Y	3	N
	3		2	N	2	N
42	0	13	3	Y	3	N
	1		2	N	2	Y
	2		1	Y	1	Y
	3		0	N	0	Y
43	0	8	1	Y	1	N
	1		0	N	0	N
	2		2	Y	2	Y
	3		3	N	3	N
44	0	9	1	Y	1	N
	1		0	N	0	N
	2		3	Y	3	Y
	3		2	N	2	N
45	0	4	3	Y	3	Y
	1		2	N	2	N
	2		0	N	0	N
	3		1	N	1	N
46	0	5	3	Y	3	N
	1		2	N	2	N
	2		1	Y	1	Y
	3		0	N	0	Y
47	0	48	2	N	2	Y
	1		3	N	3	Y
	2		0	N	0	N
	3		1	Y	1	Y
48	0	49	2	Y	2	N
	1		3	N	3	N
	2		0	N	0	N
	3		1	N	1	Y

QSFPPort#	QSFPLane#	ETH #of Tofino	TX Lane	TX PN Swap	RX Lane	RX PN Swap
49	0	44	3	N	3	Y
	1		2	N	2	Y
	2		0	N	0	N
	3		1	N	1	Y
50	0	45	3	N	3	N
	1		2	N	2	N
	2		1	N	1	Y
	3		0	N	0	Y
51	0	28	3	Y	3	Y
	1		2	N	2	Y
	2		1	N	1	N
	3		0	Y	0	Y
52	0	29	3	N	3	N
	1		2	N	2	Y
	2		1	N	1	Y
	3		0	Y	0	Y
53	0	24	2	N	2	Y
	1		3	N	3	Y
	2		1	N	1	N
	3		0	Y	0	Y
54	0	25	3	N	3	N
	1		2	Y	2	Y
	2		0	N	0	Y
	3		1	Y	1	Y
55	0	20	1	N	1	Y
	1		0	Y	0	Y
	2		3	N	3	N
	3		2	Y	2	N
56	0	21	3	N	3	N
	1		2	Y	2	Y
	2		1	N	1	Y
	3		0	N	0	Y
57	0	16	3	N	3	Y
	1		2	N	2	Y
	2		1	N	1	N
	3		0	Y	0	Y
58	0	17	3	N	3	N
	1		2	Y	2	Y
	2		1	N	1	N
	3		0	Y	0	Y
59	0	40	3	N	3	Y
	1		2	Y	2	Y
	2		1	N	1	N
	3		0	Y	0	Y
60	0	41	3	N	3	N
	1		2	Y	2	Y
	2		1	N	1	Y
	3		0	Y	0	Y
61	0	36	3	N	3	Y
	1		2	Y	2	Y
	2		1	N	1	N
	3		0	Y	0	Y
62	0	37	2	N	2	Y
	1		3	Y	3	N
	2		1	N	1	N
	3		0	Y	0	N
63	0	32	3	Y	3	Y
	1		2	N	2	Y
	2		1	Y	1	N
	3		0	N	0	Y
64	0	33	2	N	2	N
	1		3	N	3	N
	2		0	N	0	N
	3		1	N	1	Y

Table 5: Tofino SERDES Configuration-1

3.2.3.2. Internal SERDES Configuration

- LANE 0/1 of Tofino ETH64 connects to Intel Broadwell-DE. Lane speed is 10G
- LANE 2/3 of Tofino ETH64 connects to 1588 Controller. Lane speed is 10G.

QSFPPort#	QSFPLane#	ETH #of Tofino	TX Lane	TX PN Swap	RX Lane	RX PN Swap
NA	0	64	0	N	0	N
	1		1	N	1	N
	2		2	N	2	N
	3		3	N	3	N

Table 6: Tofino SERDES Configuration-2

3.3. VDD Voltage Setting

VR initial boot-up voltage level and Voltage ID settings are specified in the table below. User can get Tofino VDD value from CPLD.

VID[2:0][5]	Description	VDD_{MIN}	VDD_{PWR}[6]	VDD_{DC_MAX}	VDD_{MAX}	Units
000 (0)	Initial Boot VDD Voltage	822	848	870	917	mV
100 (4)	VDD AC/DC range	717	742	768	812	mV
010 (2)	VDD AC/DC range	742	768	793	837	mV
110 (6)	VDD AC/DC range	767	793	815	862	mV
001 (1)	VDD AC/DC range	792	818	840	887	mV
101 (5)	VDD AC/DC range	817	843	865	912	mV
011 (3)	VDD AC/DC range	842	869	890	937	mV
111 (7)	VDD AC/DC range	867	894	915	962	mV

Table 7: Tofino VDD Voltage Setting

4. BMC SUBSYSTEM

A baseboard management controller (BMC) is a specialized service processor that monitors the physical state of a network server or other hardware device using sensors and communicating with the system administrator through an independent connection. The BMC is part of the Intelligent Platform Management Interface (IPMI) and is usually contained in the motherboard or main circuit board of the device to be monitored.

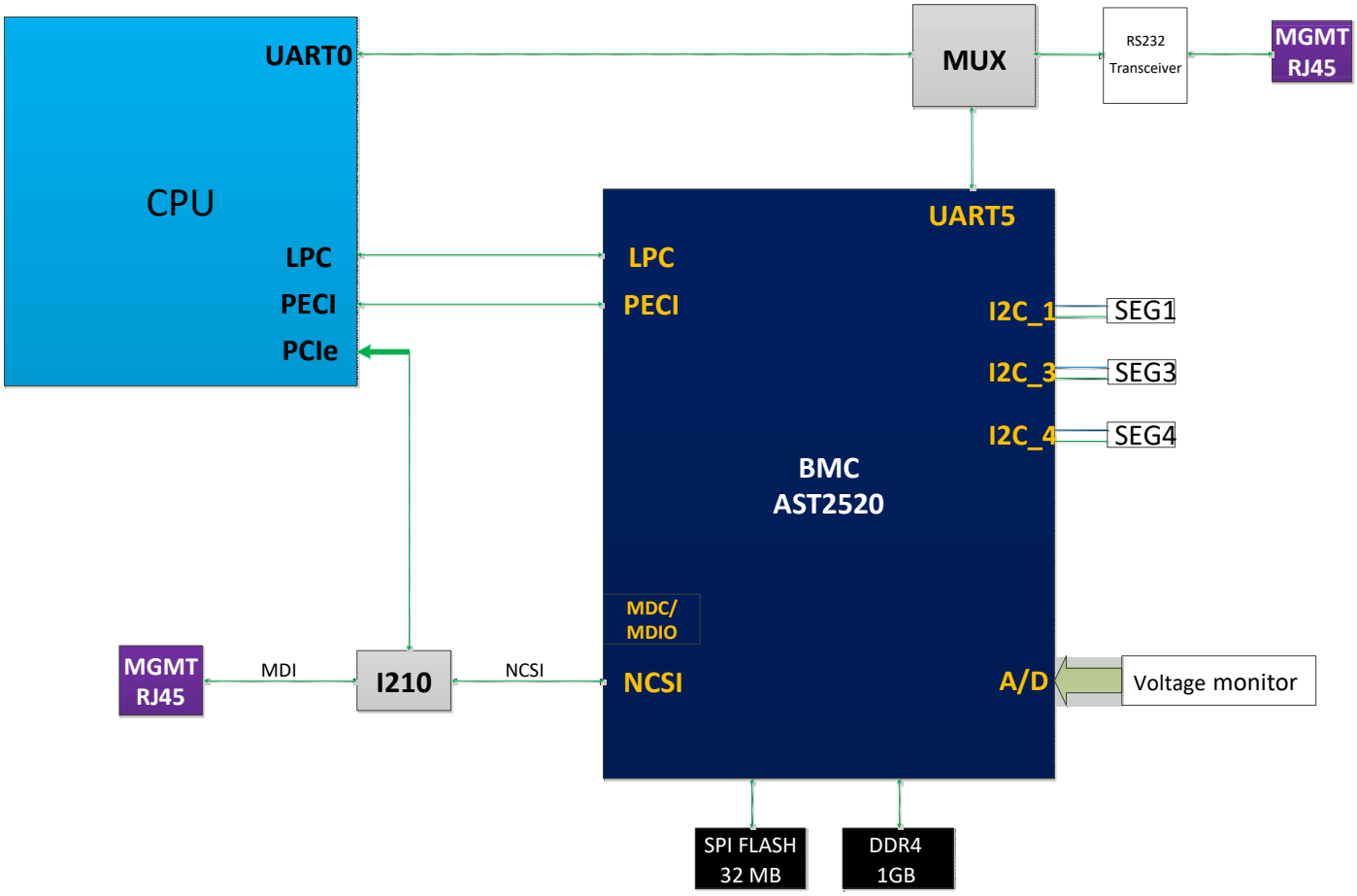

Figure 14: BMC Block Diagram

4.1. DDR4 SDRAM (K4A8G165WB-BCPB)

BMC designed install 512MByte memory on board.

[Table 1] Samsung 8Gb DDR4 B-die ordering information table

Organization	DDR4-2133 (15-15-15)	DDR4-2400 (17-17-17)[2]	Package
512Mx16	K4A8G165WB-BCPB	K4A8G165WB-BCRC	96FBGA

NOTE :
1. Speed bin is in order of CL-tRCD-tRP.
2. Backward compatible to DDR4-2133(15-15-15)

8 Gb Addressing Table

Configuration		2 Gb x4	1 Gb x8	512 Mb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A16	A0~A15	A0~A15
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

Figure 15: BMC Memory Configuration

- 16-bit DDR4 SDRAM (64Mb x 16 bits x 8 bank)
- Clock frequency: 800MHz (DDR4-1600)
- Power supply VDD: 1.2V (+/- 0.06V)
- Operating Temperature range: from 0 °C up to +95 °C

4.2. Firmware SPI Memory Control NOR flash (MX25L25635FMI-10G)

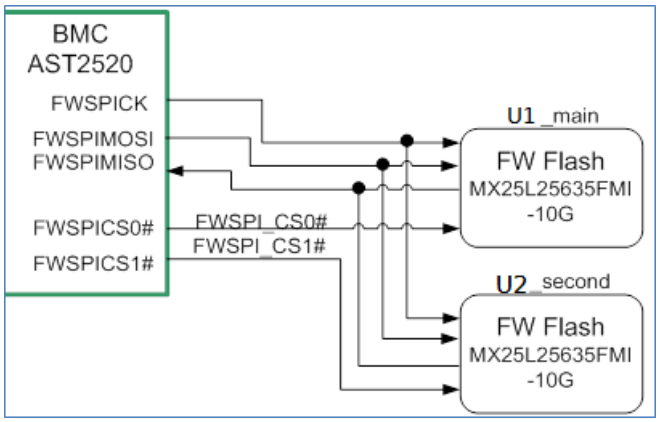

Figure 16: BMC System Flash Block Diagram

4.3. Hardware Strap Definition

Hardware Strap Table			
PIN NAME/BIT NUMBER	**PIN#**	**Description**	**Setting**
FWSPIMOSI / bit[31]	U17	**Enable SPI Flash Strap Auto Fetch Mode** 0: Disable. 1: Enable.	1
FWSPICK / bit[30]	AA18	**Enable GPIO Strap Mode** 0: Disable. 1: Enable.	1
TXD5 / bit[29]	K1	**Select UART Debug port** 0: Select UART1 as BMC console port. 1: Select UART5 as BMC console port. This bit is used to select the UART port for user debugging. It is not the BMC console function.	1
GPIOZ7 / bit[27]	W21	**Enable fast reset mode for ARM ICE debugger** 0: Long reset mode, normal operation. 1: Fast reset mode, for ICE debugger connection. Enable fast reset mode to enable ICE debugger can stop ARM at starting address 0.	1
RTCK / bit[26]	C9	**Enable eSPI flash mode** 0: eSPI respond with no flash attached. 1: eSPI respond with flash attached.	0
FWSPIMISO / bit[25]	T18	**Enable eSPI mode** 0: LPC mode. 1: eSPI mode.	0
RGMII2TXD3 / bit[24]	D4	**Select DDR4 SDRAM** 0: DDR3(L) SDRAM. 1: DDR4 SDRAM.	1
RGMII2TXD2 / bit[23]	D5	**Select 25 MHz reference clock input mode** 0: CLKIN is 24 MHz and USBCKI not used. 1: CLKIN is 25 MHz and USBCKI = 24/48 MHz (determined by bit[18]).	0
RGMII2TXD1 / bit[22]	B3	**Enable GPIOE pass-through mode** 0: Disable, pass through can be enabled by SCU8C [15:12]. 1: Enable pass-through at power on. Pass-through pins set: GPIOE0 → GPIOE1 GPIOE2 → GPIOE3 GPIOE4 → GPIOE5 GPIOE6 → GPIOE7	0
RGMII2TXD0 / bit[21]	A2	**Enable GPIOD pass-through mode** 0: Disable, pass through can be enabled by SCU8C [11:8]. 1: Enable pass-through at power on. Pass-through pins set: GPIOD0 → GPIOD1 GPIOD2 → GPIOD3 GPIOD4 → GPIOD5 GPIOD6 → GPIOD7	0
GPIOZ6 / bit[20]	V22	**Disable LPC to decode SuperIO 0x2E/0x4E address** 0: Enable address decoding. 1: Disable address decoding.	0

RGMII1TXD3 / bit[19]	D7	**Enable ACPI function** 0: Disable ACPI. 1: Enable ACPI.	0
GPIOZ5 / bit[18]	W22	**Select USBCKI input frequency** 0: 24 MHz. 1: 48 MHz.	0

GPIOZ4 / bit[17]	U21	**Enable BMC 2nd boot watchdog timer** 0: Disable 1: Enable BMC 2nd boot watchdog timer start counting at power up. The watchdog timer was located at WDT2. After watchdog timeout, it will reset BMC and restart booting from the 2nd boot flash at CS1#. CS1# must be the same flash type as CS0# and could be the same firmware as CS0#.	1
RGMII1TXD2 / bit[16]	E7	**SuperIO configuration address selection** 0: Decode 0x2E. 1: Decode 0x4E.	1
GPIOS7 / bit[15]	AA20	**VGA Class Code selection** 0: Select the Class Code for video device. 1: Select the Class Code for VGA device.	1
/ bit[14]	G22	**Select dedicated LPC reset input** 0: LPC reset is shared with PCIe reset pin. 1: LPC reset is located at pin number G22, shared with GPIOAC7.	1
RGMII1TXD1 / bit[13] RGMII1TXD0 / bit[12]	A5 F9	**SPI mode selection** 00: Disable SPI interface. 01: Enable SPI Master 10: RSVD, enable SPI Master and SPI Slave to AHB Bridge (debug mode) 11: Enable SPI Pass-through	11
/ bit[11:9]		**AXI/AHB clock frequency ratio selection** 000: undefined 001: Select AXI:AHB = 2:1 010: Select AXI:AHB = 3:1 011: Select AXI:AHB = 4:1 100: Select AXI:AHB = 5:1 101: Select AXI:AHB = 6:1 110: Select AXI:AHB = 7:1 111: Select AXI:AHB = 8:1 HCLK freq = H-PLL / 2 / (ratio of AXI-AHB)	001
/ bit[8]		**Enable software Secure-boot test mode** 0: Normal mode. 1: Enable Secure boot test mode.	0
RGMII2TXCTL / bit[7]	B1	**Define MAC#2 interface** 0: RMII/NCSI. 1: RGMII.	0
RGMII1TXCTL / bit[6]	E9	**Define MAC#1 interface** 0: RMII/NCSI. 1: RGMII.	0
GPIOS6 / bit[5]	U20	**Enable dedicated VGA BIOS ROM** 0: No VGA BISO ROM, VGA BIOS is merged in the system BIOS. 1: Enable dedicated VGA BIOS ROM.	0
GPIOS4 / bit[3:2]	R19	**VGA memory size selection** 00: Select 8 MB VGA memory. 01: Select 16 MB VGA memory. 10: Select 32 MB VGA memory. 11: Select 64 MB VGA memory. Defined the VGA memory size that will share with SOC memory.	01

FWSPICS0# / bit[0]	AB19	**Disable CPU boot** 0: Enable boot. 1: Disable CPU operation, when no firmware exists.	1

Table 8: BMC Hardware Strap Definition

4.4. LPC

The LPC serves as a PCI-to-ISA bridge to a number of legacy ISA devices integrated in the SoC and to the external LPC-1.1-compliant devices connected to the LPC interface pins. They are written and read by the software.

- Maximum running frequency: 33MHz
- Slave mode: designed for BMC functions (I/O R/W cycles)

4.5. UART

AST2520 supports a new hardware UART debug interface, which is different from the firmware console and doesn't require the firmware to support.

- "UART 5" for debug function.

4.6. ADC Voltage Monitor

ADC Engine has 16 voltage sensing channels. Each channel has upper and lower bound.

- Integrate 10-bit analog-to-digital converter (ADC)
- 16 low-leakage (< 1.0uA) inputs to measure up to 16 analog voltages
- Support intelligent hardware monitor function for all of the 16 analog input with interrupt option

ADC voltage divider

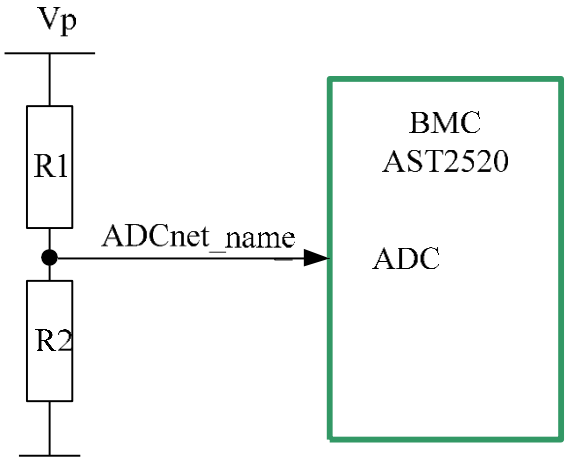

Figure 17: BMC ADC Voltage Measurement

Note: **Input voltage = ADC_Value Step + 1) / 1024 x 1.8 = Vp x R2 / (R1+R2)**

Vp	R1	R2	BMC_ADC		
			channel	net name	Input voltage
VCC_12V	5.6k	0.68k	0	ADC0	1.299V
VCC_5V	5.6k	2k	1	ADC1	1.315V
VCC_3V3V	10k	6.8k	2	ADC2	1.335V
VCC_3V_CT	10K	6.8K	3	ADC3	1.335V
VCC_2V5	5.76K	6.8K	4	ADC4	1.353V
VCC_MAC_AVDD_0V 9	0	NC	5	ADC5	0.9V
VCC_MAC_VDD_0V8	0	NC	6	ADC6	0.8V
DDR_2V5	5.76K	6.8K	13	ADC13	1.35V
BMC_DDRVDDQ	0	NC	14	ADC14	1.2V
BMC_1V15	0	NC	15	ADC15	1.15V

Table 9: BMC ADC Voltage Detection List

5. 1588 Controller SUBSYSTEM

1588 Controller is specialized for IEEE 1588 application. The device contains a powerful VCore-III CPU system that is based on an embedded MIPS24KEc compatible microprocessor. The VCore-III system can handle networking protocols, for example, IEEE-1588 protocols stack.

5.1. Boot Strip

Item	Value	Description
VCORE_CFG[3:0]	0000	VCore-III CPU is enabled (Little Endian mode) and boots from SI (the SI slave is disabled)
REFCLK2_SEL	1	PLL2 is source of switch core and VCore clocks
REFCLK2_CONF[2:0]	001	156.25MHz

Table 10: 1588 Controller Boot Strip Setting

5.2. DDR3 SDRAM

1588 Controller designed install 512MByte memory on board.

- 16-bit DDR3 SDRAM (256Mb x 16 bits)
- Power supply VDD: 1.5V (+/- 0.75V)
- Operating Temperature range: from 0 °C up to +95 °C

Lead-free RoHS compliance and Halogen-free

4Gb (Org. / Package)		Length x Width (mm)	Ball pitch (mm)
512Mb x 8	78-ball TFBGA	8.00 x 10.50	0.80
256Mb x 16	96-ball TFBGA	8.00 x 13.00	0.80

Density and Addressing

Organization	512Mb x 8	256Mb x 16
Bank Address	BA0 – BA2	BA0 – BA2
Auto precharge	A10 / AP	A10 / AP
BL switch on the fly	A12 / $\overline{BC}$	A12 / $\overline{BC}$
Row Address	A0 – A15	A0 – A14
Column Address	A0 – A9	A0 – A9
Page Size	1KB	2KB
tREFI(us) [3]	*Tc*<=85℃:7.8, *Tc*>85℃:3.9	
tRFC(ns) [4]	260ns	

Figure 18: 1588 Controller Memory Configuration

5.3. SPI

CS0: connected to NOR Flash

- MX25L25645GM2I-10G, 256Mb serial NOR Flash for firmware storage.

CS1: connected to ZL30363

5.4. UART

1588 Controller connects Broadwell-DE UART1. Please refer to CPU UART section for more detail

5.5. Switch Port Mapping

- Port 0 connects to front panel SYNC port
- Port 9 connects to **Lane 2 of Tofino ETH64**
- Port 10 connects to **Lane 3 of Tofino ETH64**

Port Number	Port Module	Port Speed	Interface Macro	Connection
0	DEV2G5_0	1 Gbps	CUPHY_0	Front Panel SYNC Port
1	DEV2G5_1	NA	CUPHY_1	NA
2	DEV2G5_2	NA	SERDES1G_2	NA
3	DEV2G5_3	NA	SERDES1G_3	NA
4(NPI)	DEV2G5_4	NA	SERDES1G_4	NA
5	DEV2G5_5	NA	SERDES6G_0	NA
6	DEV2G5_6	NA	SERDES6G_1	NA
7	DEV2G5_7	NA	SERDES10G_0	NA
8	DEV2G5_8	NA	SERDES10G_1	NA
9	DEV10G_0	10 Gbps	SERDES10G_2	Lane 2 of Tofino ETH64
10	DEV10G_1	10 Gbps	SERDES10G_3	Lane 3 of Tofino ETH64

Table 11: 1588 Controller Port Mapping

6. FAN SUBSYSTEM

6.1. System FAN speed control

The FAN system supports FAN speeds control for different environment temperature workable. Two Linear Fan-Speed Controller “EMC2305” for the FAN speed controls.

FAN Connection diagram

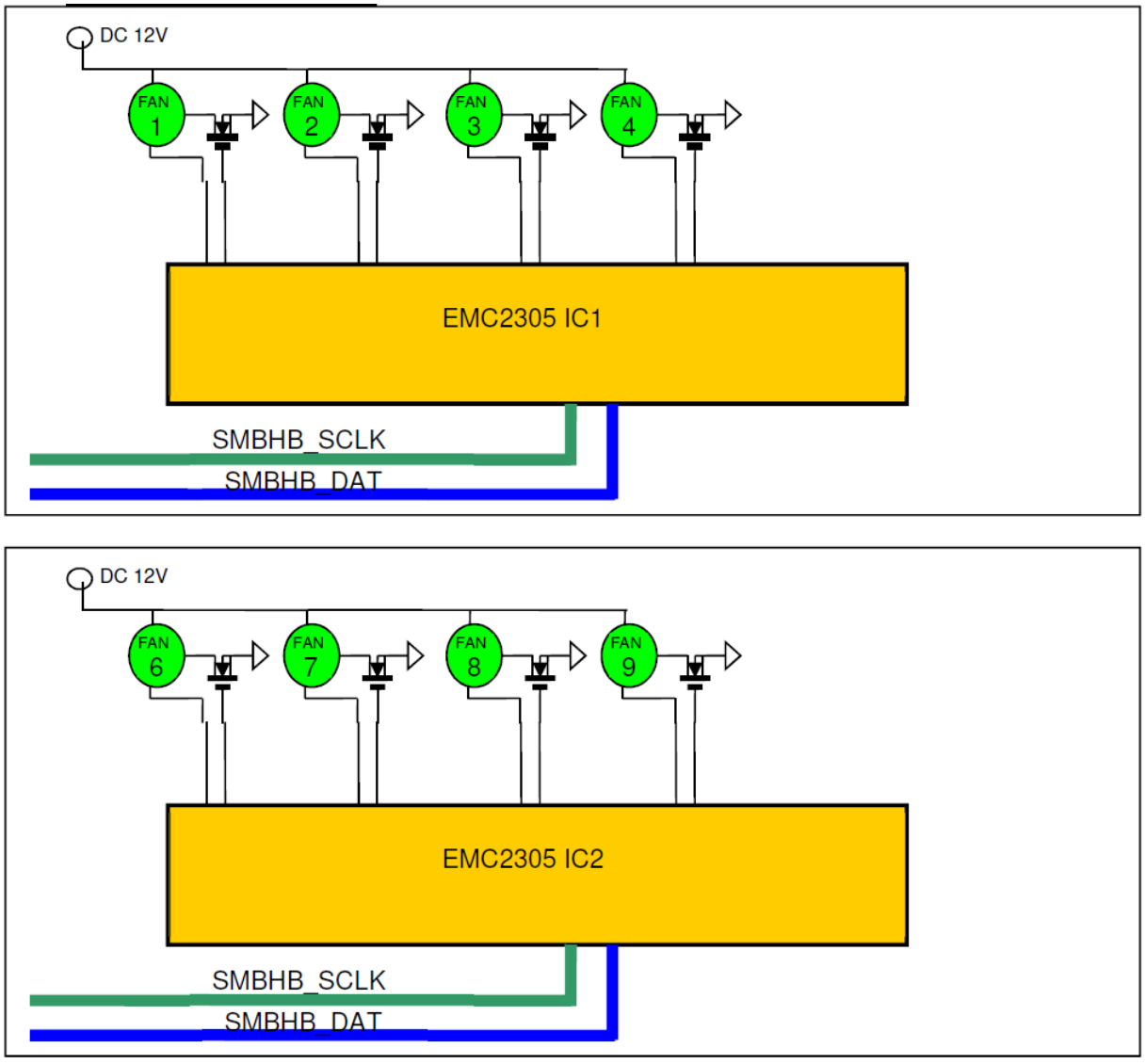

Figure 19: FAN Unit, Block Diagram

EMC2305 FAN Speed control

For FAN speed control, it can directly set register 30h, 40h, 50h and 60h of EMC2305.

Table 5.8 Fan Driver Setting Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
30h	R/W	Fan 1 Setting	128	64	32	16	8	4	2	1	00h
40h	R/W	Fan 2 Setting	128	64	32	16	8	4	2	1	00h
50h	R/W	Fan 3 Setting	128	64	32	16	8	4	2	1	00h
60h	R/W	Fan 4 Setting	128	64	32	16	8	4	2	1	00h
70h	R/W	Fan 5 Setting	128	64	32	16	8	4	2	1	00h

The Fan Setting register always displays the current setting of the respective fan driver. Reading from any of the registers will report the current fan speed setting of the appropriate fan driver regardless of the operating mode. Therefore it is possible that reading from this register will not report data that was previously written into this register.

While the RPM-based Fan Speed Control Algorithm is active, the register is read only. Writing to the register will have no effect and the data will not be stored.

The contents of the register represent the weighting of each bit in determining the final output voltage. The output drive for a PWM output is given by Equation [1].

$$Drive = \left(\frac{VALUE}{255}\right) \times 100\% \qquad [1]$$

The following table shows a brief register setting value for fan speed control.

Fan Speed	50%	60%	70%	80%	90%	100%
Register Set	0x80	0x99	0xB3	0xCC	0xE6	0XFF

Table 12: Register Setting for Fan Speed Control

6.2. Over Temperature Protection

There are many thermal sensors in the system, help to monitor system temperature. User can get temperature through I2C. Meanwhile, both Broadwell-DE and Tofino have built in thermal sensor, which provides chip die temperature, and user can get this information from SW function.

Item	Schematics Ref.	I2C address	I2C Channel	PCB	Description	Part number
1	U36	0x4D	SML0	CPU	CPU Thermal Sensor	TMP75AIDR
2	U505	0x48	SMB (CH3)	MB	MAC Thermal Sensor 1	TMP461AIR UNR
3	U59	0x4A	SMB (CH3)	MB	MAC Thermal Sensor 2	TMP75AIDR
4	U58	0x4B	SMB (CH3)	MB	Inlet Thermal Sensor 1	TMP75AIDR
5	U56	0x4C	SMB (CH3)	MB	Inlet Thermal Sensor 2	TMP75AIDR
6	U57	0x4E	SMB (CH3)	MB	Inlet Thermal Sensor 3	TMP75AIDR
7	U334	0x4F	SMB (CH3)	FAN Control	Outlet Thermal Sensor 3	TMP75AIDR
8	U521	0x60	SMB (CH3)	MB	Power Thermal Sensor	TPS53667
9	PSU1	0x58	SMB (CH4)	PSU	PSU internal temp	
10	PSU2	0x59	SMB (CH4)	PSU	PSU internal temp	
11	CPU(U21)	NA	NA	CPU	CPU Internal temp	
12	MAC(U500)	NA	NA	MB	MAC Internal temp	

Table 13: Thermal Sensor List

6.3. Fan RFU

There are 4 Fan Tray modules on STORDIS BF6064X-T. All modules can be replaced and installed in the field. The following diagram shows Fan tray number and address.

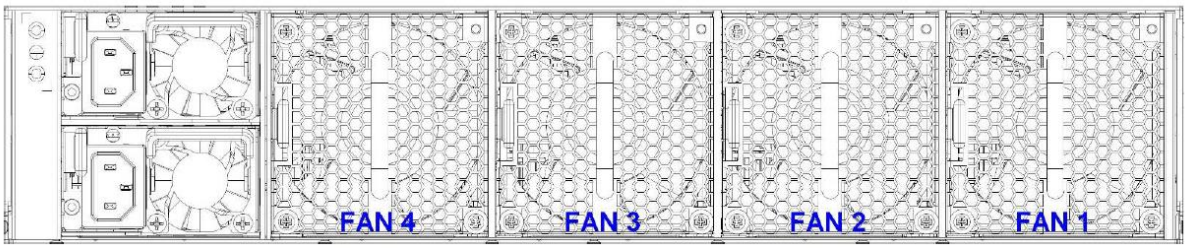

Figure 20: STORDIS BF6064X-T FAN RFU

FAN Module #	Address	Note
FAN-1	0x50	
FAN-2	0x52	
FAN-3	0x51	
FAN-4	0x53	

Table 14: FAN FRU Address

7. PSU SUBSYSTEM

7.1. Overview

- Features
  - Output power: 1300W
  - Input: AC 110V~220V
  - Output: DC 12V/132A; DC standby 12V/2.1A
  - FAN speed: 13200 Rpm
  - Air direction: front to rear
- Power Supply Top View

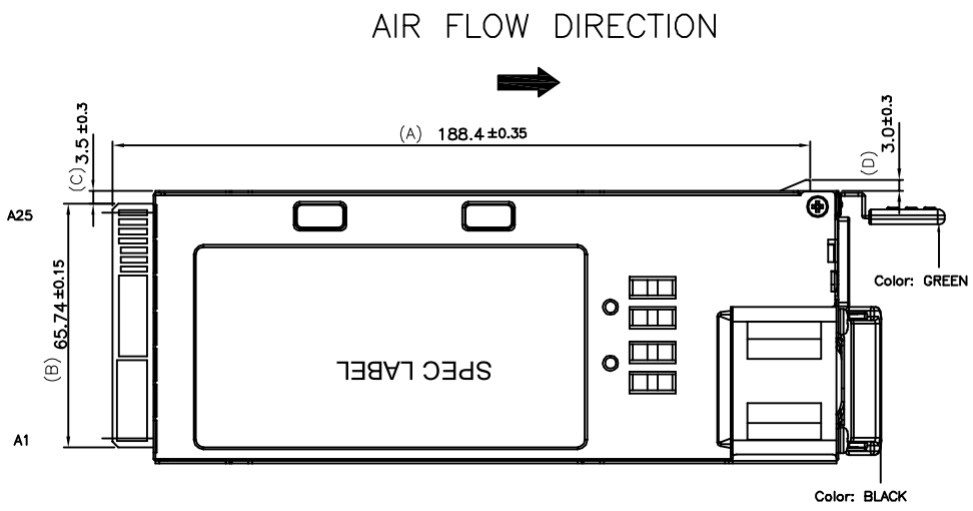

Figure 21: DPS-1300AB-6 D

7.2. PSU FAN Control

PSU controlled registers please refer to [9]

PMBUS protocol

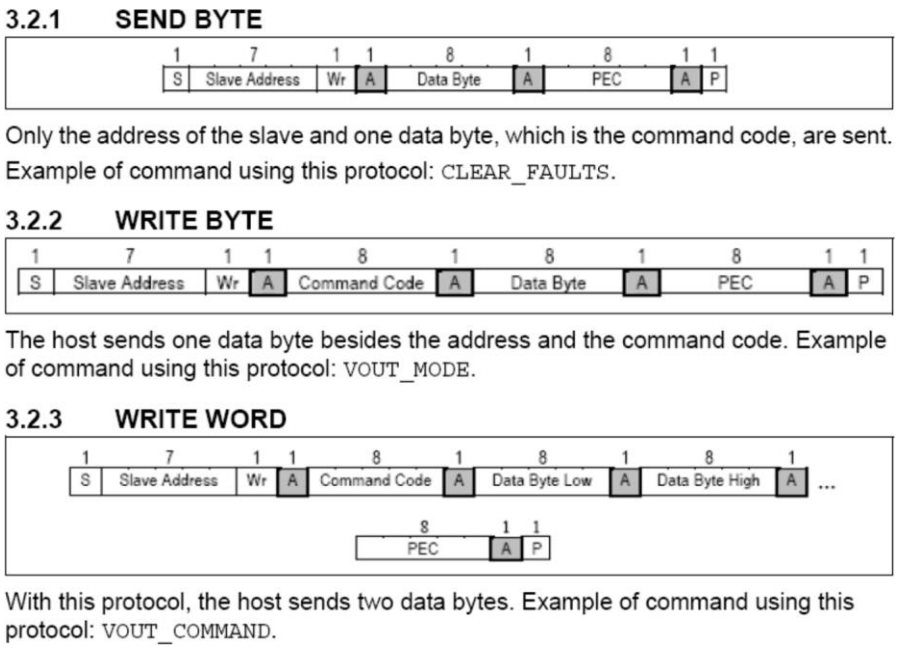

Figure 22: PMbus Protocol

For example:

If it wants to control the PSU FAN speed at 100% operation, there need to input the value as below.

B0/B2_w_3B_64_00_PEC

PSU0 address B2

When operate at 100% duty: B2/3B/64/00/18

When operate at 50% duty: B2/3B/32/00/6A

PSU1 address B0

When operate at 100% duty: B0/3B/64/00/34

When operate at 50% duty: B0/3B/32/00/46

8. MISCELLANEOUS

8.1. I2C

8.1.1. I2C Block diagram

- BMC handle I2C channel 1, 3 and 4 on MB, which can access thermal sensor, PSUs, Fan controller and Fan Tray.
- Intel CPU Handle I2C channel 2, 5 and 6 on MB, which can access CPLDs and QSFP28 I2C control.

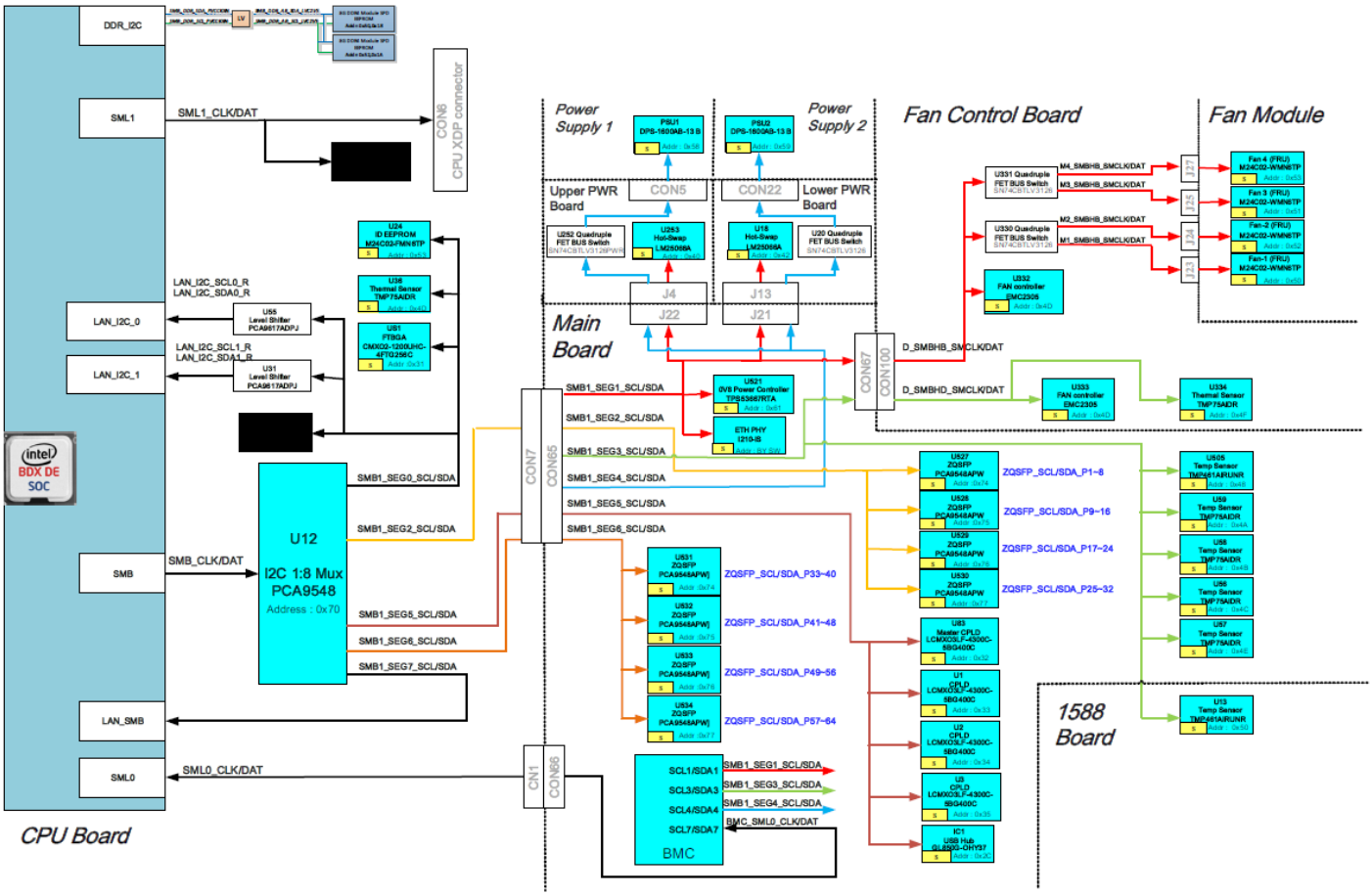

Figure 23: I2C Block Diagram-1

QSFP28 port LEDs are controlled by Tofino. Tofino drives LEDs signal to CPLDs by I2C. CPLDs decode the data then to drive port LEDs.

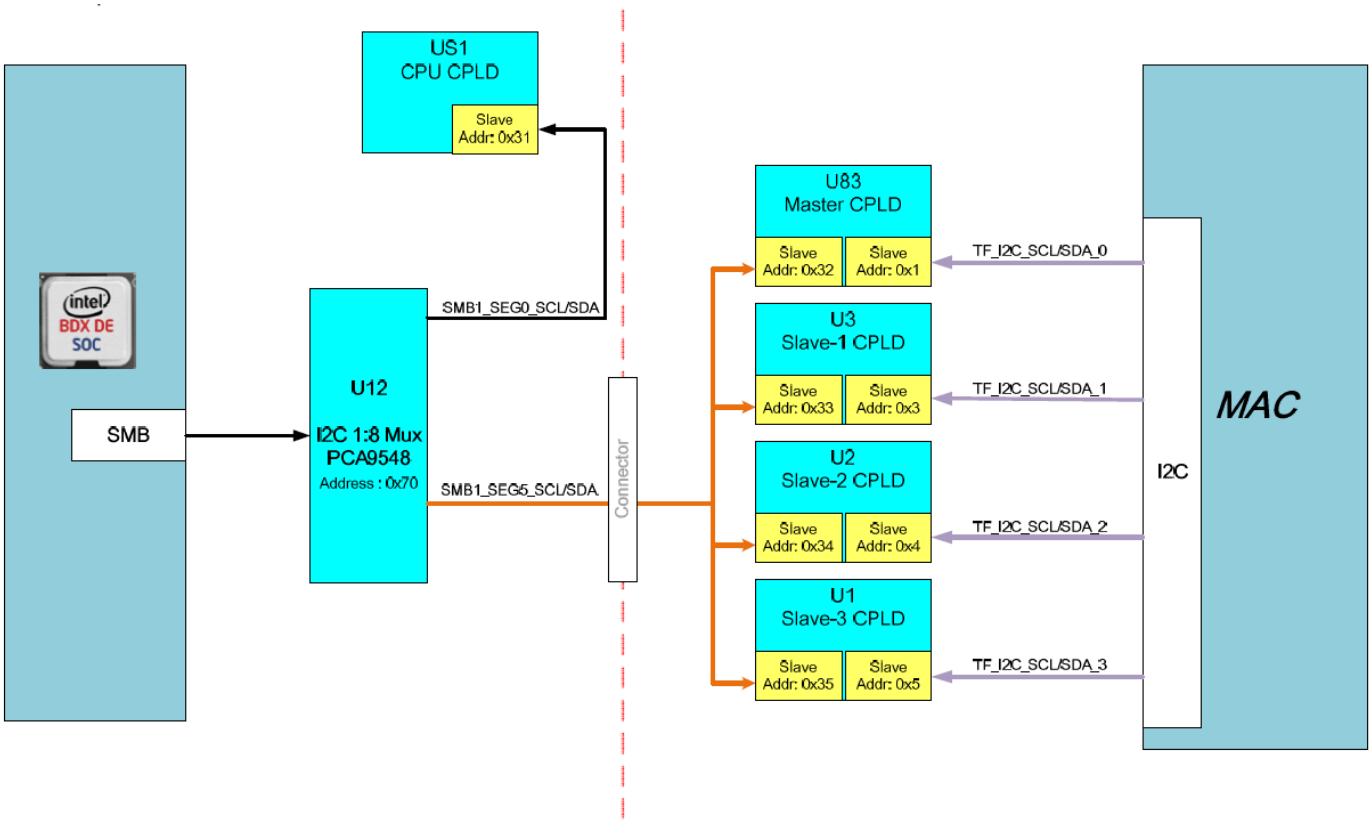

Figure 24: I2C Block Diagram-2

8.1.2. I2C channel table

I2C BUS	COMPONENT	I2C ADDRESS	Location	Note
CPU-SMB	PCA9548	0x70	CPU BD	I2C Extender (8 Channel)
	CPU CPLD	0x31 (CH0)	CPU BD	US1
	Temp Sensor (TMP75)	0x4D (CH0)	CPU BD	U36
	System EEPROM	0x53 (CH0)	CPU BD	U24
BMC	Intel I210	By SW (CH1)	DB	U348
	TPS53667 (VCC_MAC_VDD_0V8)	0x61 (CH1)	MB	U521
	Hot Swap (LM25066A)	0x4D (CH1)	Upper PWR BD	U253
	Hot Swap (LM25066A)	0x42 (CH1)	Lower PWR BD	U18
	FAN Controller (EMC2305)	0x4D (CH1)	Fan Control BD	U332
	Fan-1 EEPROM	0x50 (CH1)	Fan Tray	
	Fan-2 EEPROM	0x52 (CH1)	Fan Tray	
	Fan-3 EEPROM	0x51 (CH1)	Fan Tray	
	Fan-4 EEPROM	0x53 (CH1)	Fan Tray	
CPU-SMB	SN74CBTLV3251PWR_1	0x74 (CH2)	MB	QSFP28 SCL/SDA
	SN74CBTLV3251PWR_2	0x75 (CH2)	MB	QSFP28 SCL/SDA
	SN74CBTLV3251PWR_3	0x76 (CH2)	MB	QSFP28 SCL/SDA
	SN74CBTLV3251PWR_4	0x77 (CH2)	MB	QSFP28 SCL/SDA
BMC	Temp Sensor 1 (TMP461)	0x48 (CH3)	MB	U505 MAC Thermal Sensor 1
	Temp Sensor 2 (TMP75)	0x4A (CH3)	MB	U59 MAC Thermal Sensor 2
	Temp Sensor 3 (TMP75)	0x4B (CH3)	MB	U58 Inlet Thermal 1
	Temp Sensor 4 (TMP75)	0x4C (CH3)	MB	U56 Inlet Thermal 2
	Temp Sensor 5 (TMP75)	0x4E (CH3)	MB	U57 Inlet Thermal 3
	FAN Controller (EMC2305)	0x4D (CH3)	Fan Control BD	U333
	Temp Sensor 6 (TMP75)	0x4F (CH3)	Fan Control BD	U334 Outlet Thermal Sensor
	Temp Sensor 1 (TMP461)	0x50 (CH3)	1588 BD	U13 1588 Controller Thermal Sensor
	PSU1	0x58 (CH4)	PSU	Upper PSU
	PSU2	0x59 (CH4)	PSU	Lower PSU
CPU-SMB	CPLD_1	0x32 (CH5)	MB	U83
	CPLD_2	0x33 (CH5)	MB	U3
	CPLD_3	0x34 (CH5)	MB	U2
	CPLD_4	0x35 (CH5)	MB	U1
	USB Hub (GL850G-OHY37)	0x2C (CH5)	MB	IC1
	SN74CBTLV3251PWR_1	0x74 (CH6)	MB	QSFP28 SCL/SDA
	SN74CBTLV3251PWR_2	0x75 (CH6)	MB	QSFP28 SCL/SDA
	SN74CBTLV3251PWR_3	0x76 (CH6)	MB	QSFP28 SCL/SDA
	SN74CBTLV3251PWR_4	0x77 (CH6)	MB	QSFP28 SCL/SDA

I2C BUS	COMPONENT	I2C ADDRESS	Location	Note
CPU-DDR	DDR4 module1 SPD EEPROM	0x50 0x18	CPU BD	DDR CH0 SPD 0x50 Thermal Sensor 0x18
	DDR4 module2 SPD EEPROM	0x52 0x1A	CPU BD	DDR CH1 SPD 0x52 Thermal Sensor 0x1A

Table 15: I2C Channel Table

8.1.3. QSFP28 I2C channel table

CPU MUX	MB MUX Address	MB MUX Channel	QSFP28 I2C Port #
0x70 (CPU-CH2)	0x74	CH0	QSFP28 SCL/SDA P1
		CH1	QSFP28 SCL/SDA P2
		CH2	QSFP28 SCL/SDA P3
		CH3	QSFP28 SCL/SDA P4
		CH4	QSFP28 SCL/SDA P5
		CH5	QSFP28 SCL/SDA P6
		CH6	QSFP28 SCL/SDA P7
		CH7	QSFP28 SCL/SDA P8
	0x75	CH0	QSFP28 SCL/SDA P14
		CH1	QSFP28 SCL/SDA P13
		CH2	QSFP28 SCL/SDA P16
		CH3	QSFP28 SCL/SDA P15
		CH4	QSFP28 SCL/SDA P10
		CH5	QSFP28 SCL/SDA P9
		CH6	QSFP28 SCL/SDA P12
		CH7	QSFP28 SCL/SDA P11
	0x76	CH0	QSFP28 SCL/SDA P17
		CH1	QSFP28 SCL/SDA P18
		CH2	QSFP28 SCL/SDA P26
		CH3	QSFP28 SCL/SDA P25
		CH4	QSFP28 SCL/SDA P22
		CH5	QSFP28 SCL/SDA P21
		CH6	QSFP28 SCL/SDA P24
		CH7	QSFP28 SCL/SDA P23
	0x77	CH0	QSFP28 SCL/SDA P29
		CH1	QSFP28 SCL/SDA P30
		CH2	QSFP28 SCL/SDA P27
		CH3	QSFP28 SCL/SDA P28
		CH4	QSFP28 SCL/SDA P32
		CH5	QSFP28 SCL/SDA P31
		CH6	QSFP28 SCL/SDA P19
		CH7	QSFP28 SCL/SDA P20

CPU MUX	MB MUX Address	MB MUX Channel	QSFP28 I2C Port #
0x70 (CPU-CH6)	0x74	CH0	QSFP28 SCL/SDA P33
		CH1	QSFP28 SCL/SDA P34
		CH2	QSFP28 SCL/SDA P35
		CH3	QSFP28 SCL/SDA P36
		CH4	QSFP28 SCL/SDA P37
		CH5	QSFP28 SCL/SDA P38
		CH6	QSFP28 SCL/SDA P39
		CH7	QSFP28 SCL/SDA P40
	0x75	CH0	QSFP28 SCL/SDA P47
		CH1	QSFP28 SCL/SDA P48
		CH2	QSFP28 SCL/SDA P41
		CH3	QSFP28 SCL/SDA P42
		CH4	QSFP28 SCL/SDA P43
		CH5	QSFP28 SCL/SDA P44
		CH6	QSFP28 SCL/SDA P45
		CH7	QSFP28 SCL/SDA P46
	0x76	CH0	QSFP28 SCL/SDA P55
		CH1	QSFP28 SCL/SDA P56
		CH2	QSFP28 SCL/SDA P53
		CH3	QSFP28 SCL/SDA P54
		CH4	QSFP28 SCL/SDA P58
		CH5	QSFP28 SCL/SDA P57
		CH6	QSFP28 SCL/SDA P49
		CH7	QSFP28 SCL/SDA P50
	0x77	CH0	QSFP28 SCL/SDA P59
		CH1	QSFP28 SCL/SDA P60
		CH2	QSFP28 SCL/SDA P61
		CH3	QSFP28 SCL/SDA P62
		CH4	QSFP28 SCL/SDA P63
		CH5	QSFP28 SCL/SDA P64
		CH6	QSFP28 SCL/SDA P52
		CH7	QSFP28 SCL/SDA P51

Table 16: QSFP28 I2C Channel Map

8.2. CPLD

For Lattice XO CPLD we used Lattice design software to program HDL. The Lattice II Assembler generates a device programming image, in the form of one or more of the following from a successful fit (that is, place-and-route).

- Programmer Object Files (.pof)
- SRAM Object Files (.sof)
- Hexadecimal (Intel-Format) Output Files (.hexout)
- Tabular Text Files (.ttf)
- Raw Binary Files (.rbf)

The .pof and .sof files are then processed by the Quartus II Programmer and downloaded to the device with the MasterBlaster TM or the ByteBlaster TM II download cable, or the Lattice Programming Unit (APU). The Hexadecimal (Intel-Format) Output Files, Tabular Text Files, and Raw Binary Files can be used by other programming hardware manufacturers that provide support for Lattice devices.

For CPLD program download, we using ByteBlaster TM II download cable through the JTAG interface to download programmer object files (.pof) into CPLD.

CPLD download connector, Single in line pin header

Description	pin
3.3V	1
TDO	2
TDI	3
NC	4
NC	5
TMS	6
GND	7
TCK	8

Table 17: CPLD JTAG Connector Pin List

8.3. QSFP28 Misc Signals

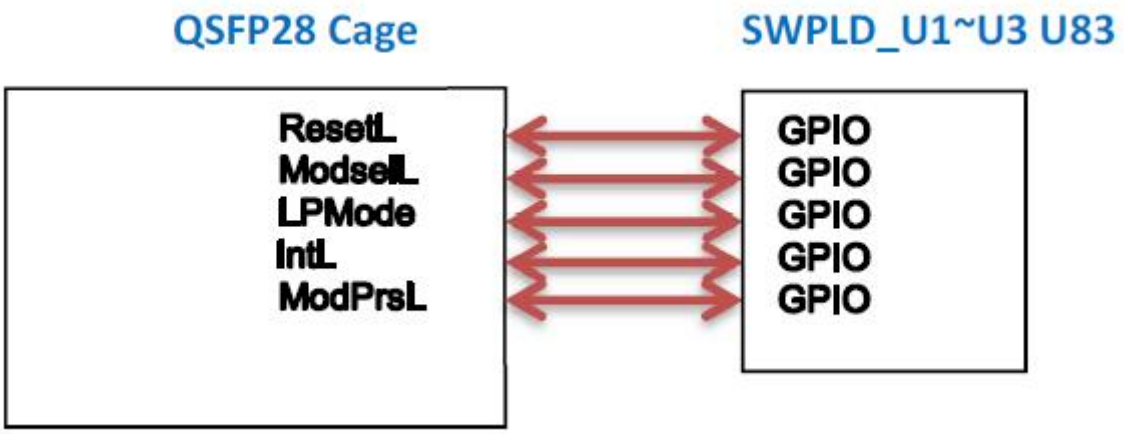

Figure 25: QSFP28 Misc Signals

Pin Name	I/O	Function Description
ModselL	I	Module Select: When held low by the PLD, the module responds to 2-wire serial communication commands. When the ModSelL is High, the module does not respond to or acknowledge any 2-wire interface communication from the host
ResetL	I	Module Reset: When PLD set a low level on the ResetL pin for longer than the minimum pulse length initiates a complete module reset, returning all user module settings to their default state.
LPMode	I	Low Power Mode: The module will be in low power mode if the LPMode pin is in the high state and in high power mode if the LPMode pin is in the low state.
IntL	O	Interrupt: IntL is an output pin. Low indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to host supply voltage on the host board.
ModPrsL	O	Module Present: The ModPrsL is asserted low when the module is inserted and de-asserted high when the module is physically absent from the host connector.

Table 18: QSFP28 Misc Signals

8.4. LED

8.4.1. System LED

Feature	Detailed Description	Comment
Power 1 LED	**Solid Green** – Power Supplier 1 is supplied to the switch & operating normally **Solid Amber** –Power Supplier 1 failed **Off** – Power is Disconnected	At front
Power 2 LED	**Solid Green** – Power Supplier 2 is supplied to the switch & operating normally **Solid Amber** –Power Supplier 2 failed **Off** – Power is Disconnected	At front
System LED	**Solid Green** – Normal operation **Blinking Green** – Booting progress **Solid Amber** – System failed **Off** – No Power	At front
FAN Status LED	**Solid Green** – FAN operating normally **Solid Amber** – FAN failed	At front

8.4.2. MGMT and SYNC Port LED

Feature	Detailed Description	Comment
Management Port	**Link LED**: (on the left side) **Off** –No link is established on the port **Solid Amber** - A valid link at 10/100Mbps is established on the port **Solid Green** – A valid link at 1000Mbps is established on the port **Act LED**: (on the right side) **Off** –No link is established on the port **Blinking Green** – Activity, transmitting or receiving packet at this port	At front

8.4.3. PSU LED

Feature	Detailed Description	Comment
PSU LED	**Solid Green** – Output ON and OK **Solid Amber** – AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power **Solid Amber** – AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power	At rear

8.4.4. FAN LED

Feature	Detailed Description	Comment

FAN Status LED	**Green** – FAN operating normally **Red** – FAN failed	At rear

8.4.5. QSFP28 Port LED Programming

Feature	Detailed Description	Comment
100G QSFP28 slots four LEDs per Port	**LED1**: (Solid Lighting – Linkup, Blinking – Activity) **Green** –100G Operation **White** – 50G Operation **Amber** – 40G Operation **Blue** – 25G Operation **Purple** – 10G Operation **Off** – No Link **LED2**: (Solid Lighting – Linkup, Blinking – Activity) **Blue** – 25G Operation **Purple** – 10G Operation **Off** – No Link **LED3**: (Solid Lighting – Linkup, Blinking – Activity) **White** – 50G Operation **Blue** – 25G Operation **Purple** – 10G Operation **Off** – No Link **LED4**: (Solid Lighting – Linkup, Blinking – Activity) **Blue** – 25G Operation **Purple** – 10G Operation **Off** – No Link	At front

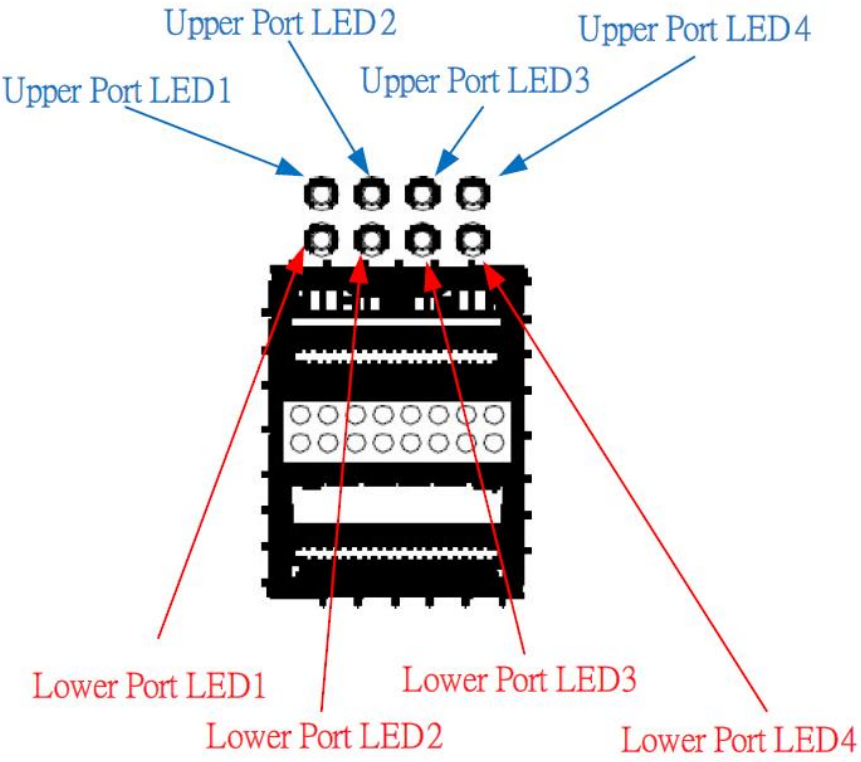

Figure 26: QSFP28 Port LED Indicator

8.5. Power

8.5.1. Power Consumption

The following table shows STORDIS BF6064X-T power consumption.

Power Dissipations of 64*100G Switch with Broadwell CPU , D-1548																		
Device	*Qty*	Current pereach Voltage Rail								Total per each Voltage Rail								*Subtotal*
		VDD 0.8V	AVDD 0.9V	1.0V	1.8V	2.5V	*3.3V*	*5V*	*12V*	0.80	0.90	1.00	1.80	2.50	3.30	5.00	12.00	
CPU Board,Broadwell (8core)	1								8,082	0	0	0	0	0	0	0	8,082	96.98
Barefoot 10k Series	1	311,250	83,333			120				311,250	83,333	0	0	120	0	0	0	324.30
Intel I210	1						400			0	0	0	0	0	400	0	0	1.32
CPLD LCMXO3LF-4300C	4						300			0	0	0	0	0	1,200	0	0	3.96
USB Port	1							800		0	0	0	0	0	0	800	0	4.00
QSFP28 (5W)	65						1,515			0	0	0	0	0	98,475	0	0	324.97
LED	260						31			0	0	0	0	0	8,060	0	0	26.60
FAN	4								6,360	0	0	0	0	0	0	0	25,440	305.28
Other (ICs, OSCs,...)	1						1,000			0	0	0	0	0	1,000	0	0	3.30
Load Total Current per Voltage [A]:										311.25	83.333	0.00	0.00	0.12	109.14	0.80	33.52	
Load Power Dissipation per Voltage [W]:										249.00	75.00	0.00	0.00	0.30	360.15	4.00	402.26	1090.71
DCDC EF (85%)										43.94	13.23	0.00	0.00	0.05	63.55	0.71		121.48
PWM Input [W]										292.94	88.23	0.00	0.00	0.35	423.69	4.71	402.26	1212.18
Total power comsuption (include efficiency of PWM) [W]:										1212.18								

Table 19: System Power Consumption

8.5.2. Power Distribution

Detail Power Distribution shows as the following figure.

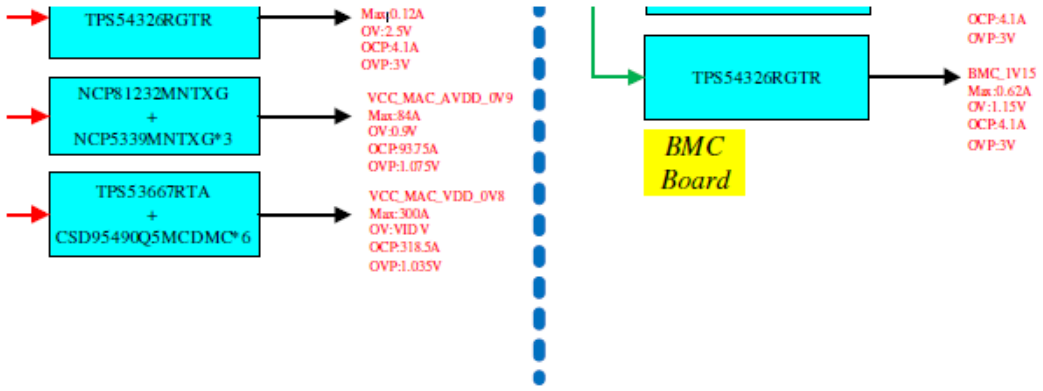

Figure 27: System Power Distribution

8.6. Clock Distribution

8.6.1. System Clock

The following figure shows STORDIS BF6064X-T system clock distribution.

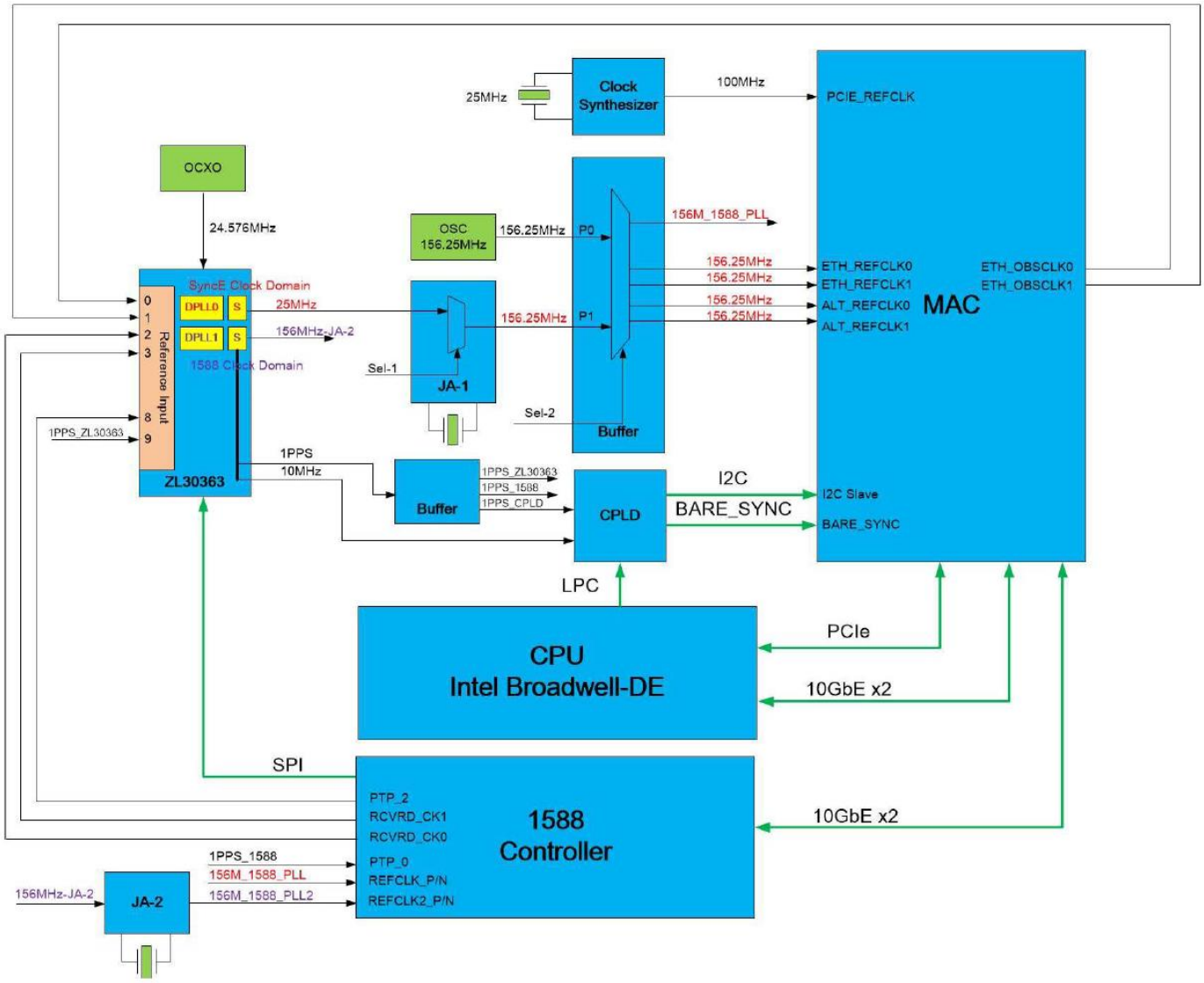

Figure 28: System Clock Distribution

8.6.2. SyncE Clock

On Tofino SDE environment, user can use Command String to let Tofino bring out the SerDes receive clocks from any lane for Synchronous Ethernet applications.

The Command String comprise 2 parts (Command A & Command B), the introduction is shown as below.

Command A	**Note :**
reg_wr 00xXXXFD20 0x00000010	**Indicate Lane N as SerDes. XXX=$(257+2*N)_{16}$**

Command B	**Note :**
reg_wr 0 0x00040004 0x0000003F	**Indicate Lane 0 ~ 7 or 40 ~ 63, Clock is divided 8**
reg_wr 0 0x00040004 0x0000013F	**Indicate Lane 8 ~ 39 or 64, Clock is divided 8**

e.g.

If user wants to get lane 8 SerDes clock dividing by 8 for Synchronous Ethernet applications. The Command String should be enter as below.

reg_wr 0 0x111FD20 0x00000010

reg_wr 0 0x00040004 0x0000013F

P.S. **XXX=$(257+2*8)_{16}$ =111**

9. Physical Design

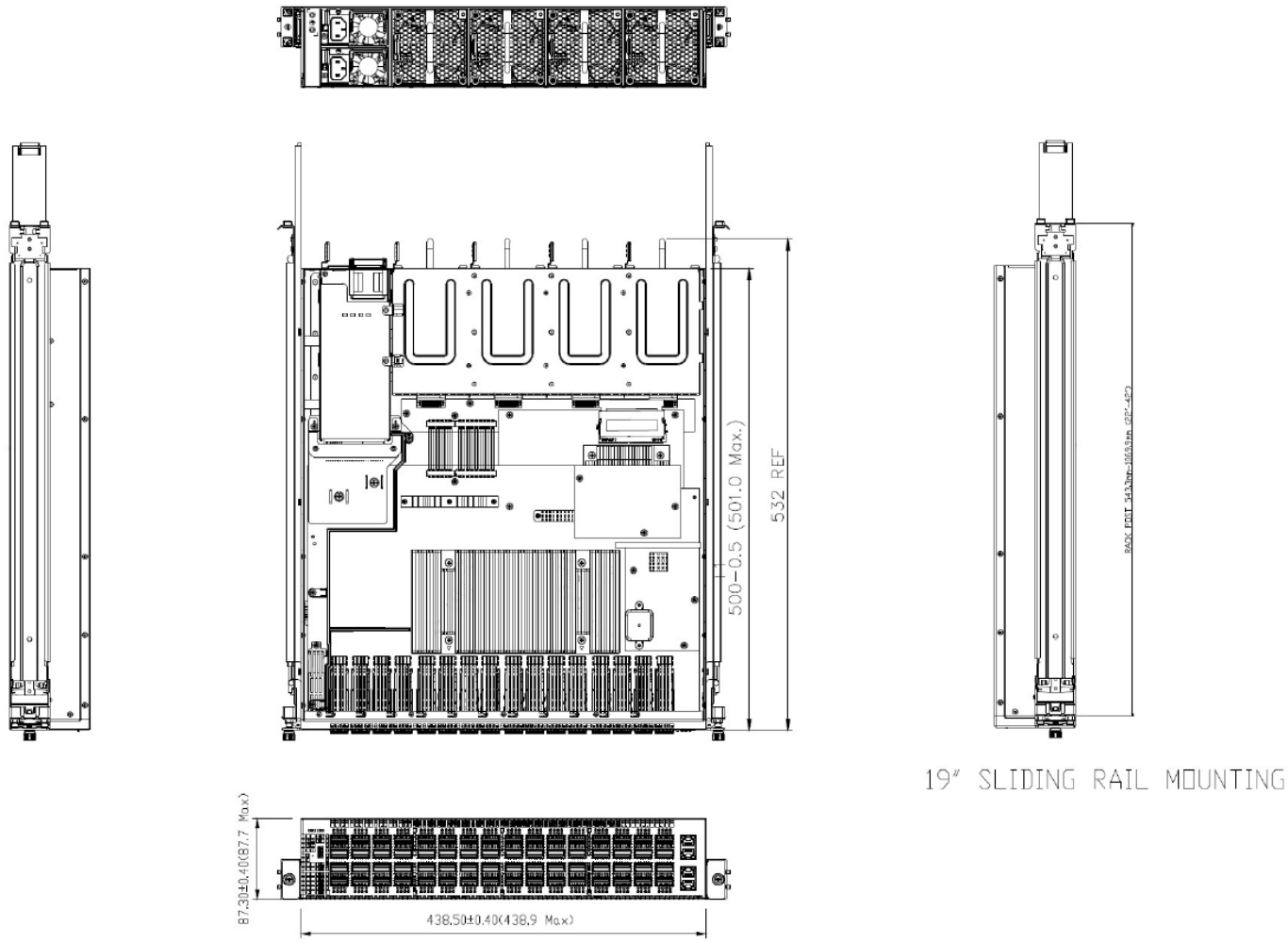

Figure 29: System Outline Overview

10. Environment

- Operating temperature of 0 to 40C
- Storage temperature of -20 to 70C
- Operational relative humidity of 10 to 90%
- Storage relative humidity of 10 to 90%
- ROHS 6 Compliance
- Non-Operational Temperature Limits: -40 to 65C (-40 to 149F)
- Non-Operational Humidity Limits: 10% to 90% RH with 33C (91F) maximum.