

Alpha Networks Inc

SNX-60x0-486T

48-port 10G BASE-T & 2-port 40G QSFP+ + 4-port 100G QSFP28 Switch (ToR/Aggregation Switch)

Author: Alex Chen, Chloe Lin



Revision History

Version	Revised Date	Author	Content Revised
0.1	16/01/16	Alex Chen	Initial Version
0.2	26/01/16	Alex Chen	Fixed invalid link
0.3	03/02/16	Alex Chen	Fixed typo



Scope

This documents defines the technical specification for SNX-60x0-486T used in the Open Compute Project as 10G Top of the Rack (ToR) or as an aggregation switch

Contents

Revis	sion History	2
Over	view	6
Licer	ıse	6
1	Feature Highl	ights8
2	Physical Over	view9
	2.1	Mechanical Dimension9
	2.2	Top View10
	2.3	Front View10
	2.4	Rear View11
3	LED Definition	n11
4	Field Replace	able Components13
	4.1	Power Supply Modules13
	4.2	Fan Modules16
5	System Overv	<i>r</i> iew18
	5.1	Main PCB18
	5.1	CPU Subsystem20
		5.1.1 Intel CPU (C2558)20
		5.1.1.1 DDR3 SDRAM26
		5.1.1.2 PCIe Interface26
6	IO and Conne	ectors



7

ን ተ ፕ		Open Compute Project Alpha Networks SNX-60x0-486T Specification v0.6				
	6.1	RS232 Interface	26			
	6.2	Management Ethernet Interfaces	26			
	6.3	USB Interface	26			
I	ower/Envir	onmental/Agency Certifications	27			

List of Figures

Figure 1: SNX-60x0-486T Chassis dimension	9
Figure 2: SNX-60x0-486T top view	.10
Figure 3: SNX-60x0-486T front view	.11
Figure 4: SNX-60x0-486T rear view	.11
Figure 5: Power Supply Mechanical specification	.15
Figure 6: Fan module mechanical specification	.18
Figure 7: Main board block diagram	.19

List of Tables

Table 1: LED behavior for system	12
Table 2: LED behavior for Port 1~48 10G Ethernet Port	12
Table 3: LED behavior for Port 49~50 40G, 51~54 100G Ethernet Port	13
Table 4: Power supply LED definition	13
Table 5: Power supplies usage	14
Table 6: Power supply connector pin out	14
Table 7: LED definition on power supply	15
Table 8: Power Supply EEPROM FRU data format	16
Table 9: Fan Modules part number	17



Open Compute Project Alpha Networks SNX-60x0-486T Specification v0.6
Table 10: Fan Modules connector pin out17
Table 11: PCBs for SNX-60x0-486T18
Table 12: CPU subsystem key Components20
Table 13: Intel CPU module connector pin out23
Table 14: Intel CPU module connector Pin Definitions 25
Table 16: Power consumption and environment table
Table 16: Regulatory Standards Compliance table



Overview

The SNX-60x0-486T Series Data Center, Top-of-Rack (ToR)/aggregation switches, with a total combined bandwidth of 960 Gbps, feature 48 ports of 10 Gbps, 2 ports of 40 Gbps and 4 ports of 100 Gbps Ethernet wire-speeds. The Layer 3 capable, bare metal system also provides an RJ-45 console port and an Out-Of-Band (OOB) management port. It also provides a micro USB interface in the front panel for the administrators to upgrade code by using an extended cable.

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Items		Detailed Description		
MAC Controller		BCM56860*1		
PHY for 10G		BCM84868*12 or BGM84858*12		
PHY for 100G		BCM82792*2		
10G NIC		BCM57810S*1 (Optional)		
		CPU Subsystem		
	CPU	Intel Rangeley C2558 4 Cores/2.4GHz		
Modular CPU board	RAM	DDR3 4GB for Intel Rangeley CPU (reserved up to 32G)		
	Flash	SSD 16GB for Intel Rangeley CPU (reserved up to 64G)		
	Boot Flash	8MB for Intel Rangeley CPU (reserved up to 16MB)		
PHY for CPU Management Port		MVL88E1112*1		



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1 Feature Highlights

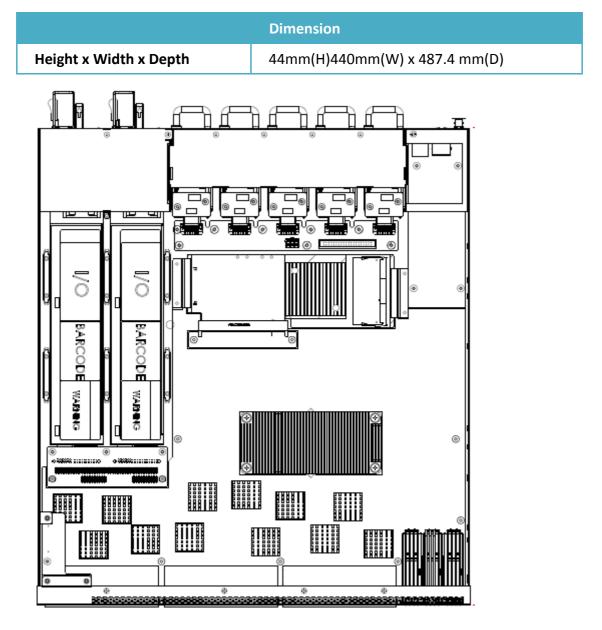
The SNX-60x0-486T Series Data Center, leaf/ToR switches, with a total combined bandwidth of 960 Gbps, feature 48 ports of 10 Gbps RJ-45, 2 ports of 40 Gbps QSFP+ and 4 ports of 100Gbps QSFP28 at Ethernet wire-speeds. The Layer 3 capable, bare metal system also provides a RJ-45 and micro USB console port, an Out-Of-Band (OOB) management port using RJ-45 and an USB type A port for storage.

- OCP micro server modular CPU board with large flash and memory
- Temperature warning
- Software-readable thermal monitor
- Real time clock (RTC) support
- Two Hot-swappable redundant power supply
- Four redundant (4+1) fan modules
- The following are supported
- Front panel
 - One Reset Button
 - One Locator LED
 - Micro USB console port
- Rear panel
 - One Out-Of-Band (OOB) 10/100/1000 Mbps RJ-45 management port
 - One RJ-45 type console port
 - One USB (Type A) port for storage device
 - Two BNC ports for IEEE 1588 clock sync (Optional)



2 Physical Overview

2.1 Mechanical Dimension

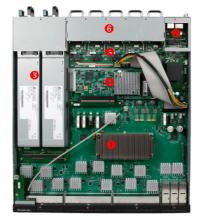


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Figure 1: SNX-60x0-486T Chassis dimension



2.2 Top View



- 1: Main Board
- 2: Management board
- **3**: PSU modules
- (4): Micro server CPU module
- **6**: Fan extender
- **6**: Fan modules

Figure 2: SNX-60x0-486T top view

2.3 Front View



- Reset button
 Micro USB console port
 : 48* 10G Base-T ports
- 2* 40G QSFP+ ports
 3: 4* 100G QSFP28 ports



Figure 3: SNX-60x0-486T front view

2.4 Rear View



- Hot swappable fan modules
- **2**: Hot swappable power supply
- 3: Console Port

: BMC port

(5) : Type A USB storage port

- **(b)** : Out of band management port
 - 1588 BNC port Design Reserved

Figure 4: SNX-60x0-486T rear view

3 LED Definition

The following table defines the per device LEDs' behaviors:

Items	LED Indication	Color	Behavior	Description
1		Blue	Blinking	Locator function is enable
1	Locator	ыце	Off	Locator function is disable
			Solid Light	POST Passed, normal operation
		Green	Blinking	POST in progress
2	STAT		Light off	System No power
		Amber	Blinking	POST failed or overheat or power supply failed or Fan module fail or over temperature
	MGMT		Solid Light	Link up
3		Green	Blinking	Packet transmitting or receiving
			Light off	No link up or port disable



4	FAN 1 FAN 2	Green	Solid Light	All diagnostics pass. The module is operational.
	FAN 3 FAN 4	Green	Off	The module is not receiving power
	FAN 5	Amber	Blinking	Failure
	PWR (P1, P2)	Green	Solid Light	Power On
5			Off	Power Off and no power attached
	Amber		Blinking	Power supply failures, over voltage, over current, over temperature

Table 1: LED behavior for system

The following defines the 10G BASE-T Ethernet port LEDs' behaviors:

Location	Speed	LED Indication	Color	Behavior	Descriptio n
	10G bps(high speed) LED	Link/Act	Green	Solid Light	The port has a link and is operating at 10Gbps
	LED			Blinking	
LED Port 1~48	Lin 5, 2.5,1 G bps(low speed)		Amber	Solid Light	The port has a link and is operating at 5/2.5/1Gbps
				Blinking	The port is sending or receiving data at 5/2.5/1Gbps
	Off			Light off	Link down or no link

Table 2: LED behavior for Port 1~48 10G Ethernet Port

The following table defines the 40G & 100G QSFP28 Ethernet port LEDs' behaviors:

Location	Speed	LED Indication	Color	Behavior	Description
LED number	40G Link/	Link/Act/Speed	Green	Solid Light	When there is a secure 40G connection (or link)
49~56 in group of 4 (40Gbps)				Blinking	Packet transmitting or receiving
				Light off	No link up or port disable
LED number	100G	Link/Act/Speed	Green	Solid Light	When there is a secure 100G



57~72, group of 4					connection (or link)
4				Blinking	Packet transmitting or receiving
	40G	Amber	Solid Light	When there is a secure 40G connection (or link)	
				Blinking	Packet transmitting or receiving
	Off			Light off	No link up or port disable

Table 3: LED behavior for Port 49~50 40G, 51~54 100G Ethernet Port

Each power supply module has a bi-color LED, which behavior is descript in the following:

LED Color	Behavior	Description
	Solid Light	Output ON and OK
Green	Blinking	AC present / AC Line 12VSB Holdup
	Light off	No AC power to all power supplies
	Solid Light	Power supply critical event causing a shutdown; failure, Fan Fail
Amber Blinking		Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.

Table 4: Power supply LED definition

4 Field Replaceable Components

4.1 Power Supply Modules

The switch is powered through one or two internal power supply modules.

Supported power supply modules:

- AC-770-12-FB
- AC-770-12-BF
- DC-1100-12-FB
- DC-1100-12-BF

The switch requires only one power supply for its operations, but you can include a second one for redundancy. By default the switch is installed one power supply in the second power supply slot, and filled the first slot with a filler panel. You can order



extra power supplies with forward airflow or reverse airflow. Be sure to order the same direction of airflow as is used with the switch. Never leave a power supply slot empty. Please fill the slot with a filler panel.

Please refer to Table 5 for the recommended power supply usage for each switch model.

Switch Model Number	Equipped CPU Model	Power Supply Vender	Power Supply Model Number	Minimum Number of Power Supply Need
SNX-60X0-486T-AF-B	Intel Rangely C2558	tel Rangely C2558 Delta Electronics		1
SNX-60X0-486T-AB-B Intel Rangely C2558		Delta Electronics	AC-770-12-BF	1
SNX-60X0-486T-DF-B Intel Rangely C2558		Delta Electronics	DC-1100-12-FB	1
SNX-60X0-486T-DB-B Intel Rangely C2558		Delta Electronics	DC-1100-12-BF	1

Table 5: Power supplies usage

Power Supply connector: Molex 45984-4343

Pin #	Descriptin	Pin #	Descriptin3
S1	+12VRS+	S13	N/A
S2	+12VRS-	S14	SGND
S3	12LS	S15	AO
S4	SMB ALERT	S16	N/A
S5	SDA	S17	Vs
S6	SCL	S18	N/A
S7	PSKILL	S19	N/A
S8	PSON	S20	N/A
S9	PWOK	S21	N/A
S10	A1	S22	N/A
S11	5VSB	S23	+5VSB
S12	5VSB	S24	+5BSB
P1	+12_VOUT	Р3	GND
P2	+12_VOUT	P4	GND

Table 6: Power supply connector pin out

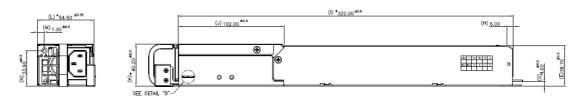




Figure 5: Power Supply Mechanical specification

LED definition on power supply

Power Supply Condition	LED Status	
PSU is switched on and is running (Output ON and OK)	Green	
No AC power to all power supplies or PSU is ON but with warning events	Off	
PSU is OFF but 5VSB is on	1Hz on Blink Green	
PSU critical event causing a shutdown: failure, OCP, OTP, OVP, UVP, Fan Fail	Amber	
PSU warning events: high temp, high power, high current, slow fan, under input voltage	1Hz on Blink Amber	

Table 7: LED definition on power supply

FRU

FRU data format compliant with IPMI ver 1.0 (per rev 1.1 from Sept. 25, 1999) specification. The FRU device will implement the same protocols as the commonly used AT24C02 device, including the Byte Read, Sequential Read, Byte Write and Page Read protocols.

The EEPROM content is as following

Area Type	Description		
Common Header	Format Version Number		
Internal Use Area	Not required, do not reserve		
Chassis Info Area	Not applicable, do not reserve		
Board Info Area	Not applicable, do not reserve		
Product Info Area	As defined by the IPMI FRU document.		
Product into Area	Product information is defined as following		
Field name	Field Description		
Manufacturer Name	{Formal name of manufacturer}		
Product Name	{Manufacturer's model number}		
Product part/model number	Customer part number		
Product Version	Customer current revision		
Product Serial Number	{Defined at time of manufacture}		
Asset Tag	{Not used, code is zero length byte}		
FRU File ID	{Not required}		
PAD Bytes	{Added as necessary to allow for 8-bype offset to next		



	area}		
	As defined by the IPMI FRU documentation. The		
	following information shall be used by this power		
	supply:		
Mulit-Record Area	Power Supply Information (Record type 0x00)		
	DC Output (Record Type 0x01)		
	No other record types are required for power supply		
	Multi-Record information shall be defined as following		
Field Name (PS Info)	Field Information Definition		
Overall Capacity (watts)	770		
Peak VA	770		
Inrush current (A)	40		
Inrush interval (msec)	5		
Low end input voltage range 1	100		
High end input voltage range 1	127		
Low end input voltage range 2	200		
High end input voltage range 2	240		
Low End Input Frequency	47		
Range	47		
High End Input Frequency	63		
Range	05		
Holdup Time (msec)	12		
Binary flags	Set for: Hot Swap support, Auto switch and PFC		
Peak Wattage	839 Watts		
Peak Wattage Time in seconds	12		
Combined wattage	770		
Predictive fail tach support	Supported		
Field Name (Output)	Field Description : Two output are to be defined from		
Field Name (Output)	#1 to #2, as follows: +12V and +5VSB		
Output Information	Set for: Standby on +5VSB, no 5VSB on all others		
All other output fields	Format per IPMI specification , using parameters in		
	this specification		

Table 8: Power Supply EEPROM FRU data format

4.2 Fan Modules

The SNX-60x0-486T supports up to 5 fan modules. For front to rear and rear to front



air flow, different types of fan modules are required.

Air Flow Direction	Part Number
Front to Rear	AVC DFTA0456B2UP057
Rear to Front	AVC DFTA0456B2UP058

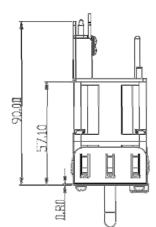
Table 9: Fan Modules part number

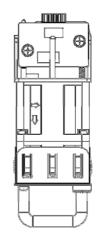
Fan module connector: LCU SM401V-20P

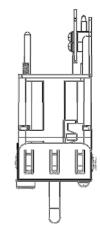
#	NAME	Description	#	NAME	Description
1	FAN_CON_TACH_0	FAN tachometer 0	11	FAN_DIR	FAN Direction
2	GND	GND	12	GND	GND
3	FAN_12VIN	12V	13	FAN_12VIN	12V
4	FAN_CON_PWM_0	PWM control for FAN0	14	EE_GND	EEPROM GND
5			15	EE_SDA	EEPROM SDA
6	EE_SCL	EEPROM SCL	16	EE_VDD	EEPROM VDD
7	EE_A0	EEPROM ADDR_0	17	FAN_CON_PWM_1	PWM control for FAN1
8	FAN_12VIN	12V	18	FAN_12VIN	12V
9	GND	GND	19	GND	GND
10	FAN_PRESENT#	Exist FAN module	20	FAN_CON_TACH_1	FAN tachometer 0

Table 10: Fan Modules connector pin out









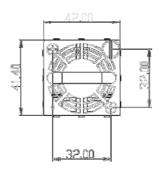


Figure 6: Fan module mechanical specification

5 System Overview

The SNX-60x0-486T comprised of the following PCB

PCB Function	PCB Layer	Dimension (mmxmm)
Main board	14	431*326.3
FAN module	2	38.5*29
FAN Adapter	2	228*30
LED board	2	50*91.5
PCIE Adapter	4	135.5*16
PSU Adapter	4	132.4*41.3
CPU board	12	210*73.8
Management board	4	58*180

Table 11: PCBs for SNX-60x0-486T

5.1 Main PCB

The main PCB is a 12 layer PCB where the switch MAC resides. It also supports the



following functions:

- Networking I/O ports
- Management ports
- LED
- Connectivity to power supply and fan
- Power conversion circuit
- Etcs

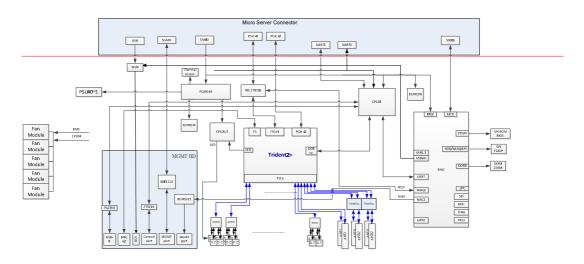
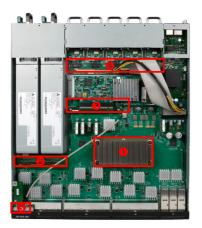


Figure 7: Main board block diagram



0: MAC BMC56860

- 2: Power supply connector
- Connector for CPU module
- **4**: Fan module connector
- G: MGMT board



Figure 8: Main PCB top view

5.1 CPU Subsystem

The following Table is the list of key components used in SNX-60x0-486T

Items		Detailed Description	
Intel			
	CPU	Intel Rangeley C2558 4 Cores/2.4G	
Modular CPU	RAM	DDR3 4GB for Intel Rangeley CPU	
board (Option 2)	Flash	SSD 8GB for Intel Rangeley CPU	
	Boot Flash	8MB for Intel Rangeley CPU	

Table 12: CPU subsystem key Components

5.1.1 Intel CPU (C2558)

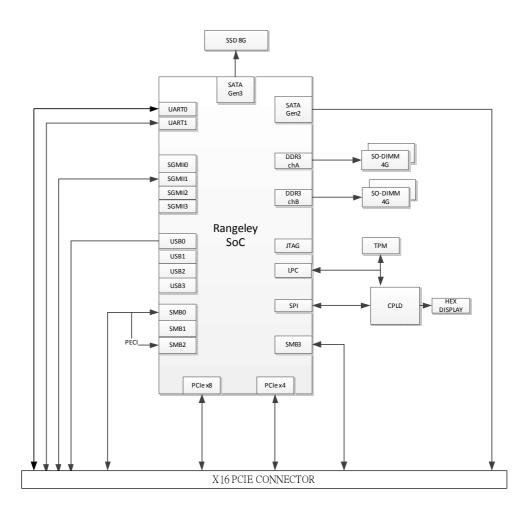


Figure 9: Intel CPU board block diagram



Intel CPU module connector: x16 PCIe Edge Connector

For 80	For 80 PIN connector			
#	Pin Name	#	Pin Name	
B1	P12V	A1	PRSNT#	
B2	P12V	A2	P12V	
B3	P12V	A3	P12V	
B4	GND	A4	GND	
B5	I2C_SCL	A5	RFU	
B6	I2C_DATA	A6	RFU	
B7	GND	A7	COM_TX	
B8	PWR_BTN#	A8	COM_RX	
B9	USB_P	A9	GE0_MDC	
B10	USB_N	A10	GE0_MDIO	
B11	SYS_RESET#	A11	PCIE0_RESET#	
		KEY		
B12	I2C_ALERT#	A12	GND	
B13	GND	A13	PCIE0_REFCLK_P	
B14	GND	A14	PCIE0_REFCLK_N	
B15	PCIE0_TX0_P	A15	GND	
B16	PCIE0_TX0_N	A16	GND	
B17	GND	A17	PCIE0_RX0_P	
B18	GND	A18	PCIE0_RX0_N	
B19	PCIE0_TX1_P	A19	GND	
B20	PCIE0_TX1_N	A20	GND	
B21	GND	A21	PCIE0_RX1_P	
B22	GND	A22	PCIE0_RX1_N	
B23	PCIE0_TX2_P	A23	GND	
B24	PCIE0_TX2_N	A24	GND	
B25	GND	A25	PCIE0_RX2_P	
B26	GND	A26	PCIE0_RX2_N	
B27	PCIE0_TX3_P	A27	GND	
B28	PCIE0_TX3_N	A28	GND	
B29	GND	A29	PCIE0_RX3_P	
B30	GND	A30	PCIE0_RX3_N	
B31	UARTO_TXD	A31	GND	
B32	UARTO_RXD	A32	GND	
B33	GND	A33	RFU	
B34	GND	A34	RFU	
B35	PCIE1_REFCLK_P	A25	GND	
B36	PCIE1_REFCLK_N	A36	GND	
B37	GND	A37	RFU	
B38	GND	A38	RFU	



B39	PCIE1 RESET#	A39	GND
B40	 RFU	A40	GND
B41	GND	A41	RFU
B42	GND	A42	NIC_SMBUS_ALERT#
B43	NIC_SMBUS_SCL	A43	GND
B44	NIC_SMBUS_SDA	A44	GND
B45	GND	A45	GE0_RX_P
B46	GND	A46	GE0_RX_N
B47	GE0_TX_P	A47	GND
B48	GE0_TX_N	A48	GND
B49	GND	A49	RFU
B50	GND	A50	RFU
B51	RFU	A51	GND
B52	RFU	A52	GND
B53	GND	A53	RFU
B54	GND	A54	RFU
B55	RFU	A55	GND
B56	RFU	A56	GND
B57	GND	A57	RFU
B58	GND	A58	RFU
B59	RFU	A59	GND
B60	RFU	A60	GND
B61	GND	A61	RFU
B62	GND	A62	RFU
B63	RFU	A63	GND
B64	RFU	A64	GND
B65	GND	A65	PCIE1_RX0_P
B66	GND	A66	PCIE1_RX0_N
B67	PCIE1_TX0_P	A67	GND
B68	PCIE1_TX0_N	A68	GND
B69	GND	A69	PCIE1_RX1_P
B70	GND	A70	PCIE1_RX1_N
B71	PCIE1_TX1_P	A71	GND
B72	PCIE1_TX1_N	A72	GND
B73	GND	A73	PCIE1_RX2_P
B74	GND	A74	PCIE1_RX2_N
B75	PCIE1_TX2_P	A75	GND
B76	PCIE1_TX2_N	A76	GND
B77	GND	A77	PCIE1_RX3_P
B78	GND	A78	PCIE1_RX3_N
B79	PCIE1_TX3_P	A79	GND
B80	PCIE1_TX3_N	A80	GND
B81	GND	A81	P12V
B82	GND	A82	P12V



Table 13: Intel CPU module connector pin out

Intel CPU module pin definitions

#	Pin	Direction (from CPU	Required/ Configurable	Pin Definition
		side)		
	P12V	Input	Required	12 V-AUX power
	I2C_SCL	Input/Output	Required	I2C clock signal. I2C is the primary sideband interface for server management functionality. 3.3 VAUX signal. Pull-up is provided on the baseboard.
	I2C_SDA	Input/Output	Required	I2C data signal. I2C is the primary sideband interface for server management functionality. 3.3 VAUX signal. Pull-up is provided on the baseboard.
	I2C_ALERT#	Output	Required	I2C alert signal. Alerts the Baseboard Management Controller (BMC) that an event has occurred that must be processed. 3.3 V-AUX signal. Pull-up is provided on the baseboard.
	NIC_SMBUS_SCL	Input/Output	Required	Dedicated SMBus clock signal for network traffic between the BMC and the NIC. 3.3 V-AUX signal. Pullup is provided on the baseboard.
	NIC_SMBUS_SDA	Input/Output	Required	Dedicated SMBus data signal for network traffic between the BMC and the NIC. 3.3 V-AUX signal. Pullup is provided on the baseboard.
	NIC_SMBUS_ALERT#	Output	Required	Dedicated SMBus alert signal for network traffic between the BMC and the NIC. 3.3 V-AUX signal. Pullup is provided on the baseboard.
	PWR_BTN#	Input	Required	Power on signal. When driven low, it indicates that the server will begin its power-on sequence. 3.3 VAUX signal. Pull-up is provided on the baseboard. If PWR_BTN# is held low for



			< 4 seconds, then this indicates a soft (graceful power off. Otherwise, a hard shutdown is initiated.
SYS_RESET#	Input	Required	System reset signal. When driven low, it indicates that the server will begin its warm reboot process. 3.3 V-AUX signal. Pull-up is provided on the baseboard.
PRSNT#	Output	Required	Present signal. This is pulled low on the card to indicate that a card is installed. 3.3 V-AUX signal. Pull-up is provided on the baseboard.
COM_TX	Output	Required	Serial transmit signal. Data is sent from the micro-server module to the BMC. 3.3 V-AUX signal.
COM_RX	Input	Required	Serial receive signal. Data is sent from the BM to the micro-server module. 3.3 V-AUX signal.
UART0_TXD	Output	Required	Serial transmit signal. Data is sent from the micro-server module to the BMC. 3.3 V-AUX signal.
UART0_RXD	Input	Required	Serial receive signal. Data is sent from the BM to the micro-server module. 3.3 V-AUX signal.
GE0_TX_P/N	Output	Required	Primary Ethernet transmit signal. Data is sent from the micro-server module to the baseboard
GE0_RX_P/N	Input	Required	Primary Ethernet receive signal. Data is sent from the baseboard to the micro-server module
GE0_MDC	Output	Required	Primary Ethernet management interface clock signal.
GE0_MDIO	Input/Output	Required	Primary Ethernet management interface data signal.
PCIE0_RESET#	Output	Required	PCIe reset signal. If a PCIe bus is connected, this signal provides the reset signal indicating the card VRs and clocks are stable when drive high to 3.3V.



PCIE0_TX0/1/2/3_P/N	Output	Configurable	PCIe x4 bus-transmit signals. Data is sent from the micro-server module to the baseboard. These signals may or may not be connected on the baseboard.
PCIE0_RX0/1/2/3_P/N	Input	Configurable	PCIe x4 bus-receive signals. Data is sent from the baseboard to the micro-server module. These signals may or may not be connected on the baseboard.
PCIE0_REFCLK_P/_N	Output	Configurable	PCIe reference clock. This signal may or may not be connected on the baseboard.
PCIE1/2_RESET#	Output	Configurable	PCIe reset signals for to 2x additional PCIe buses. If a PCIe bus is connected, this signal provides the reset signal indicating the card VRs and clocks are stable when driven high to 3.3V.
PCIE1_TX0/1/2/3_P/N	Output	Configurable	Second set of PCIe x4 bus-transmit signals. Data is sent from the microserver module to the baseboard. These signals may or may not be connected on the baseboard.
PCIE1_RX0/1/2/3_P/N	Input	Configurable	Second set of PCIe x4 bus-receive signals. Data is sent from the baseboard to the micro-server module. These signals may or may not be connected on the baseboard.
PCIE1_REFCLK_P/_N	Output	Configurable	Two additional PCIe reference clocks. These signals may or may not be connected on the baseboard.
USB_P/N	Input/Output	Configurable	USB 2.0 differential pair.
RSVD	Input/Output	Configurable	Available differential pairs that could be configured as PCIe, SATA, SAS, Ethernet, or other high-speed interfaces.
RFU	Input/Output	Not connected	These pins are reserved for future use and are not used.

Table 14: Intel CPU module connector Pin Definitions



5.1.1.1 DDR3 SDRAM

The Rangeley Memory Controller supports up to 64 GB. The memory controller supports a 64-bit data bus with 8-bit ECC. When only one of the two memory channels is used in a platform board design, Channel 0 must be used. In all designs, Channel 0 must be populated by DRAM devices. Within each memory channel DIMMs are populated in slot order; slot 0 is populated first and slot 1 last. If a DIMM has two ranks, the ranks must be symmetrical (same chip width, same chip density, and same total memory size per rank). If both memory channels of the memory controller are used, then both channels must be populated identically. The CPU board is used a DDR3-1333 4GB SO-DIMM.

5.1.1.2 PCIe Interface

The Rangeley has up to 16 PCIe ports. Each port consists of a Transmitter differential pair and a Receiver differential pair which are in the 1.0-Volt Core power well of the SoC. The Rangeley supports devices with 5.0 GT/s and 2.5 GT/s capabilities.

6 IO and Connectors

6.1 RS232 Interface

- Baud Rate: s/w define
- Data bits: 8
- Stop Bit: 1
- Parity: None
- Flow control: None

6.2 Management Ethernet Interfaces

There are one single PHY on front panel PCBA, use SGMII interface from CPU module convert to 10/100/1000 RJ-45 GbE Management port. The PHY used is Marvell 88E1112.

6.3 USB Interface

The CPU contains one Enhanced Host Controller Interface (EHCI) and complies to the EHCI 1.0 Specification. The EHCI supports up to four USB 2.0 root ports. USB 2.0 allows data transfers up to 480 Mbps. The controller integrates a Rate-Matching Hub (RMH) to support USB 1.1 devices. The USB Port 1 interface is configured by the debug software to be a debug port.



7 Power/Environmental/Agency Certifications

Power		
Number of power supply	2	
Power supply types	AC (forward and reversed airflow) DC (forward and reversed airflow)	
Typical operating power	TBD	
Maximum power	511W	
AC PSUs • Input voltage • Frequency • Efficiency	770W • 100 to 240 VAC • 50 to 60 Hz	
DC PSUs Input voltage range Efficiency 	1100W • 40.5V/23.8A 48V/19.0A -60V/15.6	
Environment		
Operating temperature	$0 \sim 45^{\circ}$ C (at sea level with Fan Failure condition)	
Altitude	$0 \sim 10,000$ ft at 40° C [*]	
Storage temperature	-40~70°C	
Operating relative humidity	0%-95% RH (non-condensing)	
Storage relative humidity	0%~95% RH (non-condensing)	
Dimensions (height x width x depth)	44mmx440mmx487.4mm	
Weight	TBD	

Table 15: Power consumption and environment table

Regulatory Standards Compliance				
Regulatory compliance Safety	Comply with CE markings per directives 2004/108/EC and 2006/95/EC FCC/IC Report Class A BSMI UL/cUL Listed Mark CCC			
Safety	IEC60950-1 FCC/IC Report Class A EN 60950-1 FCC/IC Report Class A UL/CSA 60950-1 CNS 14336-1 GB4943.1			
EMC: Emissions	IEC60950-1 FCC/IC Report Class A EN 60950-1 FCC/IC Report Class A UL/CSA 60950-1 CNS 14336-1			



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Open Compute Project Alpha Networks SNX-60x0	-4861 Specification v0.6

GB4943.1				
RoHS Requirement				
Level	#	Description	Limitation/ ppm	
	A1	Cadmium/ Cadmium Compounds		80
	A2	Hexavalent Chromium/ Hexavalent Chromium Compounds		800
А	A3	Lead/ Lead Compounds	800	
	A4	Mercury/ Mercury Compounds	Mercury/ Mercury Compounds	
	A5	Polybrominated Biphenyls (PBBs)		800
	A6	Polybrominated Diphenylethers (PBDEs)		800
		Reliability Test Reports		
Test Items		Standards	Remarks	
MTBF Prec Report	diction	Telcordia SR-332, Issue 2		
Free Fall Test Report		IEC 60068-2-32: Basic Environmental Testing Procedures Part 2: Tests Test Ed: Free Fall-Second Edition; Incorporating Amendment 1; Amendment 2: 10-1990	 Drop Range: ≤ 20Kg,1000mm; ≤ 50kg, 500mm; Max. Load: 500 kg; FCS: 1 carton. 	
Vibration Test Report		IEC 60068-2-34:1973: Environmental testing Test Fd: Random vibration wide band-General requirements	 Frequency: 3 Method: Ra Test Time: 3 Axis; FCS: 1 carto 	0 min/Per
Storage Test Report		IEC 60068-2-48: Basic Environmental Testing Procedures Part 2: Tests Guidance on the Application of the Tests of IEC Publication 68 to Simulate the Effects of Storage-First Edition	 Low Temp.: -40℃,72Hours High Temp. /Low Humidity : 70 ℃,25%R.H.,72Hours High Temp. /High Humidity : 40 ℃,95%R.H.,96Hours FCS: 1 carton 	
Cold Test Report		IEC 60068-2-1: Environmental Testing Part 2: Tests - Tests A: Cold-Fifth Edition; Amendment 1-1993; Amendment 2-1994• Temperature: • Humidity: Unc • Test Time: 72 I • FCS: 2 sets		ncontrolled
Dry Heat Cyclic Test Report		EC 60068-2-2: Basic Environmental Testing Procedures Part 2: Tests - Tests 3: Dry Heat-Fourth Edition; Supplement A-1976; Amendment 1-1993; Amendment 2-1994Temperature Humidity: 5% Test Time: 72 FCS: 2 sets		%R.H.



Damp Heat Steady State Report	IEC 60068-2-78: Environmental Testing - Part 2-78: Tests - Test 2-78: Body Cab: Damp Heat, Steady State-First Edition; (Replaces IEC 60068-2-3 and 60068-2-56)	 Temperature: 40±2°C Humidity: 95+2-3%R.H. Test time: 96 Hours FCS: 2 sets 	
Damp Heat Cyclic Report	IEC 60068-2-30: Basic Environmental Testing Procedures Part 2: Tests - Test Db and Guidance: Damp Heat, Cyclic (12 + 12-Hour Cycle)-Second Edition; Amendment 1-08/1985	 Temperature: 40±2°C Humidity: 95+2-3%R.H. Cycle Time: 24 Hours Number of Cycle: 2 Cycles FCS: 2 sets 	
ESD Simulation Test Report	IEC 61000-4-2: Electromagnetic Compatibility (EMC) - Part 4-2: Testing and Measurement Techniques - Electrostatic Discharge Immunity Test-Edition 1.2; Edition 1:1995 Consolidated with Amendments 1:1998 and 2:2000	 Air Discharge: ±8KV; Contact Discharge: ±4KV; FCS: 1 set. 	
Electrical Isolation Test Report	For Class I equipment only.	 Primary (L-N) to Earth (Metal frame or Ground Pin): Minimum 1,5 kV ac, at least 60 seconds; Lan Port (RJ-45) to Ground (Metal frame) Minimum 1,5 kV ac at least 60 seconds. 	

Table 16: Regulatory Standards Compliance table