UfiSpace S9600-48X

Open Aggregation Router Specification

Revision 1.0

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2 Revision History

Date	Rev	Author	Summary of Change
Aug. 23, 2021	R1.0	Bruce Chang	First Draft Release

3 Overview

This document describes the technical specifications of the S9600-48X open aggregation router designed for telecom service applications.

The S9600-48X provides 100GE high speed Ethernet ports together with hardware support for Edge Grand Master with Primary Reference Time Clock (PRTC) and distributing phase and time accuracy via PTP (ITU-T G.8275.1) to meet 5G application scenarios. It enables service providers to deliver next-generation technologies such as a 5G Ethernet network, which requires high data bandwidth and very precise timing synchronization.

With redundant and hot-swappable power supplies and fans with a dense port design, the S9600-48X delivers high system reliability, Ethernet switching performance and intelligence to the network.

Front View

Rear View

4 High-Level Description

This section describes key features, system block diagram and system mechanical outline for S9600-48X.

4.1 Feature Summary

- Ethernet I/O ports :
  - 48 x 100GbE QSFP28 ports
- Timing I/O :
  - 1 x SMB for 1PPS
  - 1 x SMB for 10MHz
  - 1 x SMA for GNSS
- Front/Real panel LED indicators :
  - 2 x power status LED
  - 1 x FAN status LED
  - 1 x system status LED
  - Per QSFP port (Link/ACT)
  - Beaconing LED (2-digits 7 segment)
  - Per port FAN status LED (Rear panel on each FRU)
  - Per port PSU status LED (Rear panel on each FRU)
- Management interfaces :
  - 1 x GbE OOB management port (CPU)
  - 1 x USB2.0 Type-A general purpose port
  - 1 x RS232 console port in RJ45 form factor
  - 1 x USB console port in Micro USB form factor
  - 1 x tact switch for system reset/reload default configuration
  - 2 x 10G SFP+ management ports

4.2 Component Summary

- PCBA :
  - 1 x Switch board
  - 1 x CPU card
  - 1 x BMC card
  - 1 x FAN card
  - 1 x PSU card
  - 1 x OOB card
  - 1 x Timing card
  - 1 x Beacon LED card
- On board key components :
  - Switch Board
    - 1 x MAC Jericho2 Broadcom BCM88690
    - 1 x KBP Broadcom BCM16K
    - 12 x Gearbox Broadcom BCM81724
    - 1 x BMC AST2400
    - 1 x PCIe NIC controller I210-IT for CPU
  - CPU Card
    - 1 x CPU Broadwell-DE D-1548 with 8-core @ 2.0GHz
    - 4 x DDR4 RDIMM with ECC module support up to 4 x 32GB (Alpha : 2 x 32GB)
    - 2 x M.2 2280 SATA3 SSD module support up to 2 x 128GB (Alpha : 1 x 128GB)
- PSU & FAN :

- 2x 1600W slim PSUs with redundancy support
- 4x 8080 FAN tray modules with redundancy support

4.3 Switch Board Functional Block Diagram

S9600-48X system functional block diagram is shown as below:

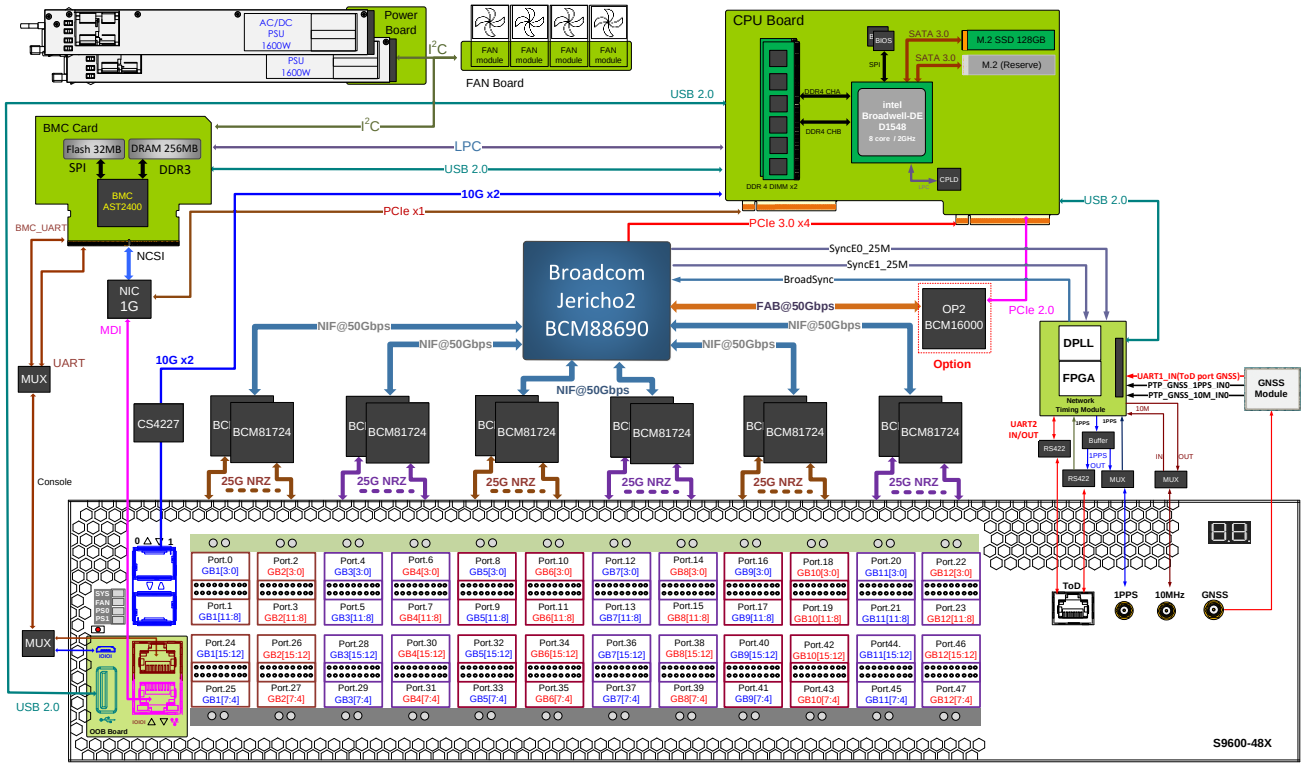


Figure 4-1 Switch Board Block Diagram

S9600-48X switch main board placement is shown as below, parts highlight in yellow are installed on PCB top side while components in blue are staffed on bottom side:

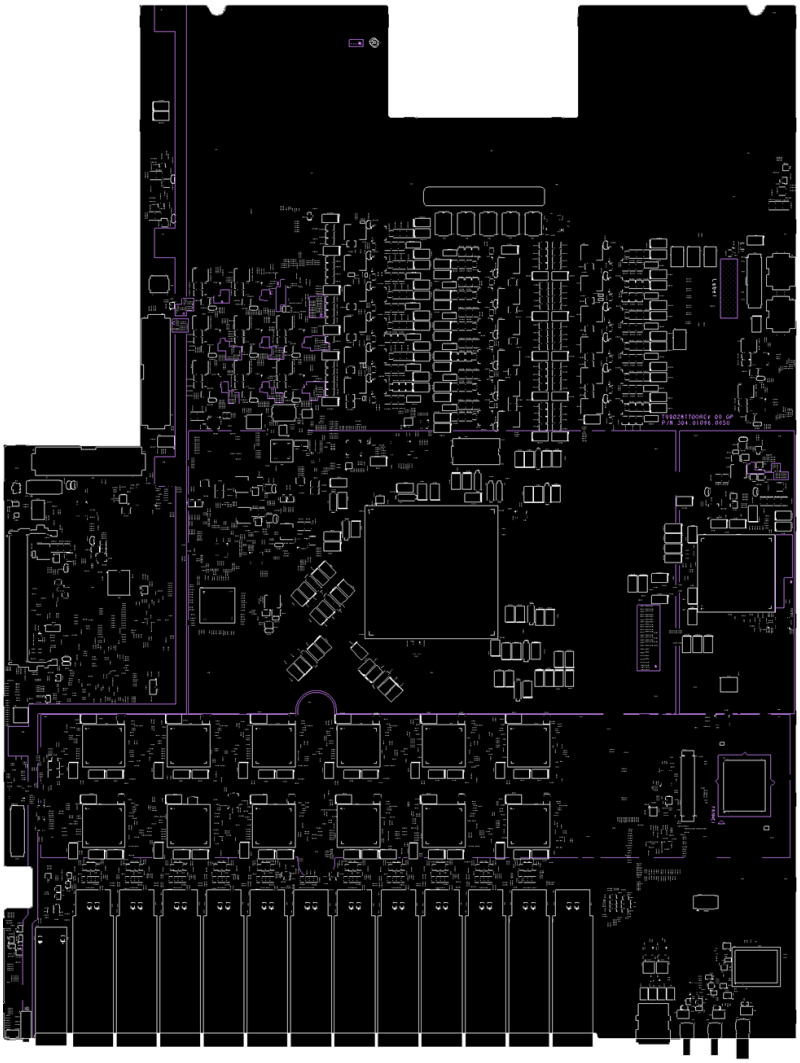


Figure 4-2 Switch Board PCB Layout

4.4 CPU Card Functional Block Diagram

S9600-48X CPU card block diagram is shown as below:

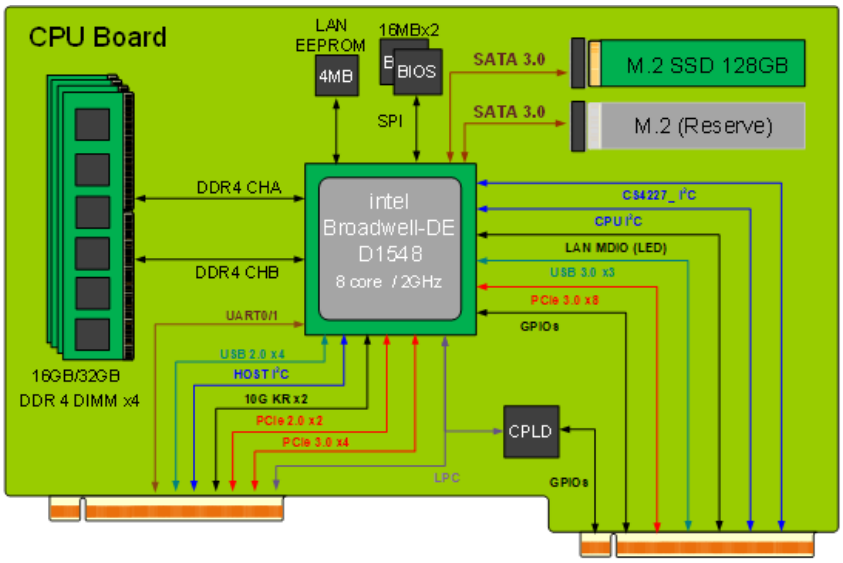


Figure 4-3 CPU Board Functional Block Diagram

S9600-48X CPU card placement is shown as below:

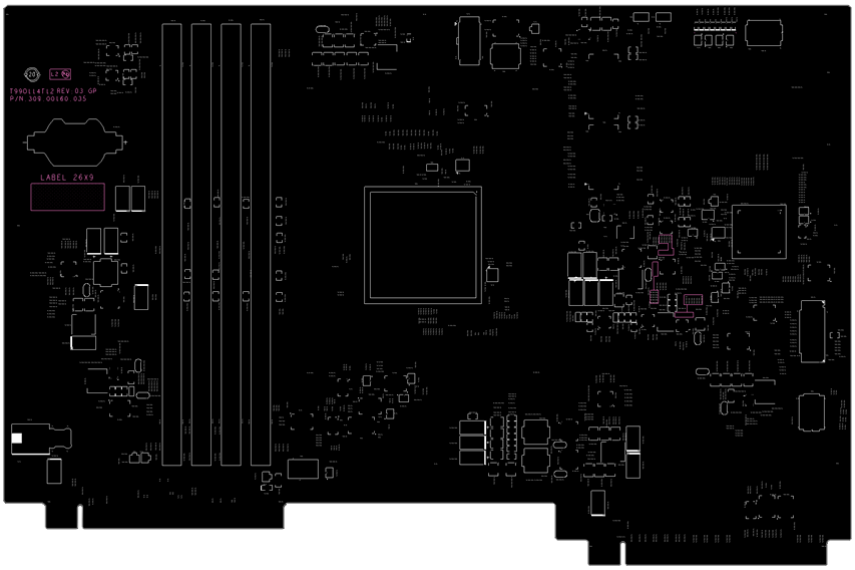


Figure 4-4 CPU Board PCB Layout

4.5 Mechanical Outline

The S9600-48X chassis is designed to meet cabinets with 19'' depth. This 2RU system mechanical dimension is: 436mm (W) x 790mm (D) x 87.7mm (H).

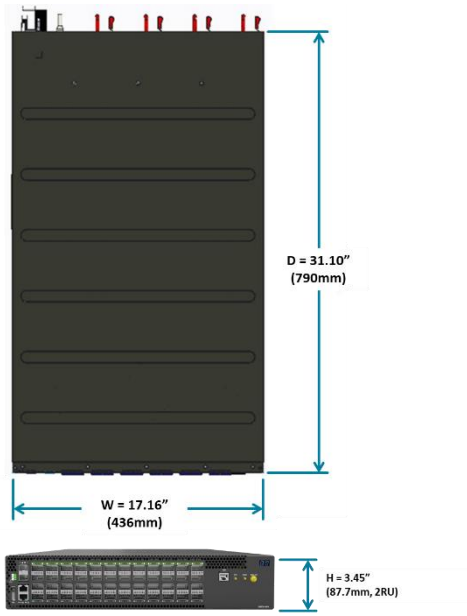


Figure 4-5 S9600-48X Mechanical Outline

4.6 System Explode Diagram

Below shows the S9600-48X system explode diagram. The mainboard will be populated inside the base chassis followed by the fan control board and air baffle together with MB and Fan card, which are fixed with screws. Next is the CPU card, which will be installed onto the right angle PCIe connector and fixed with standoffs/screws. The fan and PSU modules will be plugged into fan and PSU slots after chassis top cover is fixed.

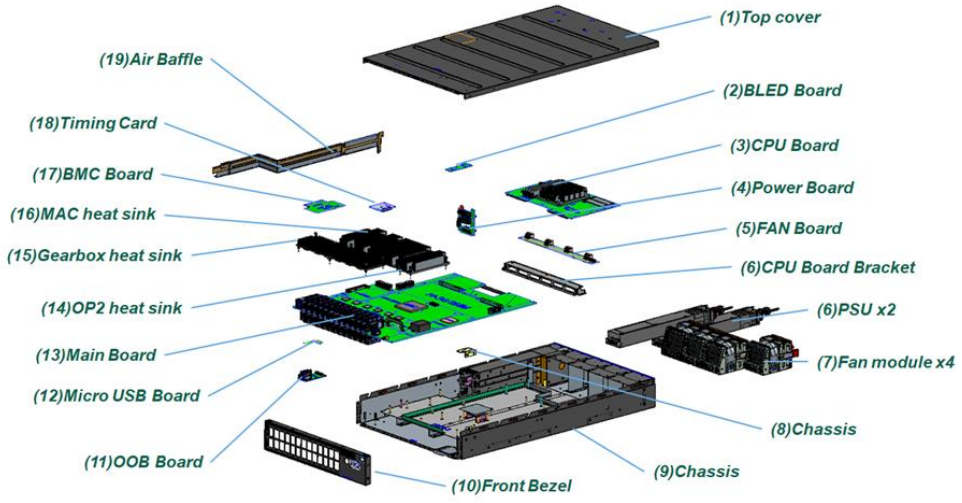


Figure 4-6 S9600-48X System Explode Diagram

The S9900-22XST system top view without top cover is shown as below :

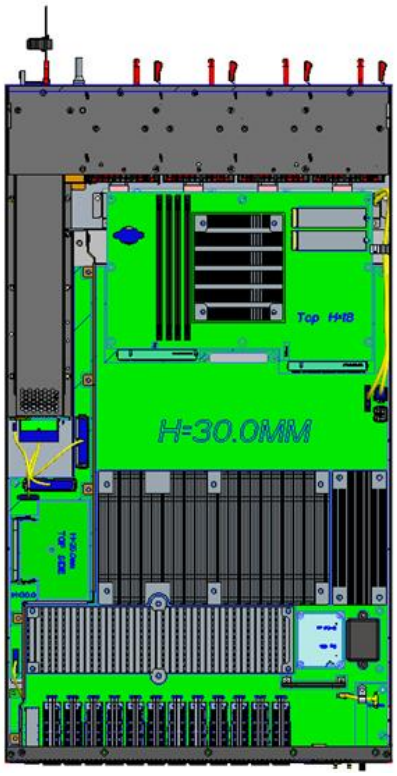


Figure 4-8 S9600-48X System Top View

5 Hardware Architecture

This section describes key features, system block diagrams and major components used on the S9600-48X.

5.1 CPU Subsystem

Intel's x86 embedded SoC processor Broadwell-DE D-1548 is equipped on the S9600-48X CPU board. The major onboard components and interfaces on the switch board are listed below:

- Intel's Broadwell-DE Processor
  - ✓ Capable of supporting up to 16-core processor
  - ✓ Four DDR4 ECC RDIMMs, up to 256GB
  - ✓ Two M.2 22*80mm SSD module, up to 512GB
  - ✓ Dual 16MB SPI boot/BIOS flash components
- Two PCIe gold fingers to switch board
  - ✓ Single x8 PCIe Gen3 interface
  - ✓ Single x4 PCIe Gen3 interface
  - ✓ Single x2 PCIe Gen2 interface
  - ✓ Two 10G-KR Ethernet interfaces
  - ✓ Two UART interfaces
  - ✓ Three USB3 interfaces
  - ✓ Three USB2 interfaces
  - ✓ Single LAN MDC/MDIO interface
  - ✓ Two SM Bus interfaces

5.2 BMC Subsystem

The S9600-48X base board management controller (BMC) autonomously monitors system's health including temperature, voltage, fan speed, etc. We use the DDR4 SO-DIMM connector as the BMC module connector. The BMC module connector is on the main board PCBA board.

5.2.1 BMC Subsystem Block Diagram

Below is the block diagram.

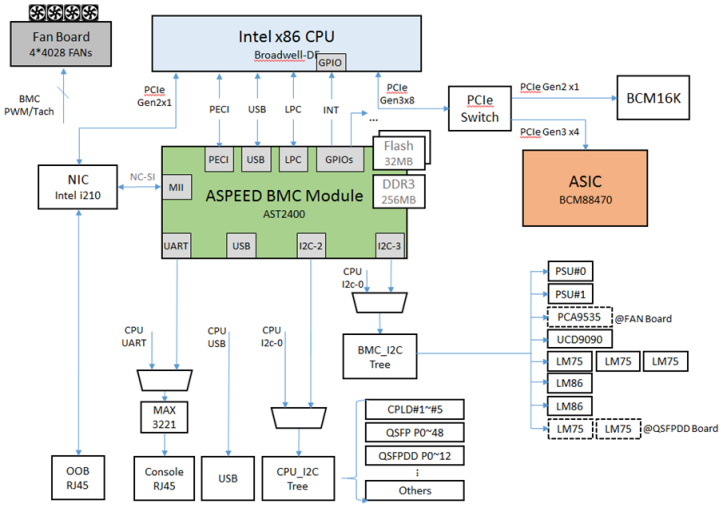


Figure 5-1 S9600-48X BMC Block Diagram

5.2.2 LPC

The Low-Pin-Count interface is an important interface for Broadwell-DE to communicate between the CPU board and the BMC. The OS running in x86 uses this interface to communicate with the BMC's IPMI message handler.

5.2.3 USB

The AST2400 provides three USB interfaces for different functional objectives. All USB controllers of AST2400 meet USB specification revision 2.0 and 1.1 and are also compliant with EHCI and UHCI specifications.

5.2.4 10/100/1000 Mbps Fast Ethernet MAC

The AST2400 integrates two MACs that are compliant with IEEE802.3 and IEEE802.3z specifications, which can support 10/100/1000M bps transfer rates. AST2400 also supports 2x RMII/NCSI or 2x RGMII interfaces. BMC shares the same management port in front-panel by connecting NC-SI interface to Intel I210 controller's NC-SI interface.

5.2.5 UART

The AST2400 supports up to 5 sets of UART IO interfaces with full flow control pins and 1 set with Tx/Rx only for BMC console. The administrator can switch between x86 and BMC consoles easily and choose between RJ45 or micro-USB connectors. Also, the BMC console could be disabled using commands. It also supports SOL, in which the host console is able to be decoded by the SuperI/O integrated in the AST2400 via the LPC interface. The UART MUX is controlled by the BMC and IO Expander on main board.

5.2.6 I2C

The AST2400 integrates up to 14 sets of multi-function I2C/SMBus bus controllers, which shall be SMBus compatible with 2-wire interfaces consisting of a serial data line (SDA) and a serial clock line (SCL). The I2C/SMBus bus controllers are used to collect voltage, temperature, FRU and EEPROM for storing manufacturing information.

S9600-48X implements two I2C trees for management: CPU_I2C tree and BMC_I2C tree. Both two I2C trees could be accessed by CPU or BMC, but the BMC only accesses the BMC_I2C tree in default configuration. The CPLD on Switch board will take the arbitration.

BMC can monitor the system's health continuously after boot up then record and handle the events when the values from sensors are out of reasonable range.

5.2.7 PWM/Tacho

The AST2400 integrates up to 8 sets of PWM outputs and 16 tachometer inputs. In S9600-48X switch, BMC Implements 4 Fans in 3+1 redundant.

5.2.8 GPIO

The AST2400 Integrates one set of parallel GPIO controllers with maximum 216 control pins, which are 28 sets, to provide general-purpose input/output functions.

5.2.9 Watchdog Timer/Keep Alive

The AST2400 supports two built-in 32-bit WDT modules. The S9600-48X uses WDT #1 to keep the x86 system alive. The OS running in x86 can enable watchdog timer, set timeout counter and timeout behavior by using IPMI command. If OS is halted, the BMC would reset the x86 system after watchdog timer is expired. The S9600-48X also implements WDT #2 internally to monitor the status itself. Once the BMC is halted, the BMC would reset itself without affecting the x86 system.

5.2.10 SPI Boot Flash

For reliability, there are two32MB SPI boot flashes, both of them include BMC firmware (U-boot, OS and application software storage). BMC will boot with flash#0 in default. Once BMC crash AST2400 will reboot after watchdog timeout with flash#1.

5.2.11 DDR3 SDRAM

The memory controller unit integrated in AST2400 supports x16 data bus width DDR3 SDRAM. One 128Mb x16 DDR3 SDRAM is installed for AST2400.

5.3 Switching Subsystem

This section details switch board component features/functionalities summary and hardware system design.

5.3.1 MAC Component

The BCM88690 is an integrated packet processor, traffic manager, and fabric interface single-chip switch. It processes 4.8Tb/s traffic at packet sizes above 284B. It also has integrated deep-buffer traffic management capabilities, a flexible and programmable packet processor, and a fabric interface. The network-facing interfaces of it can support various port rate combinations, including 10GbE, 25GbE, 40GbE, 50GbE, 100GbE, 200GbE, and 400GbE.

The BCM88690 integrates two 4-Hi HBM Gen2 for a total of 8GB deep buffering.

Applications:
- Data center TOR, leaf, spine, core and DCI
- Carrier Ethernet core/metro/edge switches and routers
- Carrier cloud
- Software Defined Networking (SDN)
- Carrier aggregation

5.3.1.1 Features Summary

- High performance
- 4.8Tb/s full-duplex packet processor
- 2000Mp/s processing rate
- StrataDNX fabric interface:
- 112 SerDes with rates up to 53.125 Gb/s
- Dynamically variable-sized cells for highly efficient segmentation
- Multiple line coding options with Reed-Solomon Forward Error Correction (RS-FEC)
- 1 + 1, N – x, and N + x redundancy schemes.
- Flexible network interface
- 96 SerDes with rates up to 53.125 Gb/s, supporting the following port configurations:
- 48 x 10GbE/25GbE/50GbE over one lane
- 24 x 40GbE/50GbE/100GbE over two lanes
- 12 x 40GbE/100GbE/200GbE over four lanes
- 6 x 400GbE over eight lanes
- Packet lengths supported in the range up to 10240B.
- Traffic Manager
- 64K programmable wire-rate queues
- Deep packet buffering
- Two integrated HBM Gen2 cubes
- Each cube is 4-Hi HBM for a total of 8 GB
- Congestion management:
- Hierarchical WRED and tail-drop policies.
- Congestion notification – CNM generation and CNM reception (proxy).
- Flow Control generation – Fully programmable in-band and out-band.
- Flow Control reception-any level – Interface, port, class, flow, traffic type-in-band out –of-band.
- Priority Flow Control (PFC), --Eight levels.

- Congestion tracking statistics.
- Up to 192K meters.
- Three ingress meter operations per packet.
- Two egress meter operations per packet.
- Hierarchical scheduling and shaping.
- Fully programmable and shaping.
- Support for priority propagation.
- MEF, DSL-FORUM TR-059-compliant scheduling and shaping.
- Packet processor
- Metro Ethernet, enterprise, and data center.
- Large, on-chip databases and optional off-chip database expansions.
- Full-featured – Bridging, routing, MPLS, VPLS L2VPNs, L3VPNs, OAM, and so on.
- Microcode controlled hardware – Flexible and future-proof.
- Increased LPM, up to 1M IPv4 prefixes.
- Ingress PMF – Cascade lookups.
- Native three-VLAN tag parsing.
- Counters and statistics.
- On-chip counter pool.
- Up to 384K counters (192K per core).
- External statistics interface..
- Statistics interface for expandable, off-chip statistics gathering:
- The SerDes used for the statistics interface is shared with NIF SerDes.
- Efficient packet-based protocol based on Ethernet simplifies connectivity to KBP BCM16K, TAP BCM5235, or FPGAs.
- Seamless connection to KBP BCM16K and TAP BCM5235 TAP devices.
- Multicast – Pointer-based ingress and/or egress multicast replication.
- In-band management.
- PCIe x four-lane Gen3 host interface with DMA.
- Hardware linkscan engine
- LED processor

5.3.1.2 KBP Component

The BCM16K Knowledge-Based Processor (KBP) performs high-speed operations on large-rule databased for a wide range of telecommunications applications.

The KBP addresses next-generation classification requirements through high-performance parallel decisions and improved entry storage capabilities. Parallel operations allow the device to reach decision speeds of multiple billion decisions per second (BDPS). Embedded error correction circuitry (ECC) improves system testability and operational reliability. The key processing unit (KPU) and the context buffer (CB) enable efficient interface transfers with flexible search key construction.

5.3.1.2.1 Features Summary

- Dual host enables two host devices to connect to one device.
- Database records 40b: 2048k/1024k.
- Table width configurable as 80/160/320/480/640 bits.

- User Data Array for associated data, width configurable as 32/64/128/256 bits.
- Context Buffer for storing master search keys.
- Up to sixteen parallel searches.
- Simultaneous Multithreading (SMT) operation up to four threads.
- NetRoute forwarding solution for Longest Prefix Match (LPM).
- NetACL solution for Access Control Lists (ACL).
- Logical Tables provide support for intelligent database management (LTR).
- Key Processing Unit (KPU) for flexible search key construction.
- Statistics and counters.
- Result Buffer provides programmability for flexible routing of search results.
- Range Matching for efficient storage utilization.
- ECC on User Data and Database Array. Parity protection on all embedded memories.
- Background ECC scan for database entries with provision for 2-bit anywhere and 4-bit continuous error detection.
- Forward Error Correction (FEC) when using PAM-4 signaling.
- PCI Express (PCIe) lane.

5.3.1.3 Reverse Gearbox

BCM81724 is a single-chip 8×56-Gb/s to 16×25-Gb/s NRZ reverse gearbox with 8×56-Gb/s PAM-4 Pass-Through mode PHY. It supports both the PAM-4 and NRZ data formats. It supports Retimer, Forward, and Reverse Gearbox modes.

5.3.1.3.1 Features Summary

- Host-side interface: 30 dB
- Line-side interface:
  - – 20 dB
  - – Chip-to-module (C2M) compliant
- Forward and Reverse Gearbox mode and Retimer mode
- Supports forward error correction (FEC)
- Supports 400G-CR8 mode
- Integrated AC-coupling capacitors at line-side receiver
- Multiple standard and line rate support for both PAM-4 and NRZ
- Continuous auto-adaptive equalizer
- Line- and system-side loopbacks
- PRBS generator/error checker
- Eye monitoring per lane on the line side, accessed through MDIO
- Single low-cost REFCLK input
- Recovered clock output
- Supports SGMII pass-through
- Interoperates with Broadcom ASIC and merchant switch silicon
- Low-power 16 nm CMOS design
- 19 mm × 19 mm BGA, 0.8 mm ball pitch package

5.3.1.4 Network Port Design

5.3.1.4.1 MIIM Interface Block Diagram

There is one OP2(option) and twelve reverse gearbox (BCM81724) for 100G ports, they are connected to dedicated MIIM interface and are directed managed by MAC, controlled by CPU.

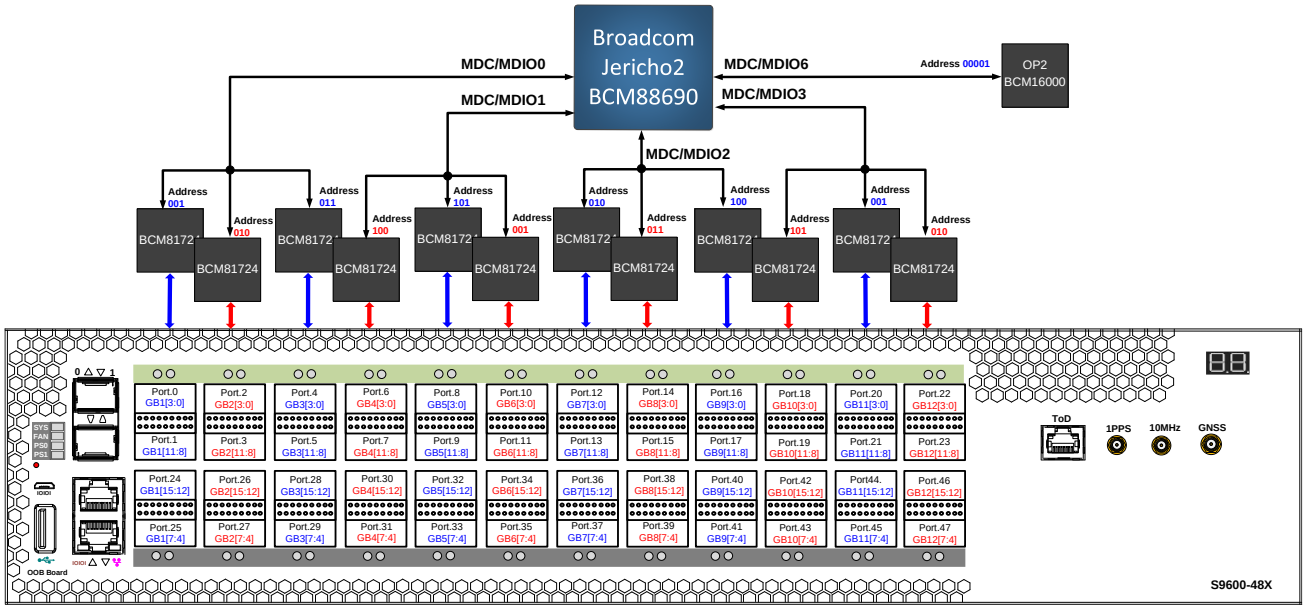


Figure 5-2 MIIM Block Diagram

5.3.1.4.2 Port Assignments

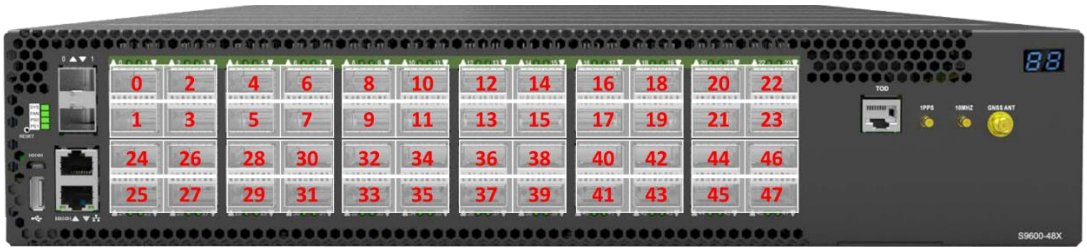


Figure 5-3 Physical Port Assignment

The table below shows the network ports numbering and speed.

Function	Port#	Speed	Notes
QSFP28 Ports	P0	40G/100G	100GBASE LR4 QSFP28
	P1	40G/100G	100GBASE LR4 QSFP28
	P2	40G/100G	100GBASE LR4 QSFP28
	P3	40G/100G	100GBASE LR4 QSFP28
	P4	40G/100G	100GBASE LR4 QSFP28
	P5	40G/100G	100GBASE LR4 QSFP28
	P6	40G/100G	100GBASE LR4 QSFP28
	P7	40G/100G	100GBASE LR4 QSFP28
	P8	40G/100G	100GBASE LR4 QSFP28
	P9	40G/100G	100GBASE LR4 QSFP28

	P10	40G/100G	100GBASE LR4 QSFP28
	P11	40G/100G	100GBASE LR4 QSFP28
	P12	40G/100G	100GBASE LR4 QSFP28
	P13	40G/100G	100GBASE LR4 QSFP28
	P14	40G/100G	100GBASE LR4 QSFP28
	P15	40G/100G	100GBASE LR4 QSFP28
	P16	40G/100G	100GBASE LR4 QSFP28
	P17	40G/100G	100GBASE LR4 QSFP28
	P18	40G/100G	100GBASE LR4 QSFP28
	P19	40G/100G	100GBASE LR4 QSFP28
	P20	40G/100G	100GBASE LR4 QSFP28
	P21	40G/100G	100GBASE LR4 QSFP28
	P22	40G/100G	100GBASE LR4 QSFP28
	P23	40G/100G	100GBASE LR4 QSFP28
	P24	40G/100G	100GBASE LR4 QSFP28
	P25	40G/100G	100GBASE LR4 QSFP28
	P26	40G/100G	100GBASE LR4 QSFP28
	P27	40G/100G	100GBASE LR4 QSFP28
	P28	40G/100G	100GBASE LR4 QSFP28
	P29	40G/100G	100GBASE LR4 QSFP28
	P30	40G/100G	100GBASE LR4 QSFP28
	P31	40G/100G	100GBASE LR4 QSFP28
	P32	40G/100G	100GBASE LR4 QSFP28
	P33	40G/100G	100GBASE LR4 QSFP28
	P34	40G/100G	100GBASE LR4 QSFP28
	P35	40G/100G	100GBASE LR4 QSFP28
	P36	40G/100G	100GBASE LR4 QSFP28
	P37	40G/100G	100GBASE LR4 QSFP28
	P38	40G/100G	100GBASE LR4 QSFP28
	P39	40G/100G	100GBASE LR4 QSFP28
	P40	40G/100G	100GBASE LR4 QSFP28
	P41	40G/100G	100GBASE LR4 QSFP28
	P42	40G/100G	100GBASE LR4 QSFP28
	P43	40G/100G	100GBASE LR4 QSFP28
	P44	40G/100G	100GBASE LR4 QSFP28
	P45	40G/100G	100GBASE LR4 QSFP28
	P46	40G/100G	100GBASE LR4 QSFP28
	P47	40G/100G	100GBASE LR4 QSFP28

Table 5-1 Network Port Connection

5.3.1.5 Port Mapping

Front Panel				Reverse Gearbox mode					
				PHY				MAC	
						Line side		Host side	
Connector		Physical port	Lane	MIIM Bus [7:0]	MIIM Address [4:2]	TX_Lane	RX_Lane	TX_Lane (NIF/FAB)	RX_Lane (NIF/FAB)
Top Side	2x1 QSFP28#0	0	0	0	001	0	0	NIF_02	NIF_02
			1			1	1		
			2			2	2	NIF_03	NIF_01
			3			3	3		
		1	0			8	8	NIF_04	NIF_04
			1			9	9		
			2			10	10	NIF_05	NIF_06
			3			11	11		
Bottom Side	2x1 QSFP28#1	24	0			12	12	NIF_06	NIF_07
			1			13	13		
			2			14	14	NIF_07	NIF_05
			3			15	15		
		25	0			4	4	NIF_01	NIF_00
			1			5	5		
			2			6	6	NIF_00	NIF_03
			3			7	7		
Top Side	2x1 QSFP28#2	2	0		010	0	0	NIF_08	NIF_09
			1			1	1		
			2			2	2	NIF_09	NIF_08
			3			3	3		
		3	0			8	8	NIF_12	NIF_14
			1			9	9		
			2			10	10	NIF_13	NIF_12
			3			11	11		
Bottom Side	2x1 QSFP28#3	26	0			12	12	NIF_14	NIF_13
			1			13	13		
			2			14	14	NIF_15	NIF_15
			3			15	15		
		27	0			4	4	NIF_10	NIF_10
			1			5	5		
			2			6	6	NIF_11	NIF_11
			3			7	7		
Top Side	2x1 QSFP28#4	4	0		011	0	0	NIF_16	NIF_19
			1			1	1		
			2			2	2	NIF_17	NIF_18
			3			3	3		
		5	0			8	8	NIF_20	NIF_20
			1			9	9		
			2			10	10	NIF_21	NIF_22
			3			11	11		
Bottom Side	2x1 QSFP28#5	28	0			12	12	NIF_22	NIF_21
			1			13	13		
			2			14	14	NIF_23	NIF_23
			3			15	15		
		29	0			4	4	NIF_18	NIF_17
			1			5	5		
			2			6	6	NIF_19	NIF_16
			3			7	7		

Top Side	2x1 QSFP28#6	6	0	1	100	0	0	NIF_24	NIF_27
			1			1	1		
			2			2	2	NIF_25	NIF_25
			3			3	3		
		7	0			8	8	NIF_28	NIF_28
			1			9	9		
			2			10	10	NIF_29	NIF_29
			3			11	11		
Bottom Side	2x1 QSFP28#7	30	0			12	12	NIF_30	NIF_30
			1			13	13		
			2			14	14	NIF_31	NIF_31
			3			15	15		
		31	0			4	4	NIF_26	NIF_26
			1			5	5		
			2			6	6	NIF_27	NIF_24
			3			7	7		
Top Side	2x1 QSFP28#8	8	0		101	0	0	NIF_32	NIF_35
			1			1	1		
			2			2	2	NIF_34	NIF_33
			3			3	3		
		9	0			8	8	NIF_36	NIF_36
			1			9	9		
			2			10	10	NIF_37	NIF_37
			3			11	11		
Bottom Side	2x1 QSFP28#9	32	0			12	12	NIF_38	NIF_38
			1			13	13		
			2			14	14	NIF_39	NIF_39
			3			15	15		
		33	0			4	4	NIF_33	NIF_32
			1			5	5		
			2			6	6	NIF_35	NIF_34
			3			7	7		
Top Side	2x1 QSFP28#10	10	0		001	0	0	NIF_89	NIF_88
			1			1	1		
			2			2	2	NIF_90	NIF_89
			3			3	3		
		11	0			8	8	NIF_95	NIF_92
			1			9	9		
			2			10	10	NIF_94	NIF_93
			3			11	11		
Bottom Side	2x1 QSFP28#11	34	0			12	12	NIF_93	NIF_95
			1			13	13		
			2			14	14	NIF_92	NIF_94
			3			15	15		
		35	0			4	4	NIF_88	NIF_90
			1			5	5		
			2			6	6	NIF_91	NIF_91
			3			7	7		

Top Side	2x1 QSFP28#12	12	0	2	010	0	0	NIF_81	NIF_81
			1			1	1		
			2			2	2	NIF_82	NIF_80
			3			3	3		
		13	0			8	8	NIF_87	NIF_85
			1			9	9		
			2			10	10	NIF_86	NIF_86
			3			11	11		
Bottom Side	2x1 QSFP28#13	36	0			12	12	NIF_85	NIF_87
			1			13	13		
			2			14	14	NIF_84	NIF_84
			3			15	15		
		37	0			4	4	NIF_80	NIF_82
			1			5	5		
			2			6	6	NIF_83	NIF_83
			3			7	7		
Top Side	2x1 QSFP28#14	14	0		011	0	0	NIF_74	NIF_72
			1			1	1		
			2			2	2	NIF_73	NIF_73
			3			3	3		
		15	0			8	8	NIF_79	NIF_79
			1			9	9		
			2			10	10	NIF_78	NIF_78
			3			11	11		
Bottom Side	2x1 QSFP28#15	38	0			12	12	NIF_77	NIF_77
			1			13	13		
			2			14	14	NIF_76	NIF_76
			3			15	15		
		39	0			4	4	NIF_75	NIF_74
			1			5	5		
			2			6	6	NIF_72	NIF_75
			3			7	7		
Top Side	2x1 QSFP28#16	16	0		100	0	0	NIF_66	NIF_64
			1			1	1		
			2			2	2	NIF_65	NIF_65
			3			3	3		
		17	0			8	8	NIF_70	NIF_71
			1			9	9		
			2			10	10	NIF_71	NIF_70
			3			11	11		
Bottom Side	2x1 QSFP28#17	40	0			12	12	NIF_68	NIF_69
			1			13	13		
			2			14	14	NIF_69	NIF_68
			3			15	15		
		41	0			4	4	NIF_67	NIF_66
			1			5	5		
			2			6	6	NIF_64	NIF_67
			3			7	7		

Top Side	2x1 QSFP28#18	18	0	3	101	0	0	NIF_57	NIF_56
			1			1	1		
			2			2	2	NIF_58	NIF_57
			3			3	3		
		19	0			8	8	NIF_62	NIF_63
			1			9	9		
			2			10	10	NIF_63	NIF_62
			3			11	11		
Bottom Side	2x1 QSFP28#19	42	0			12	12	NIF_61	NIF_61
			1			13	13		
			2			14	14	NIF_60	NIF_60
			3			15	15		
		43	0			4	4	NIF_56	NIF_58
			1			5	5		
			2			6	6	NIF_59	NIF_59
			3			7	7		
Top Side	2x1 QSFP28#16	20	0		001	0	0	NIF_43	NIF_43
			1			1	1		
			2			2	2	NIF_40	NIF_41
			3			3	3		
		21	0			8	8	NIF_44	NIF_44
			1			9	9		
			2			10	10	NIF_45	NIF_45
			3			11	11		
Bottom Side	2x1 QSFP28#17	44	0			12	12	NIF_46	NIF_46
			1			13	13		
			2			14	14	NIF_47	NIF_47
			3			15	15		
		45	0			4	4	NIF_42	NIF_42
			1			5	5		
			2			6	6	NIF_41	NIF_40
			3			7	7		
Top Side	2x1 QSFP28#18	22	0		010	0	0	NIF_51	NIF_51
			1			1	1		
			2			2	2	NIF_50	NIF_50
			3			3	3		
		23	0			8	8	NIF_52	NIF_52
			1			9	9		
			2			10	10	NIF_53	NIF_53
			3			11	11		
Bottom Side	2x1 QSFP28#19	46	0			12	12	NIF_54	NIF_54
			1			13	13		
			2			14	14	NIF_55	NIF_55
			3			15	15		
		47	0			4	4	NIF_49	NIF_48
			1			5	5		
			2			6	6	NIF_48	NIF_49
			3			7	7		

Table 5-2 Network Port Mapping

5.4 System Management

5.4.1 Local Clock Sources of System

There are two major I2C buses on the S9600-48X, one is CPU_I2C bus and another one is BMC_I2C. Both CPU and BMC can access the buses, but they need to negotiate with each other and only one host can access the buses at any time. The features of these two buses:

- CPU_I2C: Access to I2C devices including CPLDs, I/O Ports, peripherals.
- BMC_I2C: Access to I2C devices including PSU, FAN, thermal sensors.

The I2C block diagram is shown as below:

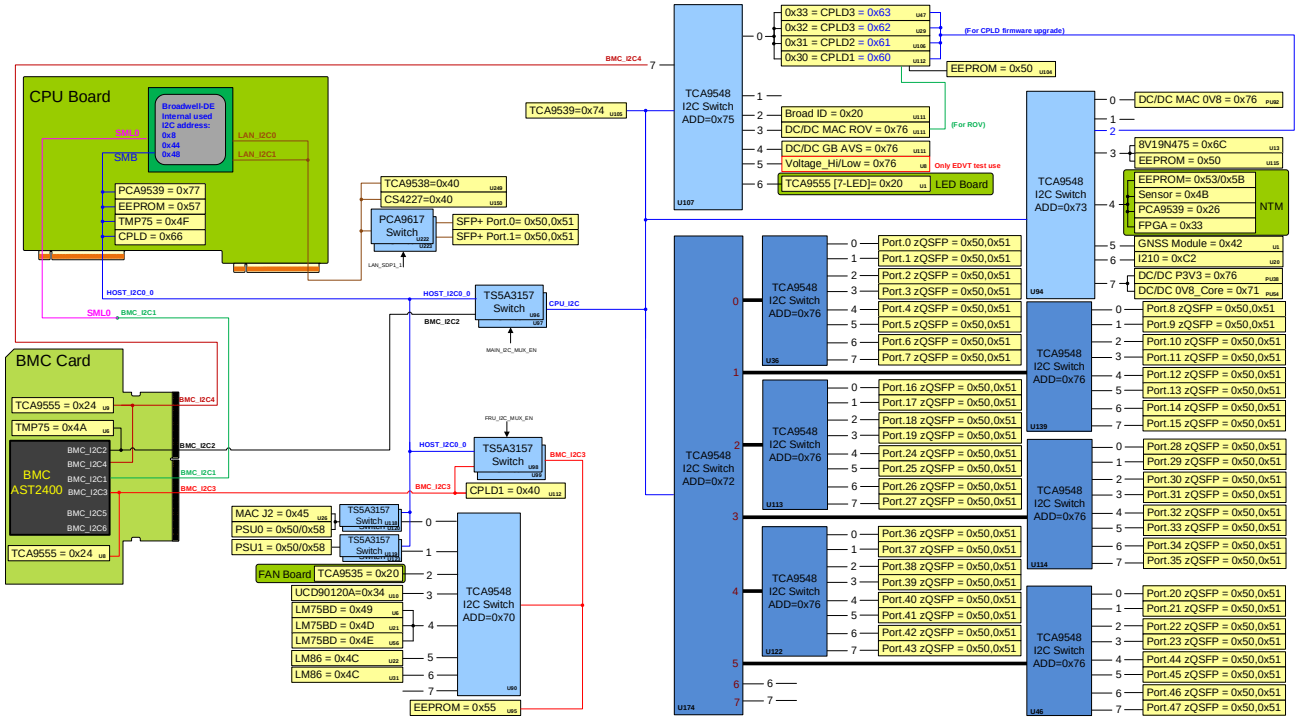


Figure 5-4 I2C Bus Connection Diagram

CPU_I2C Map:

I2C Bus	Name	Address		Device	Bit #	Function
LAN_I2C0	SFP+	101-0000/1 100-0000 101-1111	0x50/51 0x40 0x5F	SFP+ Port 0		I2C of SFP+ Port 0 TCA9538 CS4227
LAN_I2C1	SFP+	101-0000 101-0001	0x50 0x51	SFP+ Port 1		I2C of SFP+ Port 1
CPU_I2C	MAC J2 PSU0		0x45 0x50/58	BCM88690 PSU0		MAC J2 (Default disconnect) PSU0 EEPROM (Default disconnect)
	PSU1		0x50/58	PSU1		PSU1 EEPROM (Default disconnect)
	IOEXP	111-0000	0x74	TCA9539	0.7	Unused
					0.6	Unused
					0.5	Unused
					0.4	Unused
					0.3	Unused

I2C Bus	Name	Address		Device	Bit #	Function	
					0.2	Unused	
					0.1	Unused	
					0.0	Unused	
					1.7	CPLD1_TO_CPU_INT_L	
					1.6	CPLD2_TO_CPU_INT_L	
					1.5	CPLD3_TO_CPU_INT_L	
					1.4	CPLD4_TO_CPU_INT_L	
					1.3	Unused	
					1.2	Unused	
					1.1	Unused	
					1.0	Unused	
	I2C MUX	111-0101	0x75	TCA9548	CH0	CPLD4 control CPLD3 control CPLD2 control CPLD1 control	0x63 0x62 0x61 0x60
					CH1	Unused	
					CH2	Board ID	0x20
					CH3	DC/DC MAC ROV	0x76
					CH4	DC/DC Gearbox AVS	0x76
					CH5	Voltage Margin,	0x76
					CH6	TCA9555 7-SEG LED	0x20
					CH7	BMC_I2C4	
	I2C MUX	111-0011	0x73	TCA9548	CH0	DC/DC MAC 0V8	0x76
					CH1	Unused	
					CH2	CPLD4 upgrade CPLD3 upgrade CPLD2 upgrade CPLD1 upgrade	0x63 0x62 0x61 0x60
					CH3	Clock Gens 8V19N475 EEPROM	0x6C 0x50
					CH4	NTM-EEPROM NTM-Sensor NTM-PCA9539 NTM-FPGA	0x53,0x5B 0x4B 0x26 0x33
					CH5	GNSS module	0x42
					CH6	Ethernet controller, I210	0xC2
					CH7	DC/DC P3V3 DC/DC 0V8_Core	0x76 071
	I2C MUX	111-0010	0x72	TCA9548	CH0	I2C of QSFP Port 0~7 MUX	0x76
					CH1	I2C of QSFP Port 8~15MUX	0x76
					CH2	I2C of QSFP Port 16~19,24~27 MUX	0x76
					CH3	I2C of QSFP Port 28~35 MUX	0x76
					CH4	I2C of QSFP Port 36~43MUX	0x76
					CH5	I2C of QSFP Port 20~23,44~47 MUX	0x76

I2C Bus	Name	Address		Device	Bit #	Function	
					CH6	Unused	
					CH7	Unused	
	I2C of zQSFP Port 0~7 MUX	111-0110	0x76	TCA9548	CH0	I2C of QSFP Port 0 MUX	0x50,0x51
					CH1	I2C of QSFP Port 1 MUX	0x50,0x51
					CH2	I2C of QSFP Port 2 MUX	0x50,0x51
					CH3	I2C of QSFP Port 3 MUX	0x50,0x51
					CH4	I2C of QSFP Port 4 MUX	0x50,0x51
					CH5	I2C of QSFP Port 5 MUX	0x50,0x51
					CH6	I2C of QSFP Port 6 MUX	0x50,0x51
					CH7	I2C of QSFP Port 7 MUX	0x50,0x51
	I2C of zQSFP Port 8~15 MUX	111-0110	0x76	TCA9548	CH0	I2C of QSFP Port 8 MUX	0x50,0x51
					CH1	I2C of QSFP Port 9 MUX	0x50,0x51
					CH2	I2C of QSFP Port 10 MUX	0x50,0x51
					CH3	I2C of QSFP Port 11 MUX	0x50,0x51
					CH4	I2C of QSFP Port 12 MUX	0x50,0x51
					CH5	I2C of QSFP Port 13 MUX	0x50,0x51
					CH6	I2C of QSFP Port 14 MUX	0x50,0x51
					CH7	I2C of QSFP Port 15 MUX	0x50,0x51
	I2C of zQSFP Port 16~19, 24~27 MUX	111-0110	0x76	TCA9548	CH0	I2C of QSFP Port 16 MUX	0x50,0x51
					CH1	I2C of QSFP Port 17 MUX	0x50,0x51
					CH2	I2C of QSFP Port 18 MUX	0x50,0x51
					CH3	I2C of QSFP Port 19 MUX	0x50,0x51
					CH4	I2C of QSFP Port 24 MUX	0x50,0x51
					CH5	I2C of QSFP Port 25 MUX	0x50,0x51
					CH6	I2C of QSFP Port 26 MUX	0x50,0x51
					CH7	I2C of QSFP Port 27 MUX	0x50,0x51
	I2C of zQSFP Port 28~35 MUX	111-0110	0x76	TCA9548	CH0	I2C of QSFP Port 28 MUX	0x50,0x51
					CH1	I2C of QSFP Port 29 MUX	0x50,0x51
					CH2	I2C of QSFP Port 30 MUX	0x50,0x51
					CH3	I2C of QSFP Port 31 MUX	0x50,0x51
					CH4	I2C of QSFP Port 32 MUX	0x50,0x51
					CH5	I2C of QSFP Port 33 MUX	0x50,0x51
					CH6	I2C of QSFP Port 34 MUX	0x50,0x51
					CH7	I2C of QSFP Port 35 MUX	0x50,0x51
	I2C of zQSFP Port 36~43 MUX	111-0110	0x76	TCA9548	CH0	I2C of QSFP Port 36 MUX	0x50,0x51
					CH1	I2C of QSFP Port 37 MUX	0x50,0x51
					CH2	I2C of QSFP Port 38 MUX	0x50,0x51
					CH3	I2C of QSFP Port 39 MUX	0x50,0x51
					CH4	I2C of QSFP Port 40 MUX	0x50,0x51
					CH5	I2C of QSFP Port 41 MUX	0x50,0x51

I2C Bus	Name	Address		Device	Bit #	Function	
					CH6	I2C of QSFP Port 42 MUX	0x50,0x51
					CH7	I2C of QSFP Port 43 MUX	0x50,0x51
	I2C of zQSFP Port 20~23, 44~47 MUX	111-0110	0x76	TCA9548	CH0	I2C of QSFP Port 20 MUX	0x50,0x51
					CH1	I2C of QSFP Port 21 MUX	0x50,0x51
					CH2	I2C of QSFP Port 22 MUX	0x50,0x51
					CH3	I2C of QSFP Port 23 MUX	0x50,0x51
					CH4	I2C of QSFP Port 44 MUX	0x50,0x51
					CH5	I2C of QSFP Port 45 MUX	0x50,0x51
					CH6	I2C of QSFP Port 46 MUX	0x50,0x51
					CH7	I2C of QSFP Port 47 MUX	0x50,0x51

Table 5-3 CPU I2C Device List

BMC_I2C Map:

I2C Bus	Name	Address		Device	Bit #	Function	
BMC_I2C1	CPU SML0						
BMC_I2C2	Thermal sensor	100-1010	0x4A	TMP75		Thermal sensor	
BMC_I2C3	IOEXP	010-0000	0x20	PCA9539	0.7	Thermal sensor interrupt	
					0.6	Unused	
					0.5	Unused	
					0.4	Unused	
					0.3	Unused	
					0.2	Unused	
					0.1	Unused	
					0.0	Unused	
					1.7	Board ID_3	
					1.6	Board ID_2	
					1.5	Board ID_1	
					1.4	Board ID_0	
					1.3	HW_REV_1	
					1.2	HW_REV_0	
					1.1	Build_REV_1	
					1.0	Build_REV_0	
	EEPROM	101-0101	0x55	M24128	--	Main Board EEPROM	
	CPLD1	000-0100	0x40	CPLD	--	CPLD1	
	I2C MUX	111-0001	0x70	TCA9548	CH0	MAC J2 PSU0 EEPROM	0x45 0x50/0x58
					CH1	PSU1 EEPROM	0x50/0x58
					CH2	PCA9535(at Fan board) Ch1.7: FAN4_DIR Ch1.6: FAN4_ABS Ch1.5: FAN4_LED_Y Ch1.4: FAN4_LED_G Ch1.3: FAN3_DIR Ch1.2: FAN3_ABS Ch1.1: FAN3_LED_Y Ch1.0: FAN3_LED_G	0x20

I2C Bus	Name	Address		Device	Bit #	Function	
						Ch0.7: FAN2_DIR Ch0.6: FAN2_ABS Ch0.5: FAN2_LED_Y Ch0.4: FAN2_LED_G Ch0.3: FAN1_ABS Ch0.2: FAN1_ABS Ch0.1: FAN1_LED_Y Ch0.0: FAN1_LED_G	
					CH3	UCD90120A	0x34
					CH4	LM75BD 1 LM75BD 2 LM75BD 3	0x49 0x4D 0x4E
					CH5	LM86	0x4C
					CH6	LM86	0x4C
					CH7	Unused	
BMC_I2C4	IOEXP	010-0000	0x20	PCA9539	0.7	Unused	
					0.6	Unused	
					0.5	Unused	
					0.4	Unused	
					0.3	Unused	
					0.2	Unused	
					0.1	Unused	
					0.0	Unused	
					1.7	Board ID_3	
					1.6	Board ID_2	
					1.5	Board ID_1	
					1.4	Board ID_0	
					1.3	HW_REV_1	
					1.2	HW_REV_0	
					1.1	Build_REV_1	
					1.0	Build_REV_0	
BMC_I2C5						Unused	
BMC_I2C6						Unused	

Table 5-4 BMC I2C Device List

5.4.2 System PCIe Interface

PCIe Gen 2, 3 interfaces are used to manage the slave devices by host CPU. PCIe slave component includes MAC BCM88690, BCM16K, and I210.

PCIe interrupt from these components are wired together and connected to CPU card. CPU should scan PCIe devices one by one to check where the interrupt event comes from.

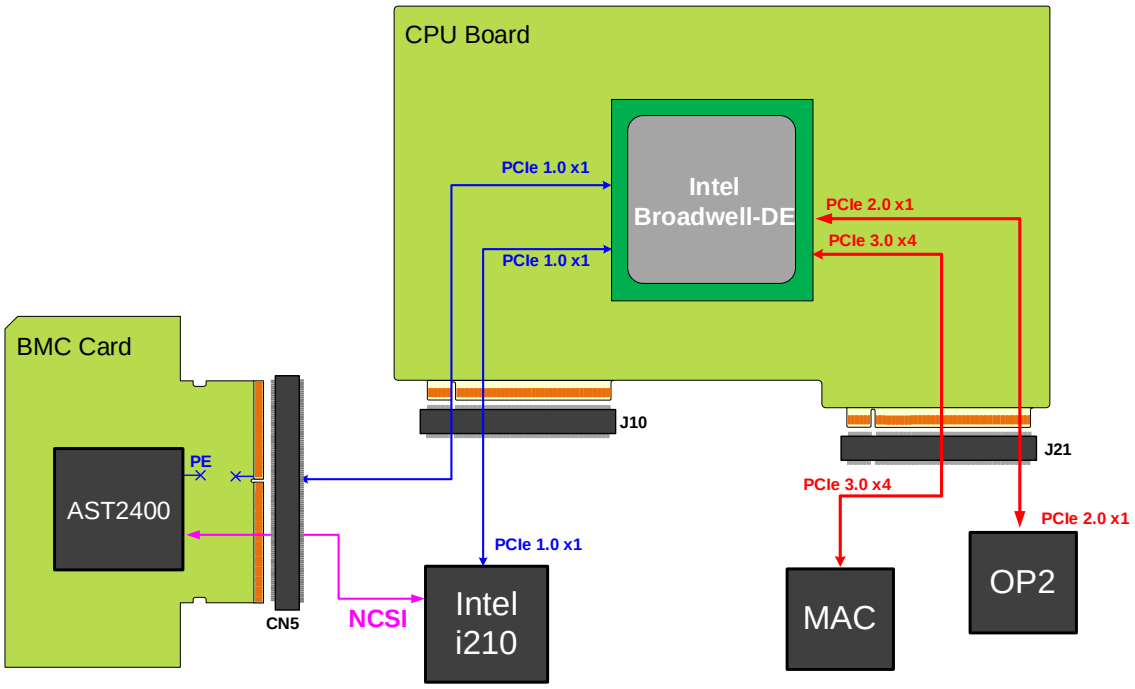


Figure 5-5 PCIe Connection Diagram

5.5 Timing Subsystem

This chapter describes timing subsystem of S9600-48X. There are two clock domains:

Local clocks for non-synchronized components (BMC, I210, DDR4, etc.)

Network timing clocks for synchronized Ethernet components: MAC and PHY

Local clock sources are generated by the motherboard clock generator 8T39S08A, while the synchronized clocks are generated by the NTM (Network Timing Module).

5.5.1 Local Clock Sources of System

Components, such as BMC, NIC i210, DDR4, PCIe Bus and core/DDR clocks of MAC, have separate clock domains and don't synchronize timing from PTP or SyncE recovered clock. These clocks will be generated by 8T39S08A right after the system powers on and doesn't need to have further software configurations.

When the NTM is not present or initialized, the MAC & PHY reference clocks will be sourced by the Jitter attenuator 8V19N475, which generates 156.25MHz for 10G PHY and MAC.

Once the NTM is initialized, the 8V19N475 will refer to the NTM's clock, which is driven by a Stratum 3E OCXO. The frequency accuracy is 4.6PPM for over 20 years.

5.5.2 Network Timing Synchronization Subsystem

The other subsystem is for network timing synchronization. It is a key subsystem that enables S9600-48X to synchronize with the external reference clocks or timing sources including 1588 packet, SyncE recovered clock, 1PPS, and 10MHz.

5.6 Daughter Boards

There are five daughter boards on the S9600-48X system. It includes FAN board, PSU Board, OOB, Micro-USB, and Beacon LED board. The details of these boards are shown in the following sections.

5.6.1 Fan Board

The Fan expander board is a passive board that bridges 12V power and control I/O to the Fan modules. The fan's I/O is controlled by BMC. The figure below shows the Fan board dimensions, layout and pin definitions.

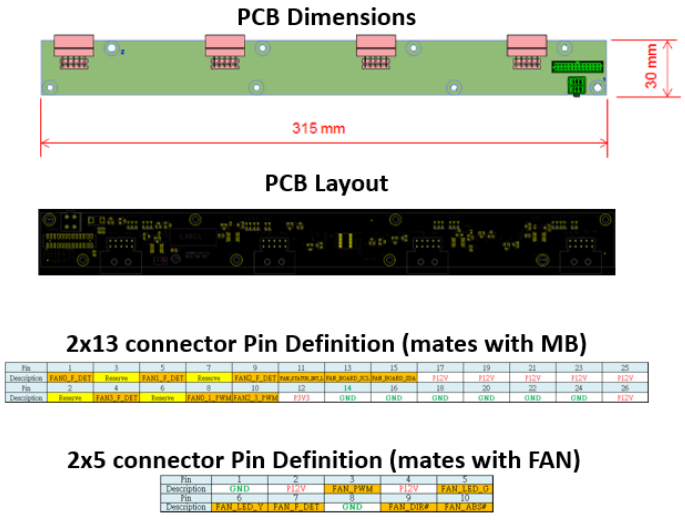
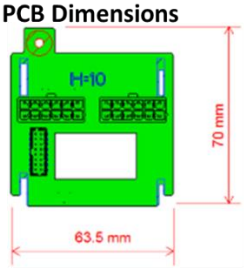


Figure 5-6 Fan Board Dimensions, Layout, Pin Definition

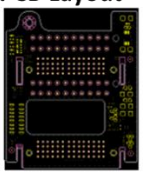
5.6.2 PSU Board

The PSU board is a passive board that bridges 12V power and control signals to the PSU. The figure below shows the PSU board dimensions, layout and pin definitions.

PCB Dimensions



PCB Layout



Power Edge Connector Pin Definition (mates with PSU)

Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description
A1	PSU_PRESENT	B1	PSU_FOB_FAULT	C1	GND	D1	P12V	P1_1	GND	P2_1	GND	P3_1	P12V	P4_1	P12V
A2	PSU_FOB_ALERT	B2	PSU_A0	C2	PSU_INT	D2	PSU_SHARE_PIN	P1_2	GND	P2_2	GND	P3_2	P12V	P4_2	P12V
A3	RESERVED	B3	AC_OK	C3	PSU_STATUS_SCL	D3	PSU_STATUS_SDA	P1_3	GND	P2_3	GND	P3_3	P12V	P4_3	P12V
A4	RESERVED	B4	RESERVED	C4	PSU_PWRON#	D4	GND	P1_4	GND	P2_4	GND	P3_4	P12V	P4_4	P12V
A5	RESERVED	B5	RESERVED	C5	PSU_A1	D5	PSU_PWROK								
A6	+5VSB	B6	+5VSB	C6	+5VSB	D6	+5VSB								

2x8 signal connector Pin Definition (mates with MB)

Pin	1	3	5	7	9	11	13	15
Description	PSU0_STATUS_SDA	PSU1_INT	PSU1_STATUS_SDA	PSU1_PRSNT	PSU1_PWROK	PSU1_PWRON	+5VSB	+5VSB
Pin	2	4	6	8	10	12	14	16
Description	PSU0_STATUS_SCL	PSU0_INT	PSU1_STATUS_SCL	PSU0_PRSNT	PSU0_PWROK	PSU0_PWRON	P3V3	GND

Power connector Pin Definition (mates with MB)

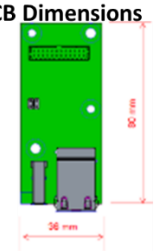
Pin	1	3	5	7	9	11	13	15	17	19
Description	GND	GND	GND	GND	GND	P12V	P12V	P12V	P12V	P12V
Pin	2	4	6	8	10	12	14	16	18	20
Description	GND	GND	GND	GND	GND	P12V	P12V	P12V	P12V	P12V

Figure 5-7 PSU Board Dimensions, Layout, Pin Definition

5.6.3 OOB Board

The management board has a console port and a management port. It also connects power outputs to the main board and fan expander board. The figure below shows the OOB board dimensions, layout and pin definitions.

PCB Dimensions



PCB Layout

2x2 Connector Pin Definition (mates with Micro-USB Board)

Pin Name	PIN NO.		Pin Name
P5V	1	2	GND
USB_UART_PN	3	4	USB_UART_DN

2x12 signal connector Pin Definition (mates with MB)

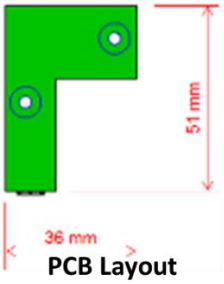
Pin Name	PIN	PIN	Pin Name
P5V_SB	1	2	P3V3
GND	3	4	OOB_SPD_1G
OOB_MDI_N0	5	6	OOB_LINK_ACT
OOB_MDI_P0	7	8	GND
OOB_MDI_N1	9	10	UART_TX
OOB_MDI_P1	11	12	UART_RX
OOB_MDI_N2	13	14	GND
OOB_MDI_P2	15	16	USB_N
OOB_MDI_N3	17	18	USB_P
OOB_MDI_P3	19	20	GND
NVCC_3V1	21	22	P5V
NC	23	24	NC

Figure 5-8 OOB Board Dimensions, Layout, Pin Definition

5.6.4 Micro USB Board

The USB board is a board that bridges 5V power and signals to the USB connector, it also provides the UART signals to USB console port for configuration. The figure below shows the Micro USB board dimensions, layout and pin definitions.

PCB Dimensions



PCB Layout

Micro-USB Pin Definition

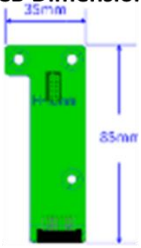
Pin	Signal
1	5V_USB
2	UART_M_RXD
3	UART_M_TXD
4	Reserve
5	GND

Figure 5-9 Micro USB Board Dimension, Layout, Pin Definition

5.6.5 Beacon LED Board

The figure below shows the Beacon LED board dimensions, layout and pin definitions.

PCB Dimensions



PCB Layout

Beacon LED Pin Definition

Pin Name	PIN	PIN	Pin Name
P3V3	1	2	P3V3
P3V3	3	4	Beacon_LED_SCL
NC	5	6	Beacon_LED_SDA
NC	7	8	GND
GND	9	10	GND

Figure 5-10 Beacon LED Board Dimension, Layout, Pin Definition

5.7 Front Panel Design

The S9600-48X front panel IO ports and LED include the functionalities below:

- System status LED
  - ✓ SYS status LED
  - ✓ FAN status LED
  - ✓ PSU0 status LED
  - ✓ PSU1 status LED
- Ethernet ports LED
  - ✓ OOB copper ports LED
  - ✓ Data traffic fiber ports LED
- Management ports (Share between CPU and BMC)
  - ✓ 1x OOB port
  - ✓ 1x Type A USB2.0 port
  - ✓ 1x console port in RJ45
  - ✓ 1x console port in Micro-USB
- Timing Portsorts
  - ✓ 1x SMB in/out port for 1PPS
  - ✓ 1x SMB in/out port for 10MHz
  - ✓ 1x SMA for GNSS
  - ✓ 1x ToD port in RJ45
- Ethernet data ports
  - ✓ 48x 100G QSFP28 ports
  - ✓ 2x 10G SFP+ ports

The S9600-48X rear panel design:

- Fan module
- Fan status LED

Detailed IO arrangement is shown as below:

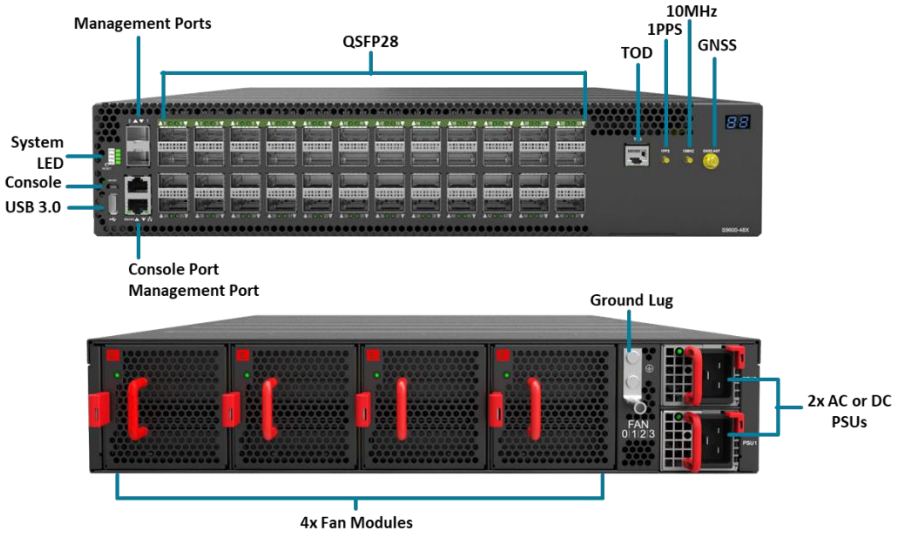


Figure 5-11 Front Panel IO Arrangement

5.7.1 System LED Indicators

The system status and LEDs are placed on the main board and controlled by CPLD1 address 0x30. The BMC monitors the system status (SYS, FAN and PS0, PS1) and controls the system LED behavior via CPLD registers.

LED Function/State	Meaning
OFF	No power
Solid Green	Host CPU/BMC boot complete
Solid Amber	Power is up but Host CPU/BMC boot failed
OFF	Fans are not initialized
Solid Green	All Fans are work normal
Blinking Amber	Fan fail : one or more Fans need service
OFF	No power
Solid Green	PSU1 is work normal
Blinking Amber	PSU1 fail (PSU1 need service)
OFF	No power
Solid Green	PSU2 is work normal
Blinking Amber	PSU2 fail (PSU2 need service)

The platform will have 2 green LEDs integrated in the front panel management RJ45 port.

OOB LED Function/State	Meaning
OFF	No power
Left LED Solid Green	1G link-up
Left LED Blinking Green	1G TX/RX activity
Right LED Solid Amber	10M/100M link-up
Right LED Blinking Amber	10M/100M TX/RX activity

The S9600-48X Support 2 x 10G SFP+ management ports

Fan LED Function/State	Meaning
OFF	Main board 3.3V power fail or Fan is not present.
Solid Green	Fan is present and interrupt de-assert
Blinking Green	N/A
Solid Yellow	N/A
Blinking Yellow	Fan is present but interrupt assert.

Table 5-5 System LED Description

For RJ45, SFP+, SFP28 and QSFP28 ports controlled by serial LED interface of MAC.

LED Function/State	Meaning	Comment
SFP+ (port 0 & 1) (Green/Yellow):		
Off	No link or port disable	

Solid Green	SFP+ port link at 10G mode	
Blinking Green	SFP+ port is transmitting at 10G mode	
Solid Yellow	SFP+ port link at 1G mode	
Blinking Yellow	SFP+ port is transmitting at 1G mode	
QSFP28 (all) (Green/Yellow):		
OFF	No link or port disable	
Solid Green	QSFP28 port link at 400G mode	
Blinking Green	QSFP28 port is transmitting at 400G mode	
Solid Yellow	QSFP28 port link at 100G mode	
Blinking Yellow	QSFP28 port is transmitting at 100G mode	
OOB port (Green/Yellow):		
OFF	No power	
Left LED Solid Green	1G link-up	
Left LED Blinking Green	1G TX/RX activity	
Right LED Solid Amber	10M/100M link-up	
Right LED Blinking Amber	10M/100M TX/RX activity	

Table 5-6 Ethernet Ports LED Description

5.7.2 OOB Ports

The S9600-48X includes 1standard GE RJ45 port for out of band (OOB) management, shared between CPU and BMC. It supports the IEEE 802.3 specification for 10/100/1000Mbps operation.

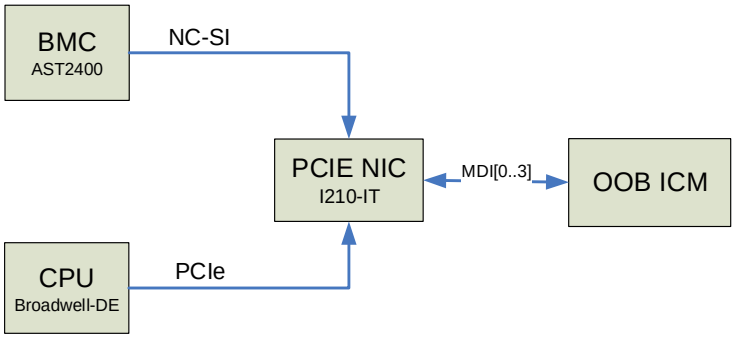


Figure 5-12 CPU OOB Interface Diagram

5.7.3 Console Port

Two console ports are available for the S9600-48X's systems access and both of them can be used for CPU or BMC access. The pin definition of the RS232 console port is shown below. Pin3 is the TX signal from internal processor to external RS232 interface, and Pin6 is the RX signal from external RS232 interface to internal processor. The bound rate is 115200 by default.

PIN #	Definition	Direction	Note
1	NC		
2	NC		
3	UART_TXD	Out	Console TX
4	GND		
5	GND		
6	UART_RXD	In	Console RX
7	GND		
8	GND		

Table 5-7 Pin Definition of RJ45 Console Connector

5.7.4 USB 2.0 Port

The S9600-48X integrates a USB 2.0 host controller that supports a single port operating at high speed (HS) at 480 Mbps (USB 2.0).

USB 5V power will be enabled during system initialization, software should de-assert 'PWR_EN' by pulling this pin low once over current event (USB device consumes >0.5A current more than 20mS) is received. 'PWR_EN' need set as 'HIGH' to re-enable USB port.

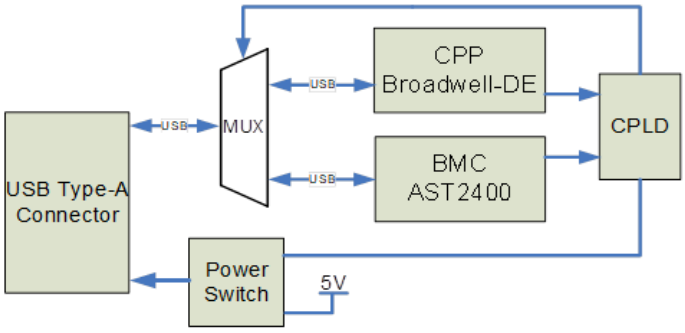


Figure 5-13 USB Interface Diagram

5.7.5 Network Synchronization Ports

- 1x GNSS port with SMA antenna interface
- 1x ToD port with RJ45 form factor
- 2x SMA ports with 1PPS and 10MHz ref. clock input/output

5.8 Power Consumption

System consumes the maximum power @ 50°C with full traffic loading & all fans runs at max. 16000RPM. The actual system power consumption will be calculated based on Beta verification data.

Per system power estimation data, the switch board power consumption is with below configuration: timing interface & BMC works normally, 2x port RJ45 loopback with 0.3W power, 2x port SFP+ loopbacks with 1.5W power, 48x port QSFP28 loopback with 3.5W, MAC runs at 9600Gpbs traffic switching/forwarding, 4x FAN modules runs at 16000RPM.

Measurement of Broadwell-DE CPU (8-core/2.0GHz) with 64GB RDIMM and 128GB SSD is 83W max.

System total input power consumption measured by power meter is 1023W.

6 Field Replaceable Components

6.1 Fan Module

A newly developed FAN tray with an 80mm x 80mm x 38mm FAN is adopted on the S9600-48X system to meet chassis depth requirements.

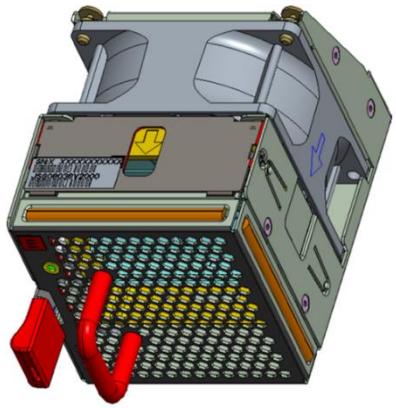


Figure 6-1 8038 FAN Module

6.1.1 Electrical Specifications

Rated voltage	12VDC
Rated current	3.5A MAX
Rated power consumption	48W MAX
Operating voltage range	10.8VDC ~ 13.2VDC
Operating temperature	-20 ~ +70
Rated speed	16100 +/- 1610 min-1
Acoustic noise	73dB MAX

Table 6-1 FAN Tray Characteristics

6.2 Power Supply

The S9600-48X adopts two kinds of 1600W hot swappable power supplies. The PSU modules are supported: One is 220Vac input to +12.2Vdc output AC/DC PSU, the other is -48Vdc input to +12.2Vdc output DC/DC PSU.

6.2.1 Physical Size

The physical size of the power supply enclosure is intended to accommodate the power range of up to 3000W. The physical size is 40mm x 68mm x 430mm (height x width x length).

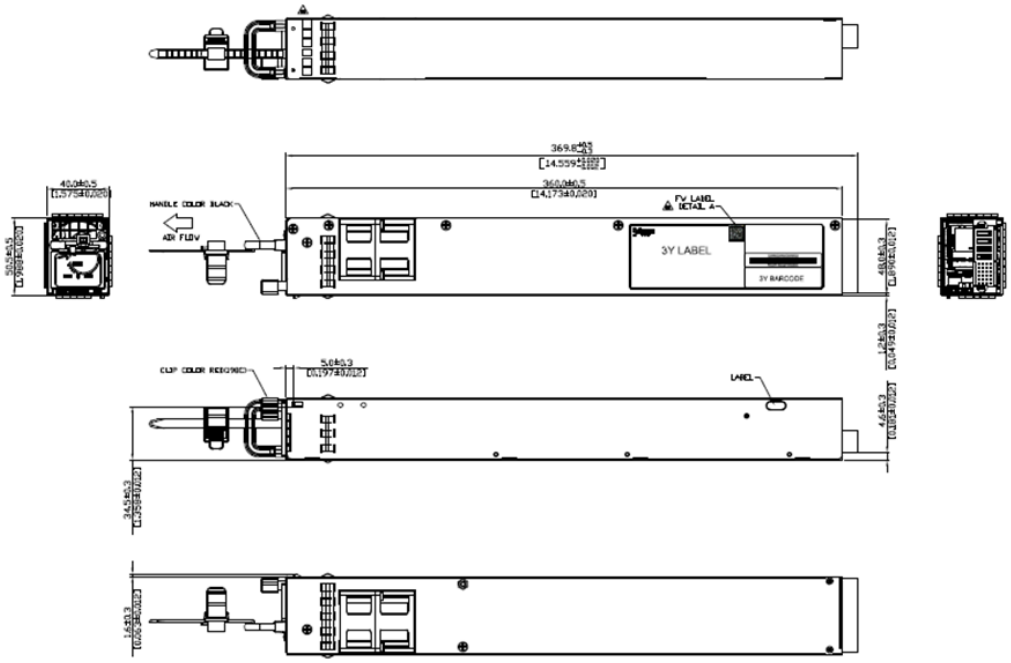


Figure 6-2 1600W AC/DC Power Supply Dimension

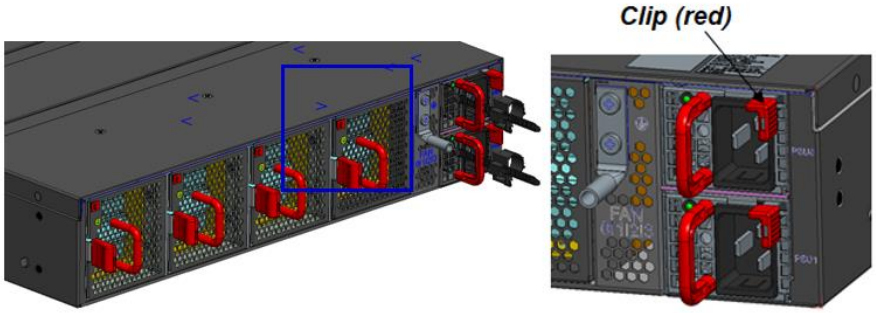


Figure 6-3 System with 1600W AC/DC Power Supply

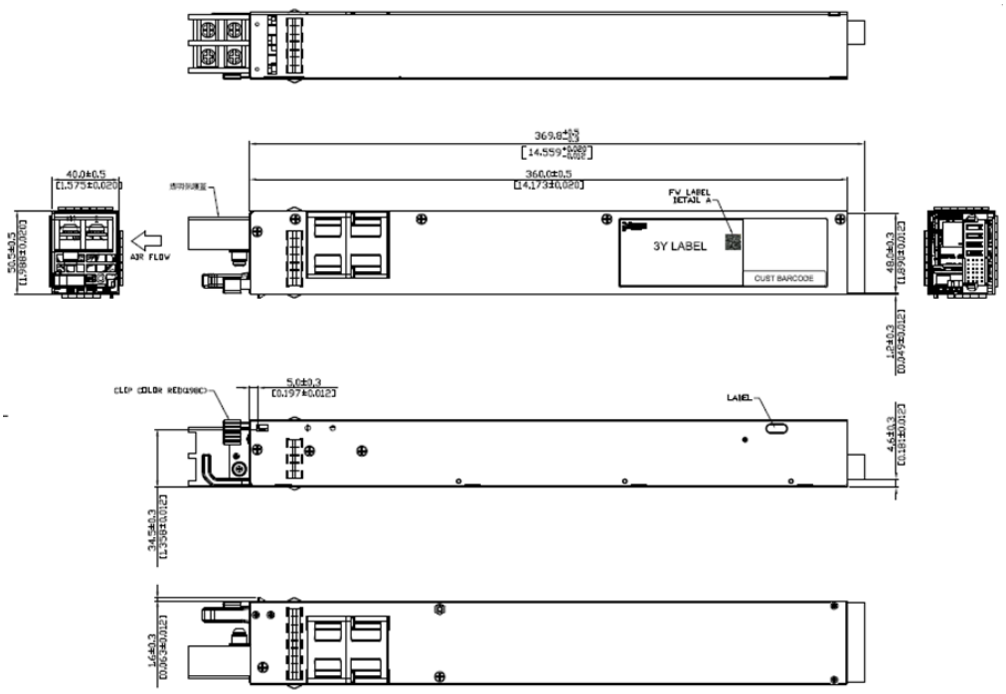


Figure 6-4 1600W DC/DC Power Supply Dimension

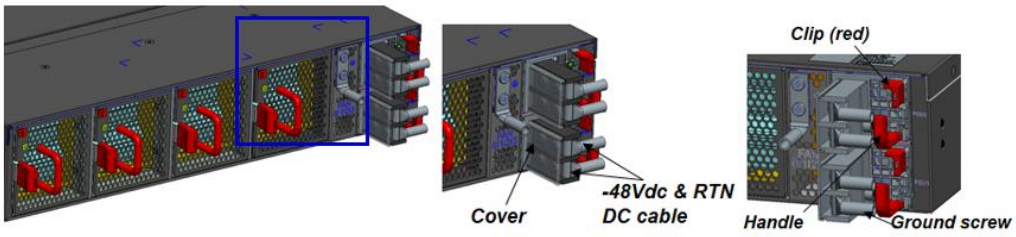


Figure 6-5 System with 1600W DC/DC Power Supply

6.2.2 Electrical Specifications

The detailed electrical specifications of AC/DC PSU are shown as below:

INPUT SPECIFICATIONS	
Input Voltage Range	90~264Vac
Input Frequency	47-63 Hz
Input Current	13A max.
Inrush Current	100A max.
OUTPUT SPECIFICATIONS	
Output Voltage (Volts)	+12.2V
Output Current (Amps)	90~264Vac:82A(+12.2V), 1000W 180~264Vac:131A(+12.2V), 1600W The output capacity varies depending on the input voltage, so for 1600W AC PSU the low-line 110Vac is disabled.

Max Power (Watt)	1600W@180~264Vac
Output Voltage (Volts)	+5VSB
Output Current (Amps)	5A (+5VSB)
Efficiency	80Plus Platinum >90% @20% load, >94 @50% load, >91% @100% load
Ripple P-P (mV) (max.)	+12.2V:200mV, +5VSB:50mV
Total Regulation	+12.2V:±5%, +5VSB:±5%
GENERAL SPECIFICATIONS	
Hold-up Time (min.)	10msec
Over Voltage Protection	Latch off
Over Current & Short Circuit Protection	Latch off
Over Temperature Protection	Auto Recovery
FAN Failure Protection	Auto Recovery
Hot Swap	Yes, 1+1 redundant
Load Sharing	Yes
Hi-pot	1800Vac
ENVIRONMENTAL SPECIFICATIONS	
Operating Temperature Range	–5°C to 50°C
Storage Temperature Range	–40°C to +70°C
Humidity, Non-Condensing	Operating: 0 to 90% RH, Non-operating: 0 to 95% RH
EMI	Meets FCC part 15/CISPR 22 Class A(under 6dB)

Table 6-2 AC/DC Power Supply Specification

The detailed electrical specifications of Neg48 DC/DC PSU are shown as below:

INPUT SPECIFICATIONS	
Input Voltage Range	-40 ~ -72Vdc
Input Current	60A max.
Inrush Current	100A
OUTPUT SPECIFICATIONS	
Output Voltage (Volts)	+12.2V
Output Current (Amps)	131A(+12.2V), 1600W
Max Power (Watt)	1600W@-40~-72Vdc
STB Output Voltage (Volts)	+5VSB
STB Output Current (Amps)	5A (+5VSB)
Efficiency	>88% @20% load, >92 @50% load, >91% @100% load
Ripple P-P (mV) (max.)	+12.2V:120mV, +5VSB:50mV
Total Regulation	+12.2V:±5%, +5VSB:±5%
GENERAL SPECIFICATIONS	
Hold-up Time (min.)	1msec
Over Voltage Protection	Latch off

Over Current & Short Circuit Protection	Latch off
Over Temperature Protection	Auto Recovery
FAN Failure Protection	Auto Recovery
Hot Swap	Yes, 1+1 redundant
Load Sharing	Yes
Hi-pot	1500Vdc
ENVIRONMENTAL SPECIFICATIONS	
Operating Temperature Range	–5°C to 50°C
Storage Temperature Range	–40°C to +70°C
Humidity, Non-Condensing	Operating: 0 to 90% RH, Non-operating: 0 to 95% RH
EMI	Meets FCC part 15/CISPR 22 Class A(under 6dB)

Table 6-3 DC/DC Power Supply Specification

6.2.3 PSU LED Status Information

Power supply condition	Power supply LED
Output ON and OK.	Green
No input power to all power supplies.	Off
PSU standby state input power present / Only +5VSB on.	1Hz Flashing Green
Input power cord unplugged or input power lost with a second power supply in parallel still with AC input power.	1Hz Flashing Red
Power supply critical event causing a shutdown, failure, over current, short circuit, over voltage, fan failure, over temperature.	Red
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	Flashing 1sec Red and 1sec Green
Power supply FW updating (Boot-loader mode).	2Hz Flashing Green

Table 6-4 LED Status Information of PSU

7 Software Support

The S9600-48X supports a base software package composed of the following components:

BIOS

The S9600-48X Supports AMI AptioV BIOS with the x86 CPU module

BMC

The S9600-48X Supports AMI MegaRAC SP-X BMC firmware for Aspeed AST2400 platform.

ONIE

See http://onie.org/ for the latest supported version

8 Compliance

Environmental	
Operating temperature	0 ~ 45°C (at sea level with Fan Failure condition)
Storage temperature	-40~70°C (–40°F to 158°F)
Altitude	0~10,000ft at 45°C
Operating relative humidity	0%-85% RH (non-condensing)
Storage relative humidity	0%-85% RH (non-condensing)
Acoustic	76dB at 27°C
Dimensions (height x width x depth)	436.0 mm (W) x 790.0 mm (D) x 87.7 mm (H)
Weight	24.68kg

Regulatory Compliances	
Safety	UL 62368-1 IEC/EN 60950-1 IEC/EN 62368-1 BSMI CNS 14336-1 UL 60960
EMC	FCC Part 15, Subpart B, Class A; EN55032, Class A EN 300 386 EN 55024 EN 301 489-1 EN 301 489-19 EN 303413 BSMI (CNS 13438), Class A

9 Appendix A – Requirements for IC Approval

Requirements	Details	Link to Section
Contribution License Agreement	OCP CLA, OCPHL Permissive	Section 1
Are all contributors listed in Section 1: License?	Yes	Section 1
Did All the Contributors sign the appropriate license for this spec? Final Spec Agreement/HW License?	Yes	Section 1
Which 3 of the 4 OCP Tenets are supported by this Spec?	Openness Efficiency Impact Scale	UfiSpace IC Presentation (Tenets on slide 9)
Is there a Supplier(s) that is building a product based on this Spec? (Supplier must be an OCP Solution Provider)	Yes	UfiSpace (OCP Solution Providers Directory)
Will Supplier(s) have the product available for GENERAL AVAILABILITY within 120 days?	Yes	Appendix B

10 Appendix B – UfiSpace – OCP Supplier Information

Table of supplier information for the S9600-48X Open Aggregation Router

Supplier Information	
Company	Ufi Space Co. Ltd.
Contact Info	sales@ufispace.com
Product Name	Open Aggregation Router
Product SKU#	S9600-48X
Link to Product Landing Page	S9600-48X

Summary of supplier requirements

Requirements	Details	Link to Section
Which Product recognition?	NA	
If OCP Accepted™, who provided the Design Package?	NA	
2021 Supplier Requirements for your product(s)	Yes	Pending Approval