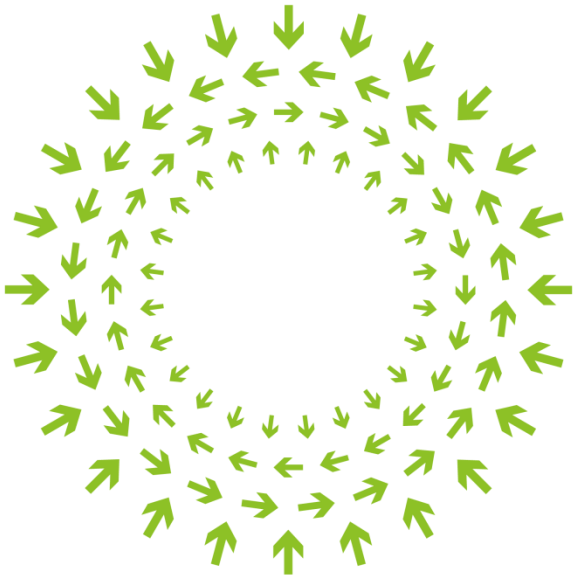

OPEN Compute Project

UfiSpace S9500-30XS

Cell Site Gateway Router Specification

Revision 1.0

Author: Hector Zhang

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Revision History

Revision	Date	Author	Description
1.0	Jan 8, 2019	Hector Zhang	Initial Draft

Table of Contents

1 Overview

This document describes the technical specifications of the S9500-30XS switch designed for Telco service application.

By providing 10GbE, 25GbE, 100GbE high speed Ethernet ports and PTP/1588V2, SyncE timing synchronization features, S9500-30XS Telco switch enables service providers to deliver next-generation technologies such as 5G mobile Ethernet network, which requires higher data bandwidth and more precise timing synchronization.

With temperature-hardened, high port density, high-throughput, small form factor, low-power-consumption & redundancy (PSU and FAN) features, S9500-30XS Telco switch delivers high system reliability, Ethernet switching performance and intelligence to the network edge in a flexible 1U form factor that helps reduce infrastructure and administrative costs.

1.1 Physical Overview

Front View

Rear View

Figure 1-1 S9500-30XS ID Rendering

1.2 Feature Summary

- 1+1 redundant power supply unit
  - 400W output
  - -36~72V DC input
  - Field replaceable
- 4+1 redundant fan module
  - 25000 RPM
  - Front to back air flow
  - Field replaceable
- Ethernet data ports:
  - 20 x 10GbE SFP+ ports
  - 8 x 25GbE SFP28 ports
  - 2 x 100GbE QSFP28 ports
- Timing Synchronization:
  - 1588V2 and SyncE with T-GM, T-TSC, T-TC, T-OC, T-BC support
  - Input source : GNSS/GPS, E1/T1, ToD, 1PPS and 10MHz
  - Output source : 1PPS and 10MHz
- Front/Real panel LED indicators:
  - 1 x power status LED
  - 1 x FAN status LED
  - 1 x system status LED
  - 1 x synchronization status LED
  - 1 x GNSS\GNSS status LED
  - Per port FAN status LED
  - Per port PSU status LED
  - Per port link status LED
- Management interfaces:
  - 1 x GbE OOB management port (CPU)
  - 1 x USB2.0 Type-A general purpose port
  - 1 x RS232 console port in RJ45 form factor
  - 1 x USB console port in Micro USB form factor
  - 1 x tact switch for system reset/reload default configuration

1.3 Mechanical Outline

S9500-30XS chassis is designed to meet cabinet with 19'' depth installation requirement. This 1RU system mechanical dimension is: 440mm (W) x 302mm (D) x 43.5mm (H).

Dimensions

	Inches	Millimeters
Length	11.89	302
Width	17.32	440
Height	1.71	43.5

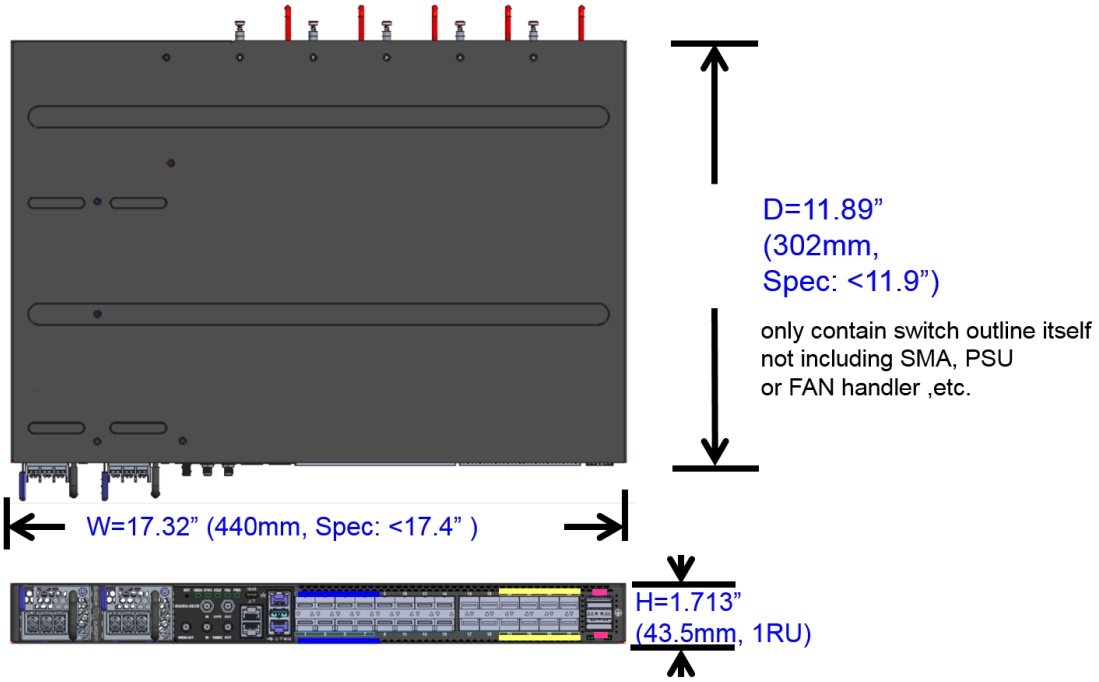


Figure 1-2 S9500-30XS Mechanical Outline

1.4 System Explode Plot

Below shows the S9500-30XS system explode view, main board will be populated into the base chassis and then follow by FAN control board，air baffle together with MB, FAN card will be fixed by screw. Next step CPU card will be installed into the right angle PCIe connector and fixed with standoff/screw. FAN and PSU modules will be plugged into FAN & PSU slots after chassis top cover is fixed.

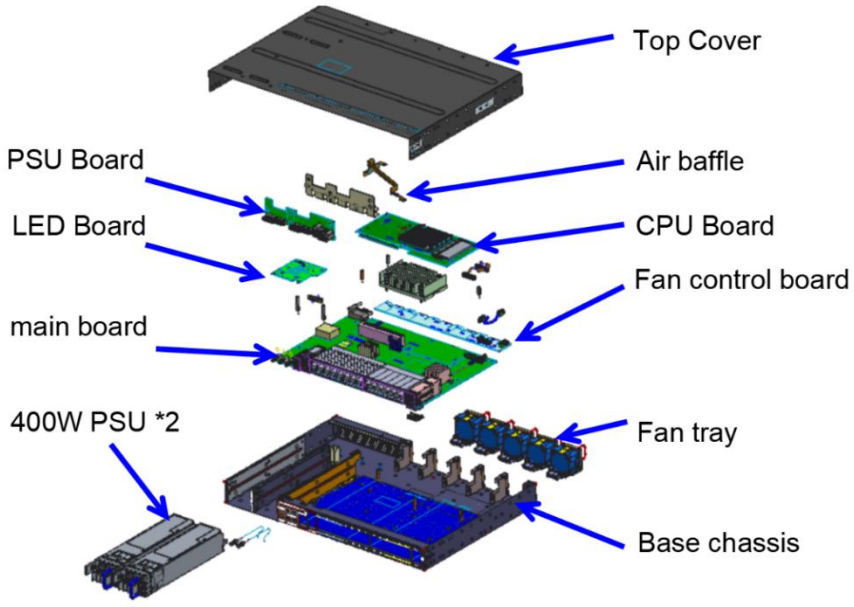


Figure 1-3 S9500-30XS System Explode Plot

S9500-30XS system top view without top cover is shown as below:

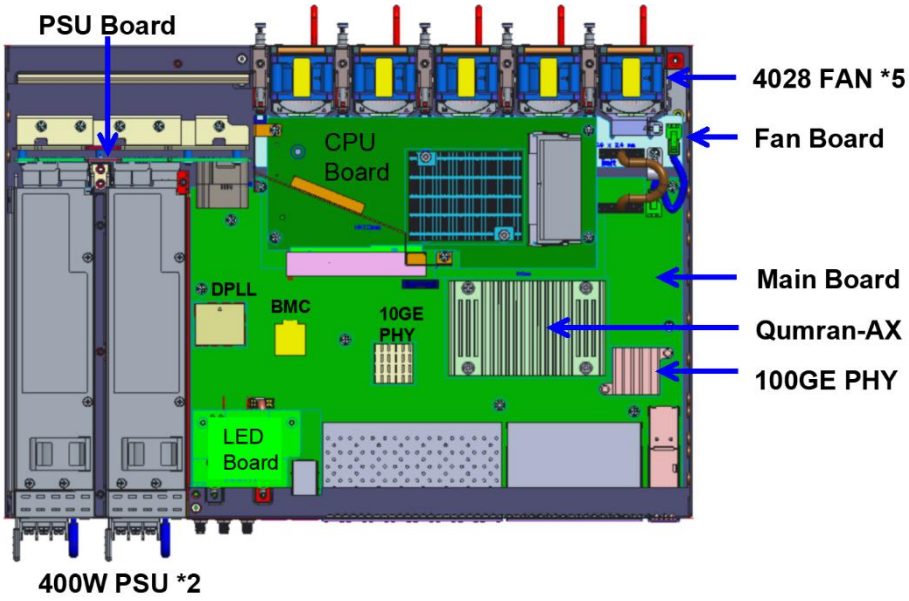


Figure 1-4 S9500-30XS System Top View

2 Hardware Architecture

This section describes key features, system block diagram and major component used on the S9500-30XS Telco switch.

2.1 Component Summary

- PCBA:
  - 1 x Switch board
  - 1 x CPU card
  - 1 x FAN card
  - 1 x PDB card
  - 1 x LED card
- On board key components:
  - Switch Board
    - 1 x MAC Qumran-AX BCM88470
    - 6 x 512MB DDR4 SDRAM @ 1200MHz
    - 1 x Octal port 10GbE PHY BCM82780F
    - 1 x Dual port 100GbE PHY BCM82398
    - 1 x management CPLD 10M04SAU169I7G
    - 1 x PCIe NIC controller I210-IT for CPU
    - 1 x SyncE & IEEE 1588 DPLL 82P33831
    - 1 x Clock jitter attenuator buffer Si5344D
    - 1 x GNSS/GPS module NEO-M8T
    - 1 x T1/E1 transceiver 82P2281
  - CPU Card
    - 1 x CPU Broadwell-DE D-1519 with quad core @ 1.5GHz
    - 2 x 8GB DDR4 SODIMM memory module with ECC support
    - 1 x 128GB SATA3 M.2 SSD Memory module
- PSU& FAN:
  - 2x 400W slim PSUs with redundancy support
  - 5x 4028 FAN tray modules with redundancy support

2.2 Front & Real Panel Design

➢ S9500-30XS front panel IO ports & LED include below functionalities:

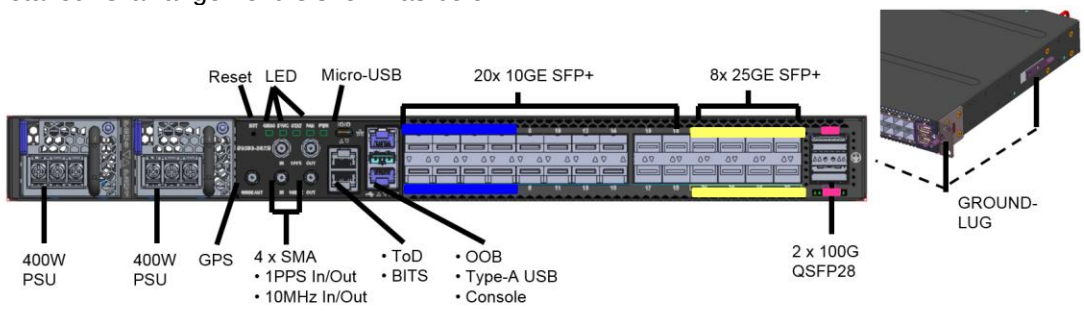
- Ethernet data ports
  - ✓ 2x 100G QSFP28 ports
  - ✓ 8x 25G SFP28 ports
  - ✓ 20x 10G SFP+ ports
- Timing synchronization ports
  - ✓ 1x GNSS port with SMA connector
  - ✓ 1x T1/E1 port with RJ45 form factor
  - ✓ 1x ToD port with RJ45 form factor
  - ✓ 4x SMA ports with 1PPS and 10MHz ref. clock input/output
- Management ports (Share between CPU and BMC)
  - ✓ 1x OOB port
  - ✓ 1x Type A USB port
  - ✓ 1x console port in RJ45
  - ✓ 1x console port in Micro-USB

- System status LED
  - ✓ Power status LED
  - ✓ FAN status LED
  - ✓ GNSS status LED
  - ✓ Synchronization status LED
- Ethernet ports LED
  - ✓ OOB copper ports LED
  - ✓ Data traffic fiber ports LED

➢ S9500-30XS Real panel design:

- FAN module
- FAN status LED

Detailed IO arrangement is shown as below:



Note: The blue bar under the I/O means those ports are capable for ER/ZR optics module.

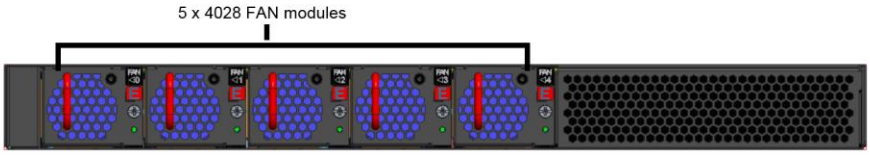


Figure 2-1 Front Panel IO Arrangement

2.2.1 LED Indicators

The front panel system status LED are placed on LED card.

System LED Function/State	Meaning	Comment
PWR (Green/Yellow):		
OFF	No power.	
Solid Green	System power good	
Blinking Green	Heater is in process	
Solid Yellow	System power good but heater heating failed	
Blinking Yellow	System DC/DC power fail	
FAN (Green/Yellow):		

System LED Function/State	Meaning	Comment
OFF	No power.	
Solid Green	All FAN modules work well	
Blinking Green	FANs are turned off in -30~-40°C environment	
Solid Yellow	One FAN module fail but system works well	
Blinking Yellow	One more FAN modules fail and need fix ASAP	
STATUS (Green/Yellow):		
OFF	System is powered off	
Solid Green	System boot complete	
Blinking Green	System in booting	
Solid Yellow	BMC or BIOS boot failed	
Blinking Yellow	Reserved.	
GNSS (Green/Yellow):		
OFF	GNSS active antenna is open or not installed	
Solid Green	GNSS works well	
Blinking Green	System is locked to GNSS	
Solid Yellow	GNSS acquisition or tracking fail	
Blinking Yellow	GNSS antenna is short to ground	
SYNC (Green/Yellow):		
OFF	System timing/clock synchronization is disabled (Don't synchronize to external clock reference)	
Solid Green	System timing/clock is synchronized to external timing/clock reference (ex: GNSS, 1PPS, PTP, BITS, etc)	
Blinking Green	Reserved	
Solid Yellow	System timing/clock synchronization is in free-run or holdover mode	
Blinking Yellow	Reserved	

Table 2-1 System LED Descriptions

For SFP+, SFP28 and QSFP28 ports are controlled by serial LED interface of MAC.

Ethernet LED Function/State	Meaning	Comment
SFP+（port 0~19）(Green/Yellow):		
OFF	No link on the SFP+ port	
Solid Green	SFP+ port link at 10G mode	
Blinking Green	SFP+ port is transmitting at 10G mode	
Solid Yellow	SFP+ port link at 1G/100M mode	
Blinking Yellow	SFP+ port is transmitting at 1G/100M mode	

Ethernet LED Function/State	Meaning	Comment
SFP28 （port 20~27） (Green/Yellow):		
OFF	No link on the SFP28 port	
Solid Green	SFP28 port link at 25G mode	
Blinking Green	SFP28 port is transmitting at 25G mode	
Solid Yellow	SFP28 port link at 10G/1G mode	
Blinking Yellow	SFP28 port is transmitting at 10G/1G mode	
QSFP28 （port 28~29） (Green/Yellow):		
OFF	No link on the QSFP28 port	
Solid Green	QSFP28 port link at 100G mode	
Blinking Green	QSFP28 port is transmitting at 100G mode	
Solid Yellow	QSFP28 port link at 40G mode	
Blinking Yellow	QSFP28 port is transmitting at 40G mode	
QSFP28 （port 28~29）(With break out cable) (Green/Yellow):		
OFF	No link on the QSFP28 port	
Solid Green	QSFP28 port link at 25G mode	
Blinking Green	QSFP28 port is transmitting at 25G mode	
Solid Yellow	QSFP28 port link at 10G mode	
Blinking Yellow	QSFP28 port is transmitting at 10G mode	
OOB port (Green/Yellow):		
OFF	No link on the OOB port	
Solid Green	OOB port link at 1G mode	
Blinking Green	OOB port is transmitting at 1G mode	
Solid Yellow	OOB port link at 10/100M mode	
Blinking Yellow	OOB port is transmitting at 10/100M mode	

Figure 2-2 S9500-30XS SFP+, SFP28 and QSFP28 Port LED

2.2.2 Network Ports

2.2.2.1 Ports Assignment

Figure 2-3 Physical Ports Assignment

Table below shows the network ports numbering & speed:

Function	Port#	Speed	Notes
SFP+ Ports	P0	100M/1G/10G	ZR optics capable
	P1	100M/1G/10G	ZR optics capable
	P2	100M/1G/10G	ZR optics capable
	P3	100M/1G/10G	ZR optics capable
	P4	100M/1G/10G	ZR optics capable
	P5	100M/1G/10G	ZR optics capable
	P6	100M/1G/10G	ZR optics capable
	P7	100M/1G/10G	ZR optics capable
	P8	100M/1G/10G	PHY-less port
	P9	100M/1G/10G	PHY-less port
	P10	100M/1G/10G	PHY-less port
	P11	100M/1G/10G	PHY-less port
	P12	100M/1G/10G	PHY-less port
	P13	100M/1G/10G	PHY-less port
	P14	100M/1G/10G	PHY-less port
	P15	100M/1G/10G	PHY-less port
	P16	100M/1G/10G	PHY-less port
	P17	100M/1G/10G	PHY-less port
	P18	100M/1G/10G	PHY-less port
	P19	100M/1G/10G	PHY-less port
SFP28 Ports	P20	1G/10G/25G	PHY-less port
	P21	1G/10G/25G	PHY-less port
	P22	1G/10G/25G	PHY-less port
	P23	1G/10G/25G	PHY-less port
	P24	1G/10G/25G	PHY-less port
	P25	1G/10G/25G	PHY-less port
	P26	1G/10G/25G	PHY-less port
	P27	1G/10G/25G	PHY-less port
QSFP28 Ports	P0-0	10G/40G/100G	ER4 optics capable
	P0-1	10G/40G/100G	ER4 optics capable
	P0-2	10G/40G/100G	ER4 optics capable
	P0-3	10G/40G/100G	ER4 optics capable
	P1-0	10G/40G/100G	ER4 optics capable
	P1-1	10G/40G/100G	ER4 optics capable
	P1-2	10G/40G/100G	ER4 optics capable
	P1-3	10G/40G/100G	ER4 optics capable

Figure 2-4 Network Port Connection

2.2.2.2 Ports Mapping

Front Panel		PHY				MAC			
Function	Port#	DEVICE	PORT#	MIIM	MIIM ADDR	DEVICE	SerDes Core	PORT#	Interface
SFP+ Ports	P0	BCM82780F	0	M1	00001	MAC BCM88470	PM10Q-6	24	XFI SFI
	P1		1		00010			26	
	P2		2		00011			25	
	P3		3		00100			27	
	P4		4		00101		PM10Q-5	23	
	P5		5		00110			22	
	P6		6		00111			21	
	P7		7		01000			20	
	P8	MAC Internal SerDes					PM10Q-4	19	
	P9							18	

Front Panel		PHY				MAC			
Function	Port#	DEVICE	PORT#	MIIM	MIIM ADDR	DEVICE	SerDes Core	PORT#	Interface
	P10							17	
	P11							16	
	P12						PM10Q-8	32	
	P13							33	
	P14							34	
	P15							35	
	P16						PM10Q-9	36	
	P17							37	
	P18							38	
	P19							39	
SFP28 Ports	P20	MAC Internal SerDes					PM25-3	12	
	P21							13	
	P22							14	
	P23							15	
	P24						PM25-2	8	
	P25							9	
	P26							10	
	P27							11	
QSFP28 Ports	P0-0	BCM82398	4-7	M0	00001	MAC BCM88470	PM25-1	3	CAUI4
	P0-1							2	
	P0-2							1	
	P0-3							0	
	P1-0		0-3		00101		PM25-0	7	
	P1-1							6	
	P1-2							5	
	P1-3							4	
CPU MAC	Lane0					MAC BCM88470	PM10-7	30	10G-KR
	Lane1							28	10G-KR
								29	
								31	
OOB Port	P1 (CPU)	I210-IT #1	1	PCIe		CPU Broadwell-DE			PCIe

2.2.3 OOB Ports

The S9500-30XS switch includes 1standard GbE RJ45 port for out of band (OOB) management, shared between CPU and BMC. It supports the IEEE 802.3 specification for 10/100/1000Mbps operation.

PCIe interface is routed between CPU & NIC I210-IT, OOB supports 10/100/1000Mbps operation. NC-SI is connected between BMC & NIC I210-IT, OOB speed is limited to 100Mbps in this case.

OOB to BMC can be disabled by BIOS.

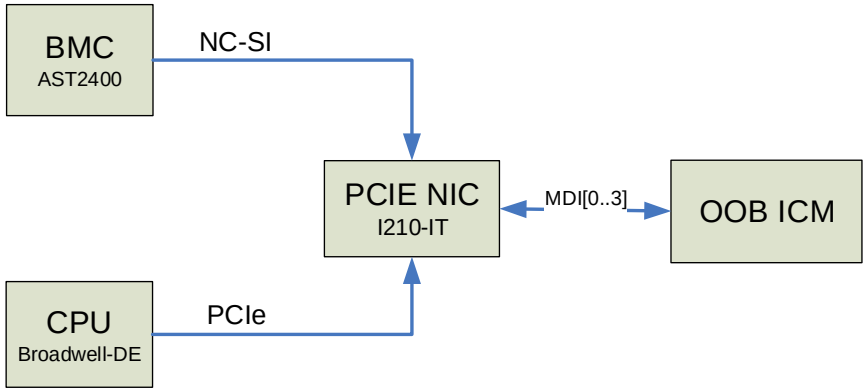


Figure 2-5 CPU OOB Interface Diagram

2.2.4 Console Port

Two console ports available for S9500-30XS systems access, RS232 & Micro USB console. Both of them can be used for CPU or BMC access. The bound rate is 115200 by default. When either console port cable is plugged, it's active immediately, RJ45 port has higher priority when both ports are present. Console port connection diagram is shown as below:

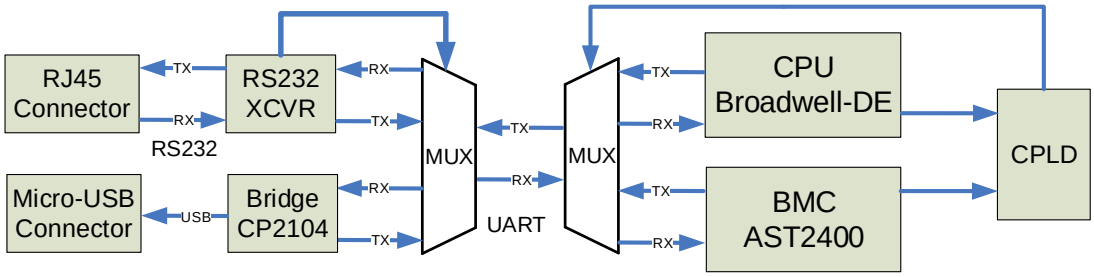


Figure 2-6 Console Interface Diagram

To use the Micro-USB console port, CP2102N driver need to be installed on host PC side.

To access the RJ45 RS232 interface, use a RS-232 to RJ45 adapter. Also, RJ45 RS232 is higher priority than Micro-USB and only activate RJ45 RS232 access if both interfaces are connected by user. The pin definition of the RS232 console port is shown as below.Pin3 is the TX signal from internal processor to external RS232 interface, and Pin6 is the RX signal from external RS232 interface to internal processor.

PIN #	Definition	Direction	Note
1	NC		
2	NC		
3	UART_TXD	Out	Console TX
4	GND		
5	GND		
6	UART_RXD	In	Console RX
7	GND		
8	GND		

Table 2-2 Pin Definition of RJ45 Console Connector

2.2.5 Synchronization Ports

- 1x GNSS port with SMA antenna interface
- 1x BITS(T1/E1) port with RJ45 form factor
- 1x ToD port with RJ45 form factor
- 2x SMA ports with 1PPS and 10MHz ref. clock input
- 2x SMA ports with 1PPS and 10MHz ref. clock output

2.3 Power Consumption & Thermal Monitoring

2.3.1 Power Consumption

System consumes the maximum power @ 65°C with full traffic loading & all FAN runs at max. 25000RPM. The actual system power consumption will be calculated based on Beta verification data.

Per system power estimation data, the switch board power consumption is around 240W with below configuration: timing interface & BMC works normally, 28x port SFP+ loopbacks with 1.5W power, 2x port QSFP28 loopback with 3.5W power, 6x DDR4 SDRAM packet buffer enabled, MAC & 10G,100G PHY runs at 300Gpbs traffic switching/forwarding, 5x FAN modules runs at 25000RPM.

Measurement of existing Broadwell-DE CPU (4-core/2.2GHz) with 16GB SODIMM and 128GB SSD is 60W max.

System total power consumption: 240 + 60W = Max. 300W

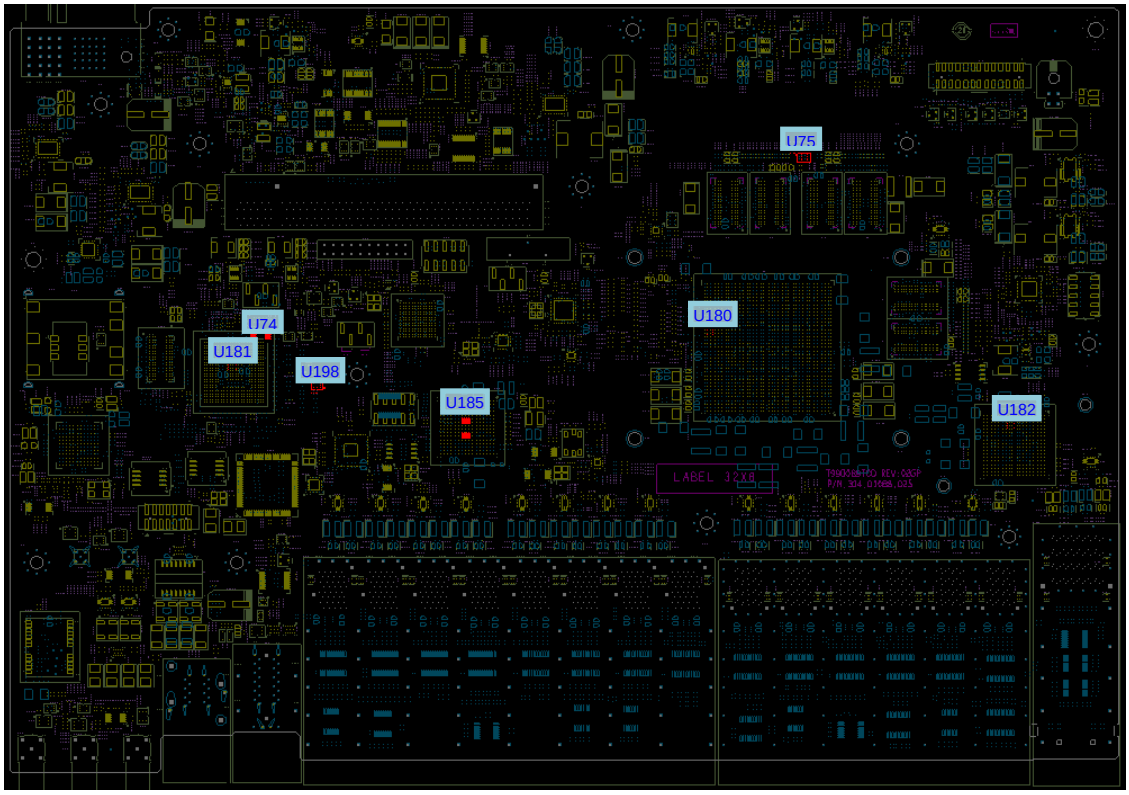
To consider PSU efficiency 90% from -48V to +12V, overall system power requirement will be 300 / 0.9 = 333.3W.

2.3.1 Thermal Monitoring

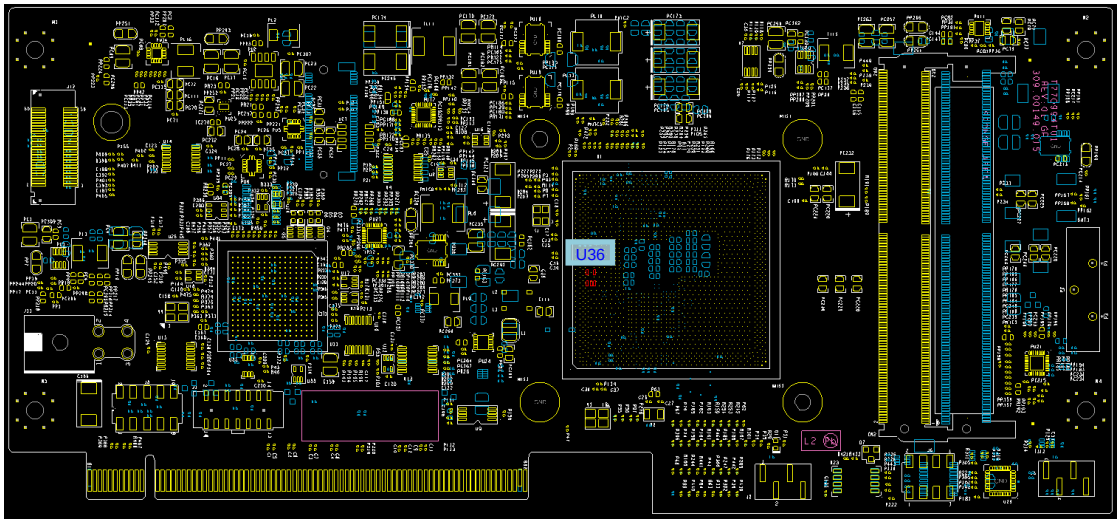
BMC controls 5 fans for thermal management, based on the 7 thermal sensors on switch board & one on CPU board.

Location	Component	Function
U74	LM75	Monitor BMC temperature
U75	TMP451	Monitor DDR4 & MAC temperature
U180	TMP235	Monitor MAC temperature
U181	TMP235	Monitor BMC temperature
U182	TMP235	Monitor 100G PHY temperature
U185	LM75	Monitor 10G PHY temperature
U198	TMP235	Monitor ambient temperature

Switch board thermal sensor locations:



CPU card thermal sensor location:



2.4 Switching Subsystem

This section details switch board component features/functionalities summary and hardware system design.

2.4.1 Switch Board Block Diagram

S9500-30XS system functional block diagram is shown as below:

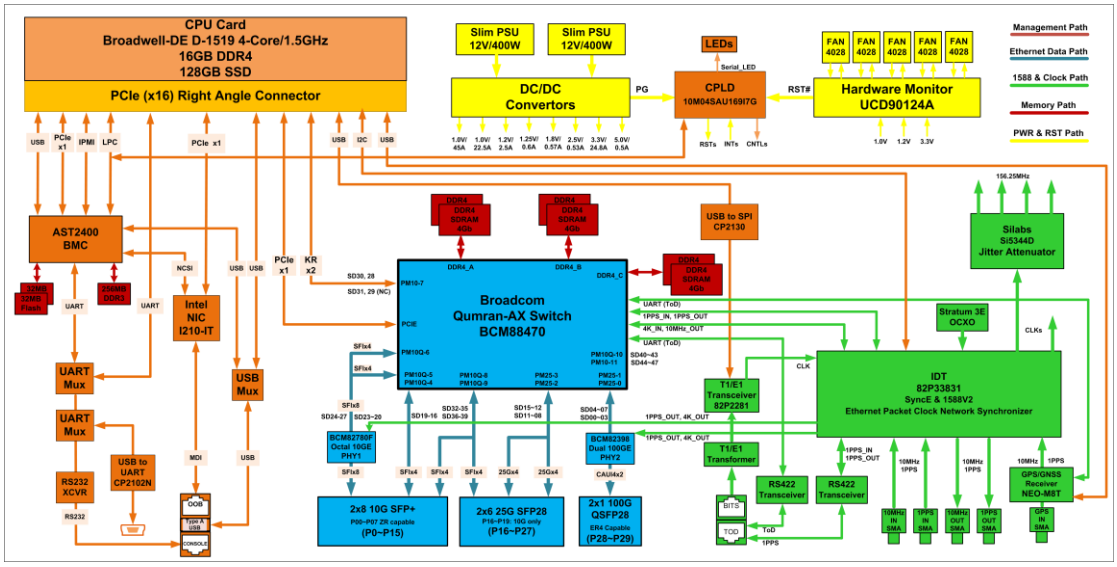


Figure 2-7 Switch Board Block Diagram

2.4.2 Switch Board PCB Placement

S9500-30XS switch main board placement is shown as below, parts highlight in yellow are installed on PCB top side while components in blue are staffed on bottom side:

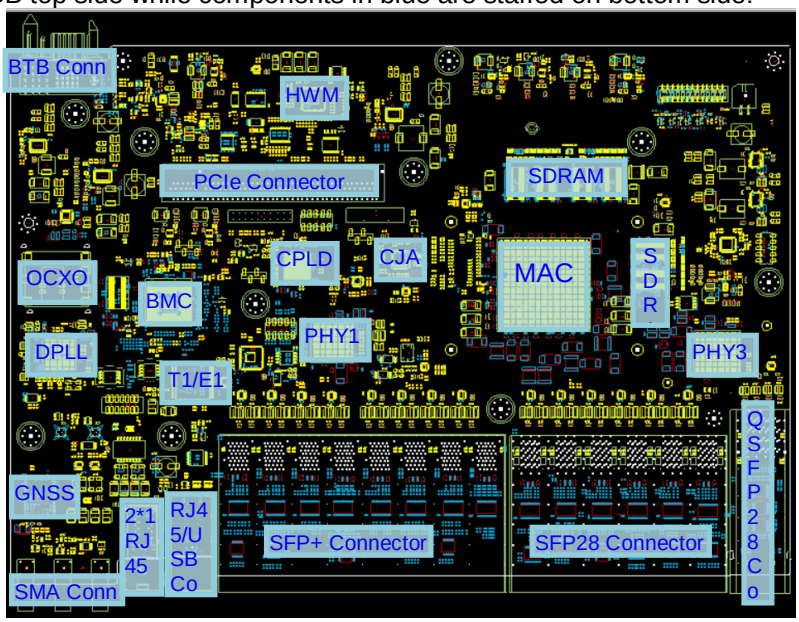


Figure 2-8 Switch Board PCB Layout

Main Board Key Components

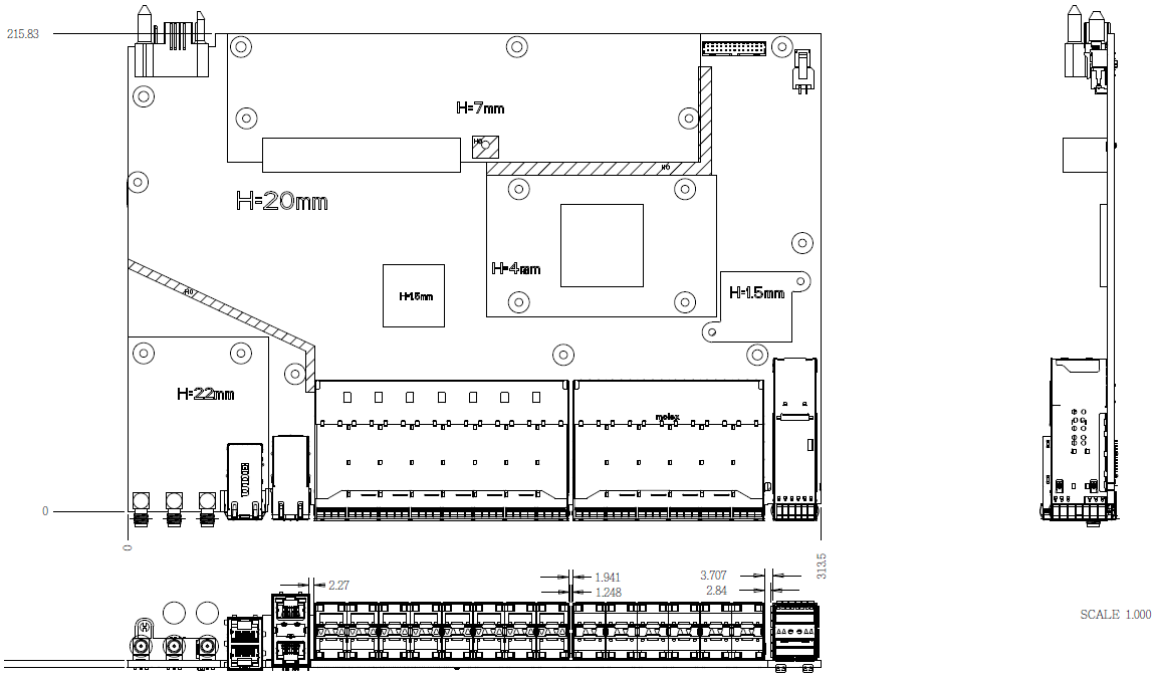
Description	Manufacturer	Manufacturer Part Number
300G MAC	Broadcom	BCM88470CB0IFSBG
DDR4 SDRAM	Micron	MT40A256M16GE-083E IT:B
100G PHY	Broadcom	BCM82780FA3IFSBG
10G PHY	Broadcom	BCM82398AIFSBG

Max 10 CPLD	Atera/Intel	10M04SAU169I7G
BMC	Aspeed	AST2400A1-GP
NIC	Intel	WGI210IT SLJXQ
HWM	TI	UCD90124ARGCR
DPLL	IDT	82P33831ABAG
Clock jitter attenuator	SiLabs	SI5344D-D09285-GMR
T1/E1 transceiver	IDT	82P2281PFG
GNSS Module	U-Blox	NEO-M8T-0
PCIe Connector	MERITEC	98317C-164-2MMF
BTB Connector	MOLEX	46437-1044
QSFP28 Connector	MOLEX	171722-6001
SFP28 Connector	AMPHENOL	UE86-K8627-20321
SFP+ Connector	AMPHENOL	UE86-3G6620-20361
RJ45/USB Combo	UDE	0D-FN-0001
2*1 RJ45 Connector	UDE	M1A-FN-0005
SMA Connector	ACES	309690012D

2.4.3 Switch Board PCB Dimensions

Main Board Dimensions

Main Board	Inches	Millimeters
Width	12.35	314
Depth	9.89	216



2.4.4 Switch Board PCB Stack-up

S9500-30XS switch board PCB stack up: 20 layers, material: TU883 or equivalent:

20-Layers Board Stackup (Material TU883)											Trace Impedance Control		
Stackup			Material		GCE TU883 Stack_up						50ohm	90ohm	100ohm
Layer Name	Layer Description	Reference	Type	Material	Structure	DF/3GHz	Dk/3GHz	Layer Thickness (mil)	Copper Weight (oz)		Design Suggestion	Design Suggestion	Design Suggestion
	Solder Mask		Solder Mask		SM			0.5					
L1_Top	SIGNAL	L2	Copper		0.5+plating			2.1	0.5+plating		6.2/50	5.2/4.8/89.8	4.5/6.0/99.7
	PREPREG			TU883	1078	TBD	TBD	2.97		GCE	5.5/49.93	4.8/5.2/90.43	4.1/6.4/100.15
L2_Plane 1	GND		Copper		1 oz HVLP			1.25	1				
	CORE			TU883	4 mil core 3313	0.0034	3.82	4					
L3_Plane 2	SIGNAL	L2/L4	Copper		1 oz HVLP			1.25	1		5.0/49.7	5.1/5.6/89.8	4.2/6.8/100.6
	PREPREG			TU883	1078*2	0.003	3.59	5		GCE	4.6/50.14	5/5.7/89.67	4.2/6.8/99.54
L4_Plane 3	GND		Copper		1 oz HVLP			1.25	1				
	CORE			TU883	4 mil core 3313	0.0034	3.82	4					
L5_Signal 1	SIGNAL	L4/L6	Copper		1 oz HVLP			1.25	1		5.0/49.7	5.1/5.6/89.8	4.2/6.8/100.6
	PREPREG			TU883	1078*2	0.003	3.59	5		GCE	4.6/50.14	5/5.7/89.67	4.2/6.8/99.54
L6_Plane 4	GND		Copper		1 oz HVLP			1.25	1				
	CORE			TU883	4 mil core 3313	0.0034	3.82	4					
L7_Signal 2	SIGNAL	L6/L8	Copper		1 oz HVLP			1.25	1		5.0/49.7	5.1/5.6/89.8	4.2/6.8/100.6
	PREPREG			TU883	1078*2	0.003	3.59	5		GCE	4.6/50.14	5/5.7/89.67	4.2/6.8/99.54
L8_Plane 5	GND		Copper		1 oz RTF			1.25	1				
	CORE			TU883	8 mil core 3313*2	0.0034	3.82	8					
L9_Signal 3	PWR	L8/L10	Copper		1 oz RTF			1.25	1				
	PREPREG			TU883	1078*2	0.003	3.59	5					
L10_Plane 6	GND		Copper		1 oz RTF			1.25	1				
	CORE			TU883	4 mil core 3313	0.0034	3.82	4					
L11_Plane 7	GND		Copper		1 oz RTF			1.25	1				
	PREPREG			TU883	1078*2	0.003	3.59	5					
L12_Signal 4	PWR	L11/L13	Copper		1 oz RTF			1.25	1				
	CORE			TU883	8 mil core 3313*2	0.0034	3.82	8					
L13_Plane 8	GND		Copper		1 oz RTF			1.25	1				
	PREPREG			TU883	1078*2	0.003	3.59	5					
L14_Signal 5	SIGNAL	L13/L15	Copper		1 oz HVLP			1.25	1		5.0/49.7	5.1/5.6/89.8	4.2/6.8/100.6
	CORE			TU883	4 mil core 3313	0.0034	3.82	4		GCE	4.6/50.14	5/5.7/89.67	4.2/6.8/99.54
L15_Plane 9	GND		Copper		1 oz HVLP			1.25	1				
	PREPREG			TU883	1078*2	0.003	3.59	5					
L16_Signal 6	SIGNAL	L15/L17	Copper		1 oz HVLP			1.25	1		5.0/49.7	5.1/5.6/89.8	4.2/6.8/100.6
	CORE			TU883	4 mil core 3313	0.0034	3.82	4		GCE	4.6/50.14	5/5.7/89.67	4.2/6.8/99.54
L17_Plane 10	GND		Copper		1 oz HVLP			1.25	1				
	PREPREG			TU883	1078*2	0.003	3.59	5					
L18_Plane 11	SIGNAL	L17/L19	Copper		1 oz HVLP			1.25	1		5.0/49.7	5.1/5.6/89.8	4.2/6.8/100.6
	CORE			TU883	4 mil core 3313	0.0034	3.82	4		GCE	4.6/50.14	5/5.7/89.67	4.2/6.8/99.54
L19_Plane 12	GND		Copper		1 oz HVLP			1.25	1				
	PREPREG			TU883	1078	TBD	TBD	2.97					
L20_Bottom	SIGNAL	L19	Copper		0.5+plating			2.1	0.5+plating		6.2/50	5.2/4.8/89.8	4.5/6.0/99.7
	Solder Mask		Solder Mask		SM			0.5		GCE	5.5/49.93	4.8/5.2/90.43	4.1/6.4/100.15
Overall Board Thickness w/SM			3 mm					117.64					

Figure 2-9 S9500-30XS switch board PCB stack up

2.5 CPU Subsystem

Intel's x86 embedded SoC processor Broadwell-DE D1519 is equipped on S9500-30XS CPU board. The major onboard components and interfaces to switch board is listed as below:

- Intel's Broadwell-DE Processor
  - ✓ Capable of supporting up to 8-core processor
  - ✓ Two DDR4 ECC SO-DIMMs, up to 16GB
  - ✓ Single M.2 22*42mm SSD module up to 128GB
  - ✓ Dual 16MB SPI boot/BIOS flash components
- PCIe x16 gold finger to switch board
  - ✓ Single x4 PCIe Gen3 interface
  - ✓ Single x2 PCIe Gen2 interface
  - ✓ Two 10Gbps Ethernet interfaces
  - ✓ Two UART interfaces
  - ✓ Three USB interfaces
  - ✓ Three I2C interfaces

2.5.1 CPU Card Block Diagram

S9500-30XS switch CPU card block diagram is shown as below:

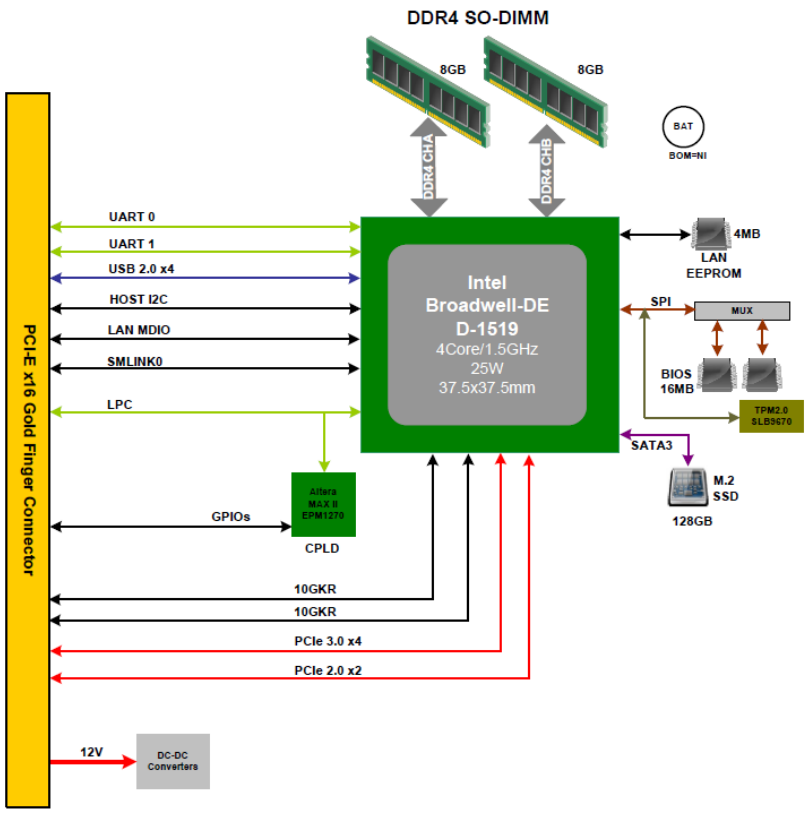


Figure 2-10 CPU Board Functional Block Diagram

2.5.2 CPU Card PCB Placement

S9500-30XS switch CPU card placement is shown as below:

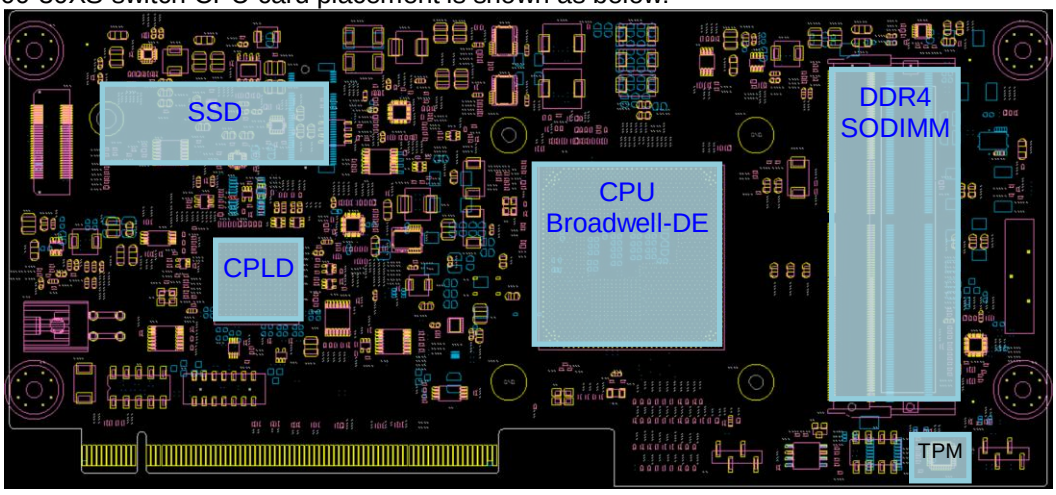


Figure 2-11 CPU Board PCB Layout

CPU Card Key Components

Description	Manufacturer	Manufacturer Part Number
Quad Core CPU	Intel	Broadwell-DE D1519

8GB SODIMM	ATP	X4F08QD8BNRCSW-B-FN1
128GB SSD	ATP	AF128GSAIA-FN1
Max II CPLD	Atera/Intel	EPM1270F256I5N
TPM 2.0	Infineon	SLB 9670XQ2.0 FW7.63

2.5.3 CPU Card PCB Dimensions

CPU Card Dimensions

CPU Card	Inches	Millimeters
Width	3.78	96
Length	8.27	210

2.5.4 CPU Card PCB Stack-up

Below shows CPU card 12 layers PCB stackup:

PCB Material : TU-862HF

Designed Impedance Table						Single End (Genereal)		Single End (Genereal)		Diff 80ohm		Diff 85ohm		Diff 100ohm	
						Signal End 40ohm	outer: +/- 10%	Signal End 50ohm	outer: +/- 10%	Diff. 80ohm	outer: +/- 10%	Diff. 85ohm	outer: +/- 10%	Diff. 100ohm	outer: +/- 10%
							inner: +/- 10%		inner: +/- 10%		inner: +/- 10%		inner: +/- 10%		inner: +/- 10%
Layer No.	Layer Name	Material	Layer Thickness (mil)	DK 1Ghz	Df 1Ghz	W		W		W // Sd // W		W // Sd // W		W // Sd // W	
		Solder Mask	0.4												
1	Top	0.5oz+Plating	1.8			6.5		4.3		5.8 // 6.7 // 5.8		5.3 // 7.7 // 5.3		3.9 // 8.6 // 3.9	
prepreg		1080*1	2.6	3.45	0.0156										
2	GND2	1oz	1.2												
Core		2116*1	5	3.8	0.0143										
3	SIG3	1oz	1.2			6		3.8		6 // 9 // 6		5.3 // 8.5 // 5.3		4 // 11.5 // 4	
prepreg		1080*1+106*1	4.1	3.7	0.0156/0.0174										
4	GND4	1oz	1.2												
Core		2116*1	5	3.8	0.0143										
5	SIG5	1oz	1.2			6		3.8		6 // 9 // 6		5.3 // 8.5 // 5.3		4 // 11.5 // 4	
prepreg		1080*1+106*1	4.1	3.7	0.0156/0.0174										
6	PWR6	2oz	2.4												
Core		2113*1	4	3.9	0.0148										
7	PWR7	2oz	2.4												
prepreg		1080*1+106*1	4.1	3.7	0.0156/0.0174										
8	SIG8	1oz	1.2			6		3.8		6 // 9 // 6		5.3 // 8.5 // 5.3		4 // 11.5 // 4	
Core		2116*1	5	3.8	0.0143										
9	GND9	1oz	1.2												
prepreg		1080*1+106*1	4.1	3.7	0.0156/0.0174										
10	SIG10	1oz	1.2			6		3.8		6 // 9 // 6		5.3 // 8.5 // 5.3		4 // 11.5 // 4	
Core		2116*1	5	3.8	0.0143										
11	GND11	1oz	1.2												
prepreg		1080*1	2.6	3.45	0.0156										
12	BOTTOM	0.5oz+Plating	1.8			6.5		4.3		5.8 // 6.7 // 5.8		5.3 // 7.7 // 5.3		3.9 // 8.6 // 3.9	
		Solder Mask	0.4												
Overall Board Thickness w/SM			64.4mils (+/-10%)												

Figure 2-12 CPU Card PCB Stack-up

2.5.5 PCIe x16 Card Edge Pinout

CPU card is installed on switch board through PCIe x16 connector, pinout is shown as below. Items marked in RED are new added / changed by comparing with Alpha design.

Description	I/O Type	Broadwell-DE Pinout--B side	Apache CPU Card PCIE X16 Connector					Broadwell-DE Pinout--A side	I/O Type	Description
12V power input	PWR	P12V	B1	P12V		PRSNT#1	A1	CPU_PRSNT_L	Out	CPU card presence signal, tie to pin B81 on CPU card.
12V power input	PWR	P12V	B2	P12V		P12V	A2	P12V	PWR	12V power input
12V power input	PWR	P12V	B3	P12V		P12V	A3	P12V	PWR	12V power input
	GND	GND	B4	GND		GND	A4	GND		
SMBus clock signal from CPU PCH	Out,	I2C0_PCH_SCL	B5	SMBCLK		JTAG_TCK	A5	JTAG_TCK	Out	Test Clock
SMBus data signal to/from CPU PCH	In/Out	I2C0_PCH_SDA	B6	SMBDAT		JTAG_TDI	A6	JTAG_TDI	In	Test Data Intput
	GND	GND	B7	GND		JTAG_TDO	A7	JTAG_TDO	Out	Test Data Output
USB 2.0 to/from CPU PCH port2	In/Out,	USB2_PCH_P2_DP	B8	P3.3V		JTAG_TMS	A8	JTAG_TMS	Out	Test Mode Select
USB 2.0 to/from CPU PCH port2	In/Out,	USB2_PCH_P2_DN	B9	JTAG_TRST#		P3.3V	A9	MIIM_IIO_LAN_MDC	Out	MIIM clock signal sourced from CPU LAN controller
SMBus alert signal to CPU PCH	In,	CPU_I2C0_ALERT_N	B10	P3.3Vaux		P3.3V	A10	MIIM_IIO_LAN_MDIO	In/Out,	MIIM data signal from/to CPU LAN controller
I2C reset signal from CPU CPLD	Out,	HOST_TO_MB_I2C_RST	B11	WAKE_N		PWRGD	A11	PWRGD_CPU_PCH	Out,	CPU power good signal buffer from 'PROCPWRGD_PCH'.
					KEY					
CPU PCIe reset to main board		HOST_TO_MB_PCIEX_RST_L	B12	RSVD		GND	A12	GND		
		GND	B13	GND	x1	PCIE0_REFCLK_P	A13	CLK_100M_PCIE0_SLOT_P	Out,	PCIe 100MHz diff. clock output from CPU PCIe_block
RTC reset by BMC	In	BMC_RTCRST_L	B14	PCIE0_TX0_P		PCIE0_REFCLK_N	A14	CLK_100M_PCIE0_SLOT_N	Out,	PCIe 100MHz diff. clock output from CPU PCIe_block
BMC reset signal from CPU CPLD	Out,	HOST_TO_MB_BMC_RST_L	B15	PCIE0_TX0_N		GND	A15	GND		
		GND	B16	GND		PCIE0_RX0_P	A16	INT0_PCH_GPIO6_N	In	GPIO signal to/from CPU GPIO6
CPU interrupt signal from CPU CPLD	Out,	HOST_TO_BMC_INT_L	B17	PRSNT2_N		PCIE0_RX0_N	A17	INT1_PCH_GPIO7_N	In	GPIO signal to/from CPU GPIO7
		GND	B18	GND		GND	A18	GND		
BMC non maskable interrupt to CPU CPLD	In,	BMC_TO_HOST_NMI_L	B19	PCIE0_TX1_P		RSVD	A19	PECI_PCH_BMC	In/Out,	PECI signal between CPU and BMC
BMC interrupt signal to CPU CPLD	In,	BMC_TO_HOST_INT_L	B20	PCIE0_TX1_N	x4	GND	A20	GND		
		GND	B21	GND		PCIE0_RX1_P	A21	INT2_PCH_GPIO1_N	In	GPIO signal to/from CPU GPIO1
		GND	B22	GND		PCIE0 RX1 N	A22	VP1P05		1.05V power for PECI
10G KR signal from CPU LAN controller TX lane1	Out,	SFPP1_KR_TX1_P	B23	PCIE0_TX2_P		GND	A23	GND		
10G KR signal from CPU LAN controller TX lane1	Out,	SFPP1_KR_TX1_N	B24	PCIE0_TX2_N		GND	A24	GND		
		GND	B25	GND		PCIE0_RX2_P	A25	SFPP1_KR_RX1_P	In, 0.1uF AC cap	10G KR signal to CPU LAN controller RX lane1
		GND	B26	GND		PCIE0_RX2_N	A26	SFPP1_KR_RX1_N	In, 0.1uF AC cap	10G KR signal to CPU LAN controller RX lane1
10G KR signal from CPU LAN controller TX lane0	Out,	SFPP0_KR_TX0_P	B27	PCIE0_TX3_P		GND	A27	GND		
10G KR signal from CPU LAN controller TX lane0	Out,	SFPP0_KR_TX0_N	B28	PCIE0_TX3_N		GND	A28	GND		
		GND	B29	GND		PCIE0 RX3 P	A29	SFPP0_KR_RX0_P	In, 0.1uF AC cap	10G KR signal to CPU LAN controller RX lane0
CPU platform reset signal buffer from CPU CPLD	Out,	CPU_PLTRST_N	B30	RSVD		PCIE0_RX3_N	A30	SFPP0_KR_RX0_N	In, 0.1uF AC cap	10G KR signal to CPU LAN controller RX lane0
System reset signal to CPU card	In,	SYS_RESET_L	B31	PRSNT2_N		GND	A31	GND		
		GND	B32	GND		RSVD	A32	USB2_PCH_P1_DP	In/Out,	USB 2.0 to/from CPU PCH port1
PCIe Gen3 signal from CPU IIO x16 block TX lane3	Out, 0.1uF AC cap	HOST_TO_MB_PCIE_TX3_P	B33	PCIE0_TX4_P		RSVD	A33	USB2_PCH_P1_DN	In/Out,	USB 2.0 to/from CPU PCH port1
PCIe Gen3 signal from CPU IIO x16 block TX lane3	Out, 0.1uF AC cap	HOST_TO_MB_PCIE_TX3_N	B34	PCIE0_TX4_N	x8	GND	A34	GND		
		GND	B35	GND		PCIE0_RX4_P	A35	MB_TO_HOST_PCIE_RX3_P	In,	PCIe Gen3 signal to CPU IIO x16 block RX lane3
		GND	B36	GND		PCIE0_RX4_N	A36	MB_TO_HOST_PCIE_RX3_N	In,	PCIe Gen3 signal to CPU IIO x16 block RX lane3
PCIe Gen3 signal from CPU IIO x16 block TX lane2	Out, 0.1uF AC cap	HOST_TO_MB_PCIE_TX2_P	B37	PCIE0_TX5_P		GND	A37	GND		
PCIe Gen3 signal from CPU IIO x16 block TX lane2	Out, 0.1uF AC cap	HOST_TO_MB_PCIE_TX2_N	B38	PCIE0_TX5_N		GND	A38	GND		
		GND	B39	GND		PCIE0_RX5_P	A39	MB_TO_HOST_PCIE_RX2_P	In,	PCIe Gen3 signal to CPU IIO x16 block RX lane2
		GND	B40	GND		PCIE0_RX5_N	A40	MB_TO_HOST_PCIE_RX2_N	In,	PCIe Gen3 signal to CPU IIO x16 block RX lane2
PCIe Gen3 signal from CPU IIO x16 block TX lane1	Out, 0.1uF AC cap	HOST_TO_MB_PCIE_TX1_P	B41	PCIE0_TX6_P		GND	A41	GND		
PCIe Gen3 signal from CPU IIO x16 block TX lane1	Out, 0.1uF AC cap	HOST_TO_MB_PCIE_TX1_N	B42	PCIE0_TX6_N		GND	A42	GND		
		GND	B43	GND		PCIE0_RX6_P	A43	MB_TO_HOST_PCIE_RX1_P	In,	PCIe Gen3 signal to CPU IIO x16 block RX lane1
		GND	B44	GND		PCIE0_RX6_N	A44	MB_TO_HOST_PCIE_RX1_N	In,	PCIe Gen3 signal to CPU IIO x16 block RX lane1
PCIe Gen3 signal from CPU IIO x16 block TX lane0	Out, 0.1uF AC cap	HOST_TO_MB_PCIE_TX0_P	B45	PCIE0_TX7_P		GND	A45	GND		
PCIe Gen3 signal from CPU IIO x16 block TX lane0	Out, 0.1uF AC cap	HOST_TO_MB_PCIE_TX0_N	B46	PCIE0_TX7_N		GND	A46	GND		
		GND	B47	GND		PCIE0_RX7_P	A47	MB_TO_HOST_PCIE_RX0_P	In,	PCIe Gen3 signal to CPU IIO x16 block RX lane0
System reset signal to CPU PCH 'PWRBTN'	In,	FP_PWR_BTN_N	B48	PRSNT2_N		PCIE0_RX7_N	A48	MB_TO_HOST_PCIE_RX0_N	In,	PCIe Gen3 signal to CPU IIO x16 block RX lane0
		GND	B49	GND		GND	A49	GND		
Thermal Trip signal from CPU	Out,	CPU_THERMTRIP_L	B50	PCIE0_TX8_P		RSVD	A50	CPU_CATERR_L	out	MISC. signal from CPU
PROCHOT signal from CPU	Out,	CPU_PROCHOT_L	B51	PCIE0_TX8_N	x16	GND	A51	GND		
		GND	B52	GND		PCIE0_RX8_P	A52	INT4_PCH_GPIO15_N	In,	GPIO signal to/from CPU GPIO15
		GND	B53	GND		PCIE0_RX8_N	A53	INT3_PCH_GPIO12_N	In,	GPIO signal to/from CPU GPIO12
UART TXD signal bufferred from CPU PCH port 1	Out,	CPU_UART1_TXD	B54	PCIE0 TX9 P		GND	A54	GND		
UART RXD signal to CPU PCH port 1 through buffer	In,	CPU_UART1_RXD	B55	PCIE0_TX9_N		GND	A55	GND		
		GND	B56	GND		PCIE0_RX9_P	A56	UART0_PCH_RXD	In,	UART RXD signal to CPU PCH port 0 through buffer
		GND	B57	GND		PCIE0_RX9_N	A57	UART0_PCH_TXD	Out,	UART TXD signal bufferred from CPU PCH port 0
PCIe Gen2 signal from CPU PCH x8 block TX lane1		G2_PCIE_TX0_P	B58	PCIE0_TX10_P		GND	A58	GND		
PCIe Gen2 signal from CPU PCH x8 block TX lane1		G2_PCIE_TX0_N	B59	PCIE0_TX10_N		GND	A59	GND		
		GND	B60	GND		PCIE0_RX10_P	A60	G2_PCIE_RX0_P	In,	PCIe Gen2 signal to CPU PCH x8 block RX lane1
		GND	B61	GND		PCIE0_RX10_N	A61	G2_PCIE_RX0_N	In,	PCIe Gen2 signal to CPU PCH x8 block RX lane1
PCIe Gen2 signal from CPU PCH x8 block TX lane0		G2_PCIE_TX1_P	B62	PCIE0_TX11_P		GND	A62	GND		
PCIe Gen2 signal from CPU PCH x8 block TX lane0		G2_PCIE_TX1_N	B63	PCIE0_TX11_N		GND	A63	GND		
		GND	B64	GND		PCIE0_RX11_P	A64	G2_PCIE_RX1_P	In,	PCIe Gen2 signal to CPU PCH x8 block RX lane0
		GND	B65	GND		PCIE0_RX11_N	A65	G2_PCIE_RX1_N	In,	PCIe Gen2 signal to CPU PCH x8 block RX lane0
LPC clock signal from CPU clock gen through buffer	Out,	CLK_33M_LPC	B66	PCIE0_TX12_P		GND	A66	GND		
LPC serial interrupt signal to CPU		LPC_SERIRQ	B67	PCIE0_TX12_N		GND	A67	GND		
		GND	B68	GND		PCIE0_RX12_P	A68	LPC_FRAME_PCH_N	In,	LPC frame signal from CPU PCH
		GND	B69	GND		PCIE0_RX12_N	A69	P3V3_VBAT		CPU RTC battery sourced from main board
LPC data/address signal 3 to/from CPU PCH	In/Out,	LPC_LAD3_PCH	B70	PCHE0_TX13_P		GND	A70	GND		
LPC data/address signal 2 to/from CPU PCH	In/Out,	LPC_LAD2_PCH	B71	PCHE0_TX13_N		GND	A71	GND		
		GND	B72	GND		PCHE0_RX13_P	A72	LPC_LAD1_PCH	In/Out,	LPC data/address signal 1 to/from CPU PCH
		GND	B73	GND		PCHE0_RX13_N	A73	LPC_LAD0_PCH	In/Out,	LPC data/address signal 0 to/from CPU PCH
USB 2.0 to/from CPU PCH port0	In/Out,	USB2_PCH_P0_DP	B74	PCIE0_TX14_P		GND	A74	GND		
USB 2.0 to/from CPU PCH port0	In/Out,	USB2_PCH_P0_DN	B75	PCIE0_TX14_N		GND	A75	GND		
		GND	B76	GND		PCIE0_RX14_P	A76	SMB_SMLINK0_CLK	Out,	SMBus link clock signal from CPU PCH
		GND	B77	GND		PCIE0_RX14_N	A77	SMB_SMLINK0_DAT	In/Out,	SMBus link data signal to/from CPU PCH
GPIO signal from CPU GPIO54	Out,	CPU_BOOT_DONE	B78	PCIE0_TX15_P		GND	A78	GND		
MGPIO from CPU to BMC	Out,	ME_RCVR_L	B79	PCIE0_TX15_N		GND	A79	GND		
		GND	B80	GND		PCIE0_RX15_P	A80	USB2_PCH_P3_DN	In/Out,	USB2.0 port 3 from CPU PCH to BMC
CPU card present signal, tie to pin A1 on CPU card.	In,	CPU_PRSNT_L	B81	PRSNT2_N		PCIE0_RX15_N	A81	USB2_PCH_P3_DP	In/Out,	USB2.0 port 3 from CPU PCH to BMC
Thermal sensor monitor by main board HWM	In	CPU_TEMP_SENSOR	B82	RSVD2		GND	A82	GND		

Figure 2-13 CPU Card PCIe x16 Gold Finger Pinout

2.6 BMC Subsystem

BMC subsystem is designed on switch board.

2.6.1 BMC Subsystem Block Diagram

In S9500-30XS switch, baseboard management controller (BMC) autonomous monitors system's health including temperature, voltage, fan speed, etc.

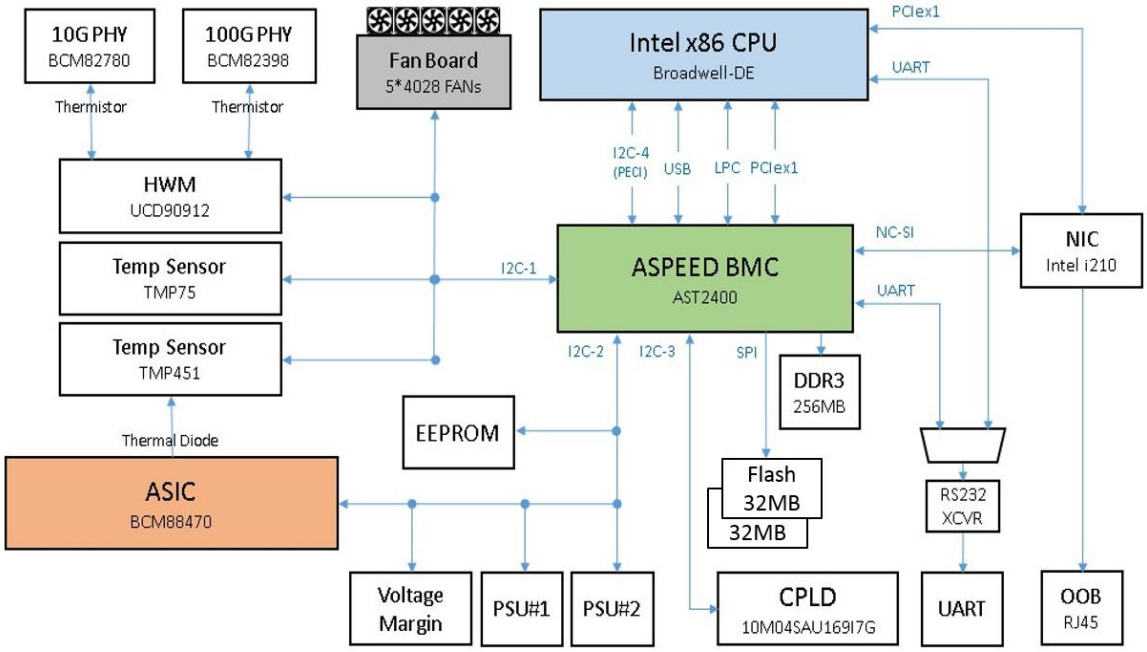


Figure 2-14 BMC Block Diagram

2.6.2 BMC Chipset Heater Control

There is no industrial rating version for AST2400. To make this commercial chipset works under -40~0°C ambient temperature, an additional chipset heater is adopted for AST2400.

BMC heater is controlled by HWM UCD90124A. It monitors chassis and BMC, chipset heater temperature and controls, after receive BMC heater heating enable signal from CPLD, BMC heater DC/DC power enable & power output circuits, BMC heater DC/DC convertor is turned on if chassis and BMC temperature is lower than -0°C, heater power will be turned off if chassis temperature is higher than 0°C.

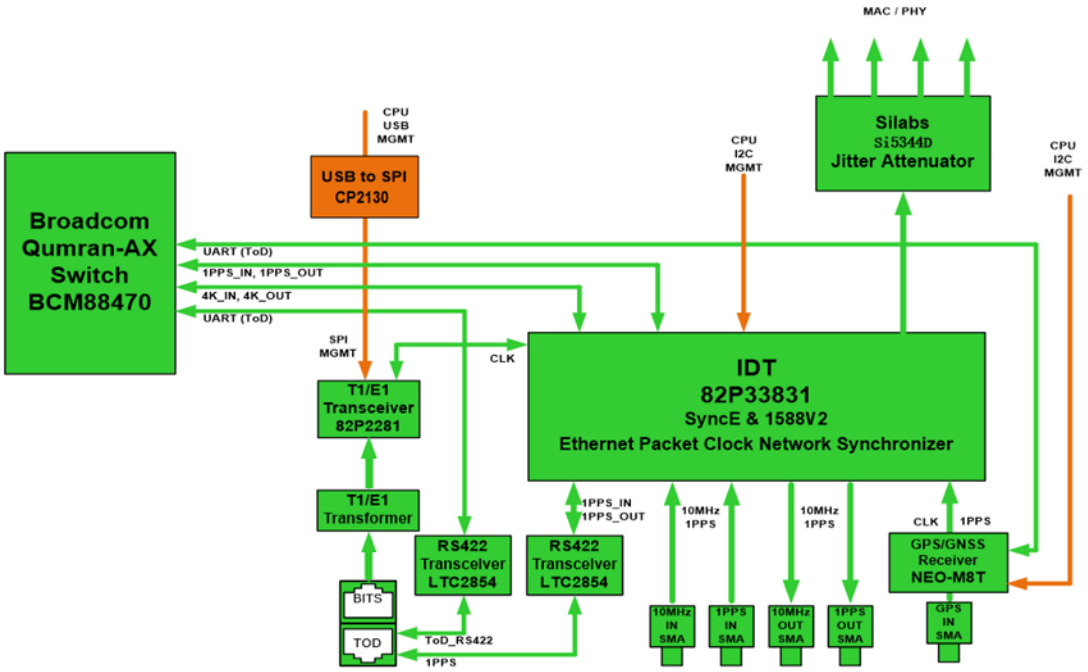
After BMC sensor reaches pre-defined temperature, UCD90124A will enable BMC DC/DC power rails and BMC start boot up, heater is being turned on continue to make BMC temperature keep in plus °C environment.

The estimated warm-up time for BMC will be 0~300 seconds in 0'C~-40'C environment, around 240s in -40°C chamber environment, the heating up time may be vary based on cabinet temperature & air flow condition.

2.7 Timing Subsystem

Timing subsystem is designed on switch board.

2.7.1 Timing Subsystem Block Diagram



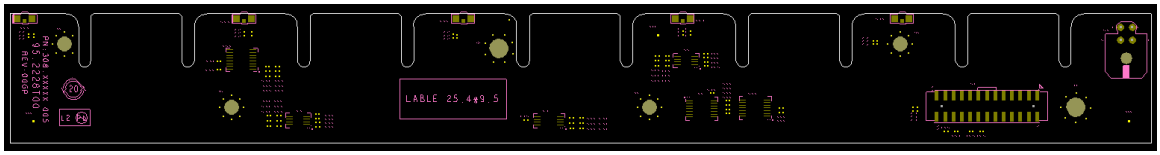
2.7.2 Timing Subsystem Features

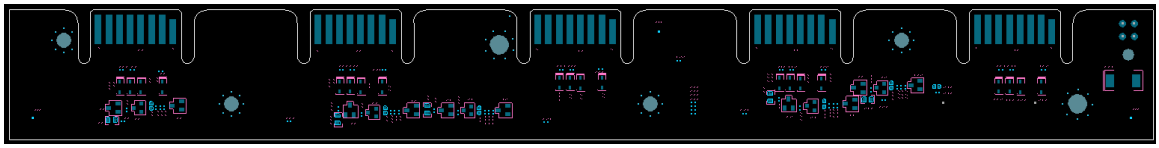
- IEEE-1588v2(PTP) & SyncE
- Timing Input / Output sources.
  - GNSS input port (SMA)
  - 1PPS input port (SMA)
  - 1PPS output port (SMA)
  - 10MHz input port (SMA)
  - 10MHz output port (SMA)
  - Time of day (TOD) input port (RJ45)
  - Building-Integrated Timing System (BITS) input port (RJ45)

2.8 FAN, LED & PSU Cards

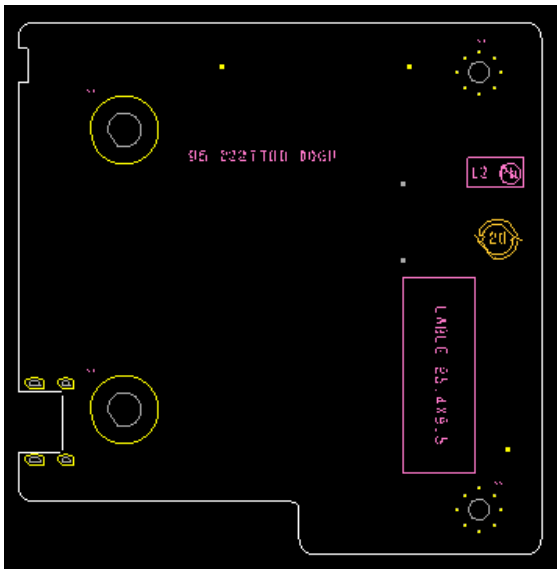
2.8.1 FAN, LED & PSU Cards Placement

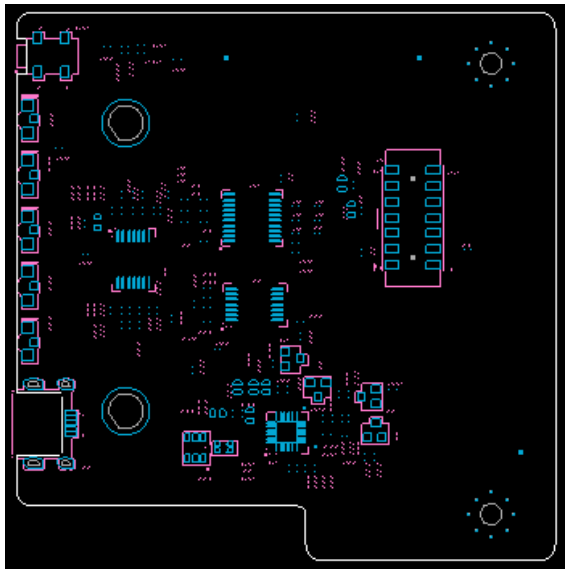
FAN Card



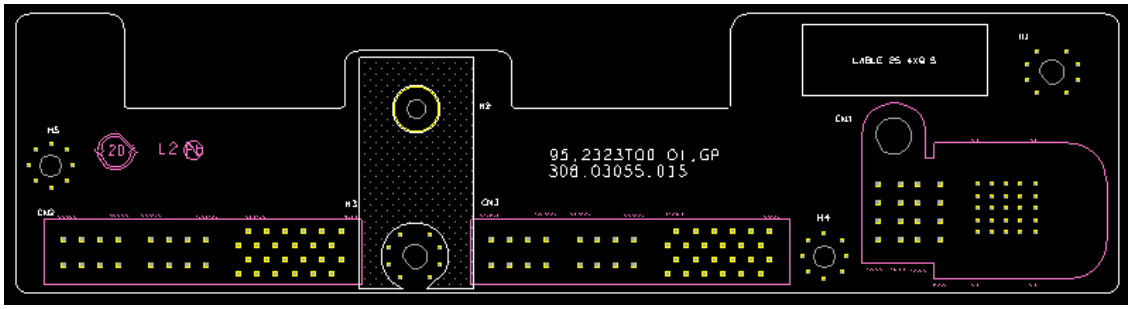


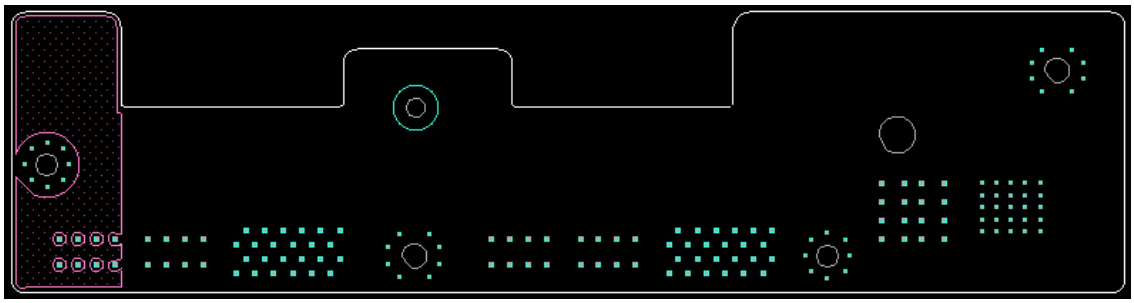
LED Card





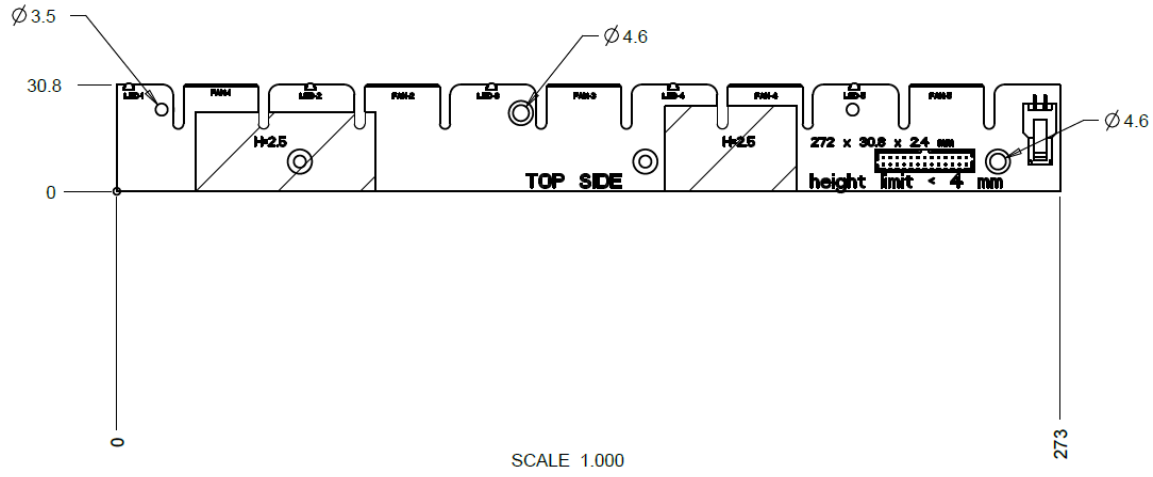
PSU Card



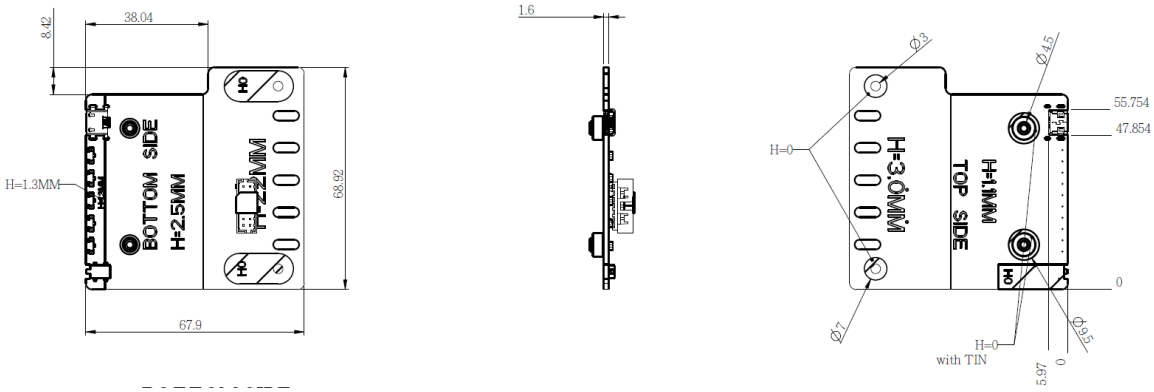


2.8.1 FAN, LED & PSU Cards Dimensions

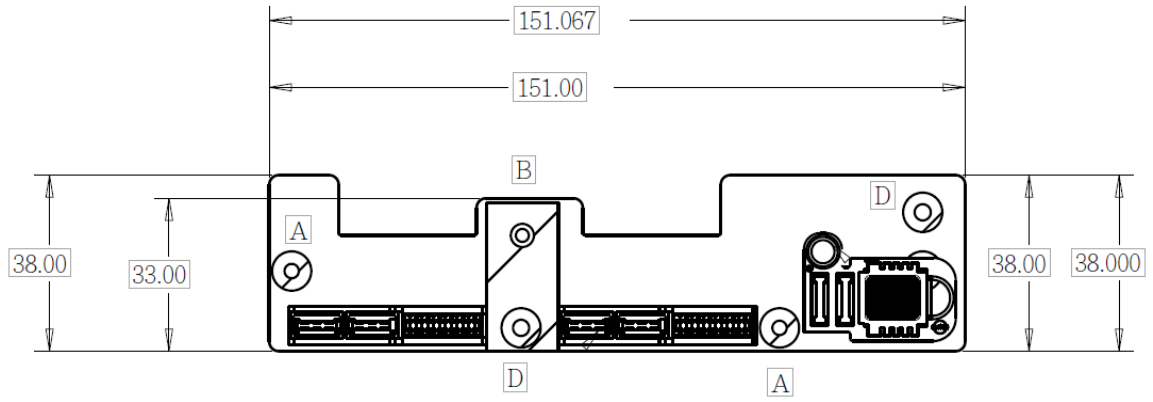
Fan Card



LED Card



PSU Card



2.8.2 FAN, LED & PSU Cards Stackup

FAN Card

Structure (Stack up)					Dk	Df	Single-End (GND/PWR reference)		
Layer	Type	Cu	Material	Thk (mil)	1GHz	1GHz	Width (mil)	Ohms	Ref
	solder mask		solder mask	0.6					
TOP1		single	0.5oz+Plating	1.8			9.0	50±10%	L2
	prepreg		2116	5.4	4	0.018			
GND2		Reference	1oz	1.2					
	core		CORE 0.8mm 1/1OZ	31.5	4.2	0.018			
SIGNAL3		single	1oz	1.2			33.0	50±10%	L2 & L5
	prepreg		2116*2	10.4	4	0.018			
SIGNAL4		single	1oz	1.2			33.0	50±10%	L2 & L5
	core		CORE 0.8mm 1/1OZ	31.5	4.2	0.018			
GND5		Reference	1oz	1.2					
	prepreg		2116	5.4	4	0.018			
BOTTOM6		single	0.5oz+Plating	1.8			9.0	50±10%	L5
	solder mask		solder mask	0.6					
ard thickness: 2.4mm+/-10%			Total:	93.8	mil				

LED card

PSU Card

Structure (Stack up)					Dk	Single-End (GND/PWR reference)		
Layer	Type	Cu	Material	Thk (mil)	1GHz	Width (mil)	Ohms	Ref
	solder mask		solder mask	0.8				
TOP1		single	1oz+Plating	2.4		10	50±10%	L2
	prepreg		1080*2	5.8	3.8			
GND2		Reference	2oz	2.4				
	core		CORE 0.4mm 2/2OZ	16	4.3			
PWR		single	2oz	2.4				
	prepreg		7628*3	20	4.1			
PWR		single	2oz	2.4				
	core		CORE 0.4mm 2/2OZ	16	4.3			
GND5		Reference	2oz	2.4				
	prepreg		1080*2	5.8	3.8			
BOTTOM6		single	1oz+Plating	2.4		10	50±10%	L5
	solder mask		solder mask	0.8				
ard thickness: 2.0mm+/-10%			Total:	79.6	mil			

3 Field Replaceable Components

3.1 Power Supply

S9500-30XS switch adopts 400W hot swappable power supply unit made by 3Y. The PSU module is supported: Neg48 DC/DC.

3.1.1 Physical Size

The physical size of the power supply enclosure is intended to accommodate the power range of up to 400W. The physical size is 40.2mm x 50.5mm x 211mm (height x width x length). The Gold finger height adjustment to 5mm.

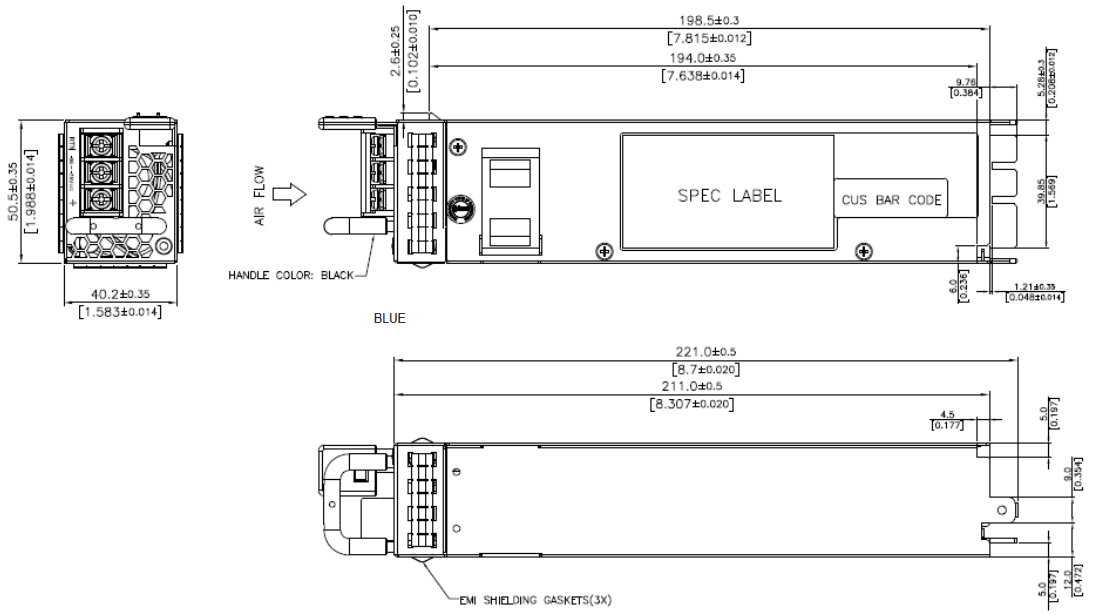


Figure 3-1 Power Supply Dimension

3.1.2 Electrical Specifications

The detailed electrical specifications of Neg48DC/DC PSU are shown as below :

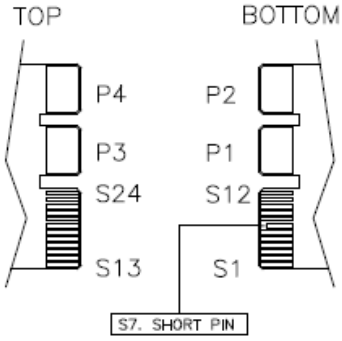
INPUT SPECIFICATIONS	
Input Voltage Range	-36 ~ -75VDC
Inrush Current	75A max.
OUTPUT SPECIFICATIONS	
Output Voltage (Volts)	+12V
Output Current (Amps)	33.3A(+12V)
Max Power (Watt)	–40°C to 55°C 450W, –40°C to 65°C 400W
Output Voltage (Volts)	+5VSB
Output Current (Amps)	3A (+5VSB)
Efficiency	>88% @20% load, >91 @50% load, >89% @100% load
Ripple P-P (mV) (max.)	+12V:120, +5VSB:50
Total Regulation	±5%
GENERAL SPECIFICATIONS	
Hold-up Time (min.)	3mS@-48VDC

Over Voltage Protection	Latch off
Over Current & Short Circuit Protection	Auto Recovery
Over Temperature Protection	Auto Recovery
FAN Failure Protection	
Hot Swap	
Load Sharing	
Hi-pot	2545VDC
ENVIRONMENTAL SPECIFICATIONS	
Operating Temperature Range	–40°C to 65°C
Storage Temperature Range	–40°C to +70°C
Humidity, Non-Condensing	0 to 95% RH
EMI	Meets FCC/CISPR 22 Class A(under 6dB) Specification

Table 3-1 3Y Power Supply Specification

3.1.3 Power Connector Pinout

The power connector is recommended backplane power connector OUPIIN 9392-4S24P04N12CB30DA or equivalent. PSU pin assignment is shown as below:



PIN NO.	CONDITION
P1	GND
P2	+12V
P3	GND
P4	+12V

PIN NO.	CONDITION
S1	+12VS
S2	+12VRS
S3	+12VBUS
S4	SMB_Alert
S5	SDA
S6	SCL
S7	PS–KILL
S8	PS ON
S9	PW OK
S10	A1
S11	+5VSB
S12	+5VSB
S13	NC
S14	PRESENT
S15	A0
S16	NC
S17	NC
S18	EEPROM_WP
S19	NC
S20	NC
S21	NC
S22	NC
S23	+5VSB
S24	+5VSB

Figure 3-2 PSU Pin Assignment

3.1.1 PSU LED Indicators

Table 2 – LED Status Information

Power supply condition	Power supply LED
No DC power to all PSU	OFF
No DC power to this PSU only	1Hz Flashing Red
DC present/only standby output on	1Hz Flashing Green
Power supply DC output ON and OK	Green
Power supply failure	Red
Power supply warning	1Hz Flashing Red*/ Green *

Note : * Flashing frequency: 1Hz (1sec Red/ 1sec Green)

3.2 FAN Module

New developed FAN tray with 40x40x28mm FAN is adopted on S9500-30XS system to meet chassis depth requirement.

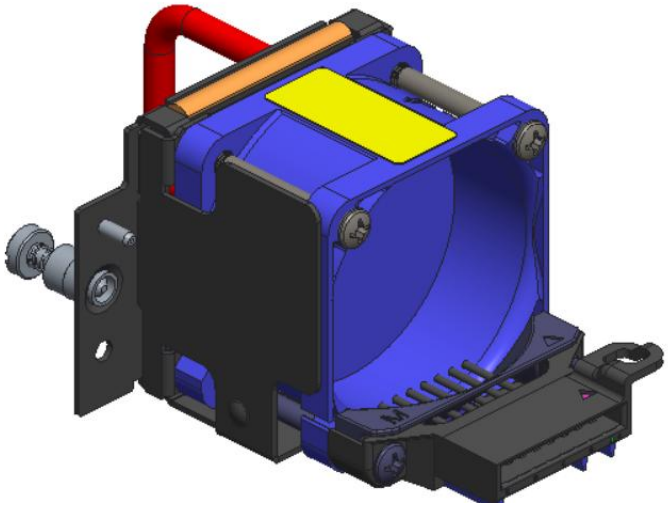


Figure 3-3 4028 FAN Module

3.2.1 Electrical Specifications

Rated voltage	12 VDC
Rated current	900mA, 1035mA, max.
Rated power consumption	10.8W, 12.42W, max.
Operating voltage range	10.2~13.2 VDC
Starting voltage	10.2 VDC (25 degC)
Operating temperature	-40~70 degC
Rated speed	25000 RPM+/-10% at rated voltage
Air flow	31.3CFM, 27.6 CFM min.
Static pressure	2.81 Inch-H2O, 1.96 Inch-H2O min.
Acoustic noise	62.0 dB(A), 69.5 dB(A) max.

3.2.2 FAN Module Pinout

Molex 46856-0003 connector is assembled in FAN tray and mated with FAN card gold finger. Following Table 5-1 shows S9500-30XS FAN tray interface pinout.

Pin #	Pin Definition	I/O	Function Description	FAN Tray Connector Connection	FAN Connection
1	+12V	-	FAN 12V power	To inlet, outlet FAN +	Out, +
2	GND	-	FAN GND	To outlet FAN -	Out, -
3	FAN_PRSNT_N	O	FAN module presence signal sent by FAN	Jump to Pin2	PIN 2
4	FAN_PWM_OUTLET	I	Outlet FAN speed PWM control signal from HWM	To outlet FAN PWM	Out, PWM
5	FAN_TACH_OUTLET	O	FAN speed tachometer sent by outlet FAN	From outlet FAN tachometer	Out, 3rd
6					
7					
8					

Table 3-2 Connector Pin Definition of FAN Tray

4 Software Support

The S9500-30XS supports a base software package composed of the following components:

BIOS

The S9500-30XS Supports AMI AptioV BIOS version xx or greater with the x86 CPU module

BMC

The S9500-30XS Supports AMI MegaRAC SP-X BMC firmware for Aspeed AST2400 platform.

ONIE

See http://onie.org/ for the latest supported version

5 Compliance

Environmental	
Operating temperature	-40 ~ 65°C (at sea level with Fan Failure condition)
Storage temperature	-40~70°C
Altitude	0 ~ 10,000ft at 65°C*
Operating relative humidity	0%-95% RH (non-condensing)
Storage relative humidity	0%~95% RH (non-condensing)
Vibration	IEC 68 - 2 - 36, IEC 68 - 2 - 6
Shock	IEC 68 - 2 - 29
Acoustic	
Dimensions (height x width x depth)	TBD
Weight	TBD

Compliance	
EMC	IEC60950-1 FCC/IC Report Class A EN 60950-1 FCC/IC Report Class A UL/CSA 60950-1 CNS 14336-1 GB4943.
Safety	IEC60950-1 FCC/IC Report Class A EN 60950-1 FCC/IC Report Class A UL/CSA 60950-1 CNS 14336-1 GB4943.1
NEBS	GR63 GR1089

RoHS	