EDGECORE Networks Corporation

Edgecore AS7326-56X

Switch Specification

Revision 1.0

OPEN

Compute Project

Revision History

Revision	Date	Author	Description
1.0	9/10/2018	Jeff Catlin	Initial Draft

Contents

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Component	Vendor	MFG P/N	Quantity	Remark
CPU Board-CPU	Intel	Broadwell-DE XeonD-1518	1	
MAC	Broadcom	BCM56873	1	
NIC	Broadcom	BCM5720	1	
EMP PHY	Broadcom	BCM54616S	1	
CPLD	Altera	5M1270ZF256C5N	1	For CPU system
CPLD	Altera	5M1270ZF256C5N	2	For Main board System and QSFP28 LED
CPLD	Altera	5M2210ZF324C5N	1	For SFP28 LED
CPLD	Altera	5M1270ZF256C5N	1	For Fan board System
I2C Switch	NXP	PCA9548APW	10	
Thermal Sensor	NS	LM75BD/SO8	3	
USB HUB IC	SMSC	USB2514B-AEZC	1	
Power Monitor	Lattice	POWR1014A	1	
UART IC	TI	MAX3232CPWR	1	Transceiver
PSU (AC/DC)	3Y	YM-2651Y,B01R	2	650W AC

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Scope

This document outlines the technical specifications for the Edgecore AS7326-56X Open Switch Platform submitted to the Open Compute Foundation to aid in porting software to the hardware platform.

Overview

This document describes the technical specifications of the AS7326-56X Switch designed by Edgecore Networks Corporation. The AS7326-56X is a cost optimized design focused on the Top of Rack installations offering 10G/25G equipment connectivity and providing 100G uplink connections.

The AS7326-56x supports forty eight SFP28 ports, eight QSFP28 ports, and two SFP+ ports for network connectivity.

The AS7326-56X is a PHY-Less design with the network interface connections directly attaching to the Serdes interfaces of the Broadcom 56873 switching silicon providing the lowest cost, latency, and power. The AS7326-56Xsupports traditional features found in switches such as:

- Redundant field replaceable power supply and fan units
- Support for “Front to Back” air flow direction
- Supports a modular CPU card that allows flexibility in the CPU and/or memory configurations that can be offered.
- Support for AC or DC power supply units

1. Introduction

The AS7326-56x is a 1U high and 536mm deep chassis base on Broadcom Trident3 chipset. The physical layer consists of 48x25G SFP28, 8x100G QSFP28 ports and 2x10G SFP+ ports. The switch has a nominal operating temperature range of 0 to +40 Degree C.
The CPU board is based upon the Intel BroadWell-DE which provide the following interfaces: x4 PCIe2.0, SGMII, MDC/MDIO, USB2.0, and 2channel I2C connect to the switch board. There are mSATA and eUSB devices in the CPU board and memory support DDR4 with ECC sodimm.

The following are key features of the product:

- Redundant and hot-swappable PS (1+1)
- Front facing for all connections
- Redundant and hot swappable fans (5+1)
- 1U rank mountable
- 48 SFP28 25G + 8 QSFP28 40G/100G + 2 10G SFP+ ports
- CPU module
  - CPU: Intel Broadwell-DE XeonD-1518
  - DDR SDRAM: 8GB x 2 2133MHz with ECC (DDR4 SO-DIMM)
  - SPI Flash (Boot): 16MB
  - USB to NAND Flash memory : 8GB SLC
  - mSATA: 32GB MLC (Reserve)
  - m.2 SATA: 64GB MLC
- USB port (5V/1A)
- Environmental operation:
  Front to Back Air Flow (0 to +45 degree C)
  Back to Front Air Flow (0 to +45 degree C)

1.1. Reference Documents

- Broadcom **BCM56870** Data Sheet
- IDT**89307** WANPLL Data Sheet
- 544040_Broadwell_DE_EDS_vol1_544040_rev1p0.pdf
- 544041_Broadwell_DE_EDS_Registers_Vol2_544041_v1_0.pdf
- 544042_Broadwell_DE_SoC_EDS_vol3_544042_v1_0.pdf
- 544043_Broadwell_DE_EDS_rev_0_75.pdf
- 544044_Broadwell_DE_EDS_Vol5_544044_rev0_71.pdf
- BCV-R-SB_SCH_20140804.pdf
- CamelBackMnt_FAB-B_NCOR2_09-09-14.pdf

1.2. Acronyms and Terminology

Some of the acronyms used in this document are listed below:

CCSR Configuration, Control, and Status Register
PCB Printed Circuit Board
PCBA Printed Circuit Board Assembly
PSU Power Supply Unit
BMC Baseboard management controller.
POR Power On Reset
RU Rack Mount Unit (equivalent to 1.75 inches)
SERDES Serializer / Deserializer

SKU Stock Keeping Unit
SMI Serial Management Interface
FRU Field Replaceable Unit
GPIO General Purpose Input Output
IP Internet Protocol
NP Network Processor
CPLD Complex Programmable Logic Device
RXAUI Reduced XAUI
RU Rack Mount Unit (equivalent to 1.75 inches)
SGMII Serial GMII
CAUI 10G/25G Attachment Unit Interface
CAUI-4 40G/100G Attachment Unit Interface
SFP28 25G/10G Small Form-Factor Pluggable
QSFP28 100G/40G Small Form-Factor Pluggable

2. Hardware Architecture

This section describes the architecture of PCBA, cooling, power consumption, electrical, reset, clocks, Ethernet port mapping etc.

2.1. Overview

The AS7326-56x provides 48x25G SFP28, 8x100G QSFP28 and 2x10G SFP+ ports on the board and can support 1 x 1G ports for management and control.

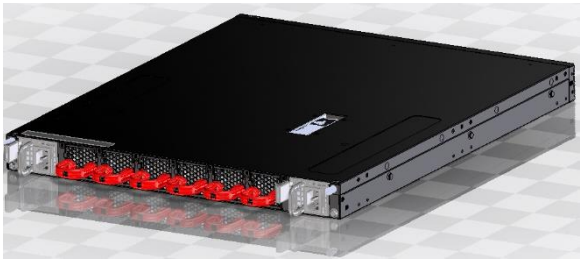

Table 1 System Overview

	ES7656BT3-0917-168ZZ
CPU sub-system	CPU: **Intel Broadwell-DE XeonD-1518 1.6G 4 Core** DDR SDRAM: **8GB x 2 2133MHz with ECC (DDR4 SO-DIMM)** SPI Flash (Boot): **16MB** USB to NAND Flash memory : **8GB SLC** mSATA SSD: **32GB MLC (Option)** m.2 SSD: **64GB MLC (2242 / 2280)**
Management	UART RS232 console port (RJ45 or Micro-USB), Out-band Management Ethernet port (RJ45)
USB	One type-A USB port at front panel, support USB 2.0 (480Mbps)
CPLD	CPLDs access by I2C and CPLDs code field upgraded by CPU GPIO

	ES7656BT3-0917-168ZZ
RJ45 LED X'FMR	One RJ45 with LED/one X'FMR embedded
MAC	Broadcom Trident3 BCM56873, 1 pcs, 2000Gbs multi-layer Ethernet switch controller
NIC	1 x BCM5720
EMP PHY	1 x BCM54616S
Ethernet Ports	48x25G SFP28, 8x100G QSFP28 and 2x10G SFP+ ports
PCB	12-Layers for CPU module 14-Layers for Mainboard 4-Layers for FAN board 4-Layers for Cable board
Power Supply	650W PSU back to front airflow, AC to DC ; front to back airflow, DC to AC, 1+1 redundant load-sharing, hot-swappable +12V/52.9A output / +5Vsb/4A output
Cooling	6 fan-tray modules with 6 pcs of 40mm x40mm x 56mm 12V fans, hot-swappable
System LED	Driving by CPLD
100G/40G/25G/10G LED	Driving by MAC LED stream
Push Button	One push button for reset at front panel
Dimension	536 mm (L: Depth) x 438.4mm (W: Width) x 43.5 mm (H: Height)
Mounting Options	Rack Mount

Table 2 Key component Table

Component	Vendor	MFG P/N	Quantity	Remark
CPU Board-CPU	Intel	Broadwell-DE XeonD-1518	1	
MAC	Broadcom	BCM56873	1	
NIC	Broadcom	BCM5720	1	
EMP PHY	Broadcom	BCM54616S	1	
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CPLD	Altera	5M1270ZF256C5N	1	For Fan board System
I2C Switch	NXP	PCA9548APW	10	
Thermal Sensor	NS	LM75BD/SO8	3	
USB HUB IC	SMSC	USB2514B-AEZC	1	

Component	Vendor	MFG P/N	Quantity	Remark
Power Monitor	Lattice	POWR1014A	1	
UART IC	TI	MAX3232CPWR	1	Transceiver
PSU (AC/DC)	3Y	YM-2651Y,B01R	2	650W AC

2.2. Block Diagram

The AS7326-56x provides 48 x 25G ports, 8 x 100G ports and 2 x 10G ports on the board and can support 1 x 1G port for management and control. It is formed by **BCM56873**, a 20 Falconcore with max. 2T switch capacity. The BCM56873 is connected to CPU module via PCIe Gen2.0 x 4 bus. The host system includes two banks of 8GB DDR4 SO-DIMM, 16MB boot Flash, Thermal detector, SYNC Ethernet and other glue logic. The Base unit uses 12VDC and 5VDC from the Hot swappable Power module. The on-board DC/DC is used to generate 3.3V/ 1.8V/1.2V/i 1.2V/ 0.8V/0.8V(ROV) from 12VDC.

Figure 1 Switch board Block Diagram

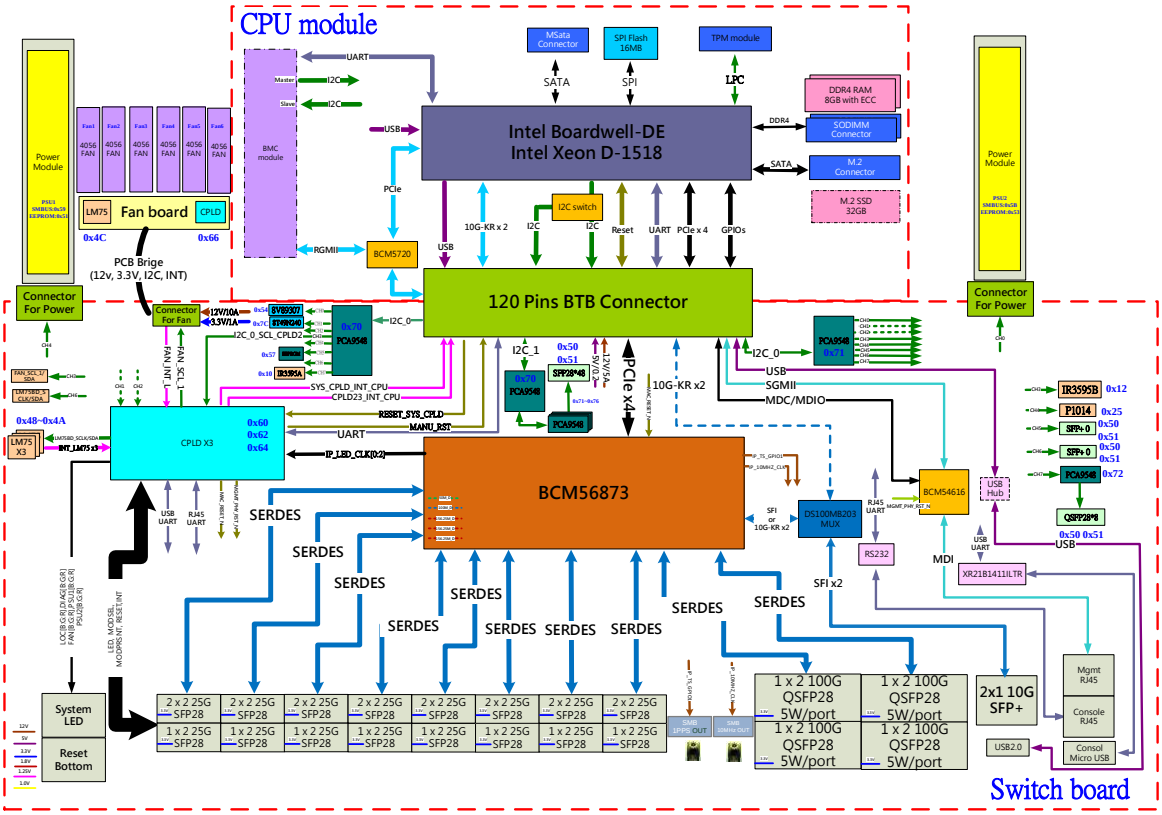
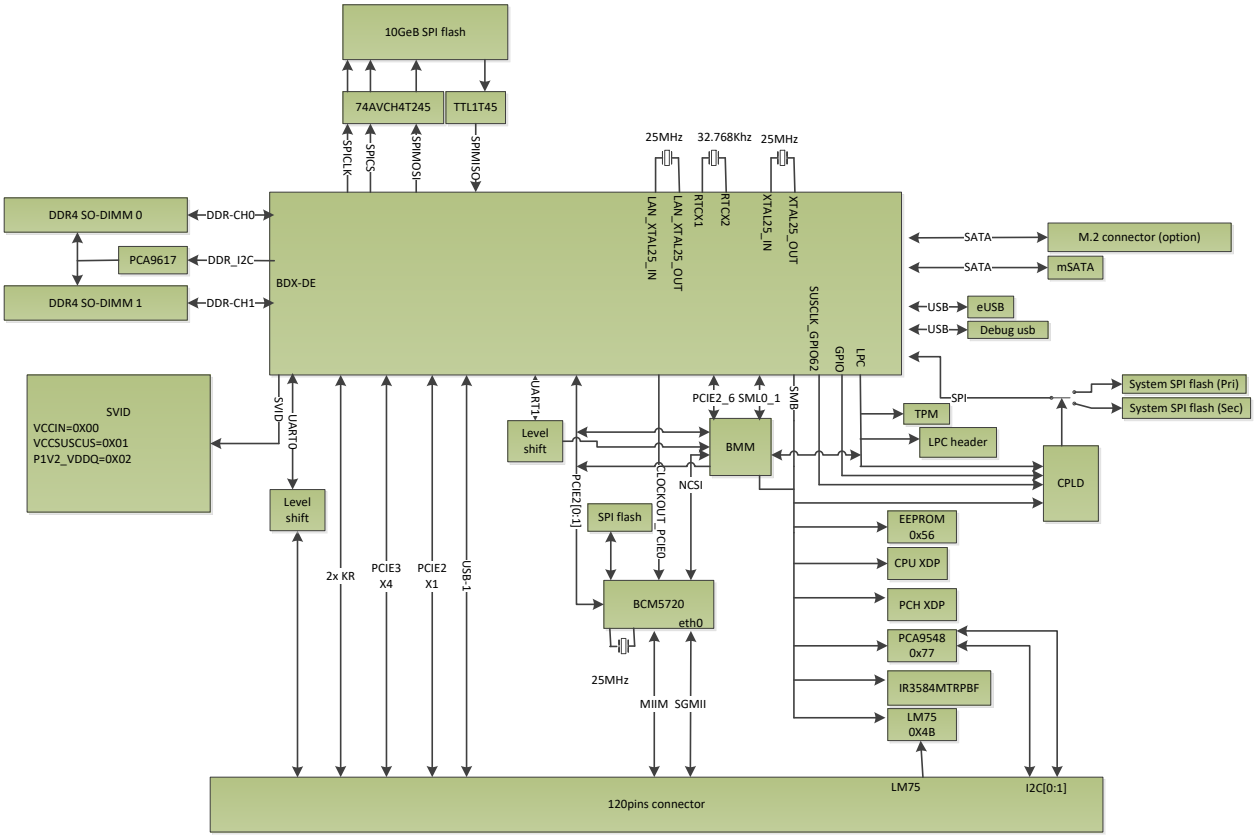


Figure 2 CPU board Block Diagram



2.2.1. Clock Tree

The unit support has a Synchronous logic which consists of Network Interface Synchronizer chip, Jitter attenuators and clock buffers. The key component is a Network Interface Synchronizer chip.

The Network Interface Synchronizer chip selects a reference clock from one of two valid clock sources generating a Stratum 3 compliant reference clock for the Broadcom Trident chip. This clock is also used as a transmit reference clock for all external interface ports. This logic consists of a IDT 89307 Network Interface Synchronizer chip and Oven controlled crystal oscillator. This synchronizer chip when properly configured will produce 25MHz and 156.25MHz clock which is frequency locked to a selected port recovered clock.

The IDT 89307 is configured through an I2C interface, it reports major state information via a number of status and control signals.

Figure 3 Switch board clock Tree

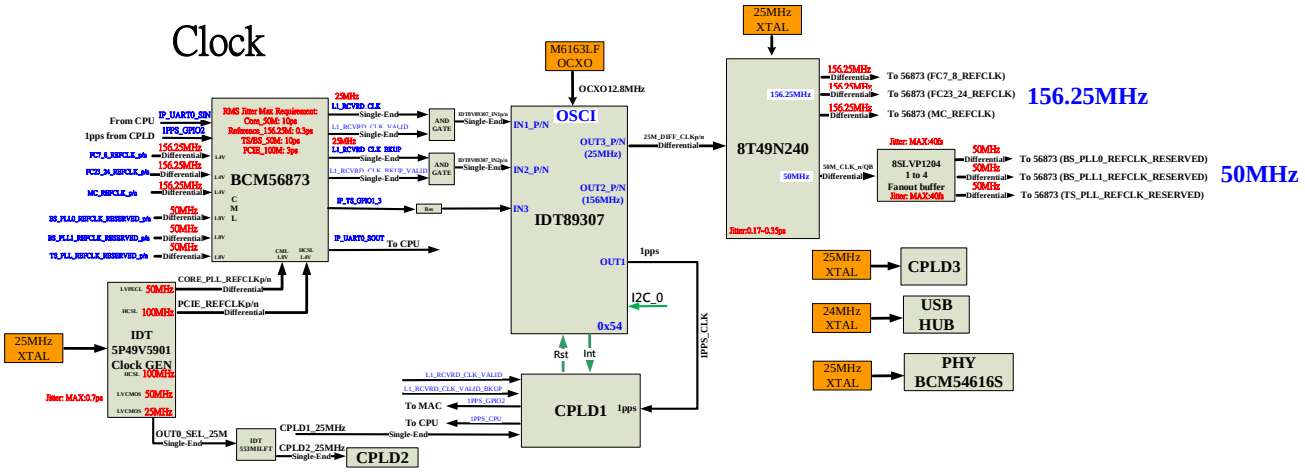
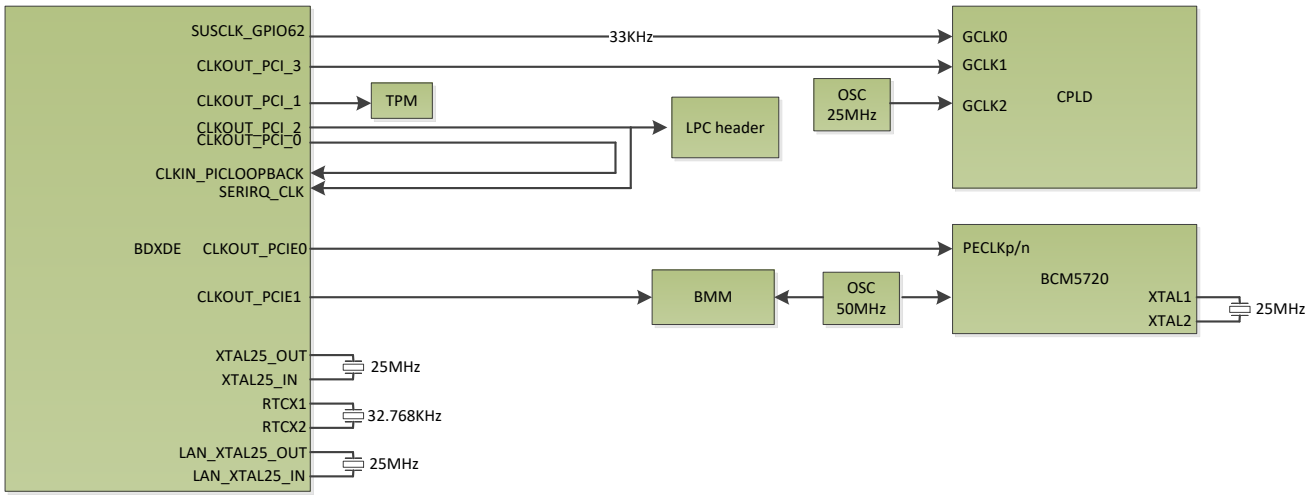


Figure 4 CPU board clock Tree



2.2.2. Power Tree

Based on the power estimation in Table 2, we have selected a suitable DC/DC with the best efficiency as possible.

In addition to convert the voltage from SPS, the regulation of each voltage is also very important. Each DC/DC is monitored to alarm the system through backplane connector if there is any DC/DC lower than monitored threshold. The power supply can support 12V output and standby 5V output, but our system only uses 12V output to be converted to other low system voltage.

The DC/DC is also shut down when the temperature is higher than the shutdown threshold of the thermal sensors.

The system power sequence is starting from high voltage to low voltage.

The following is about the power tree topology.

Figure 5 Switch board Power Tree

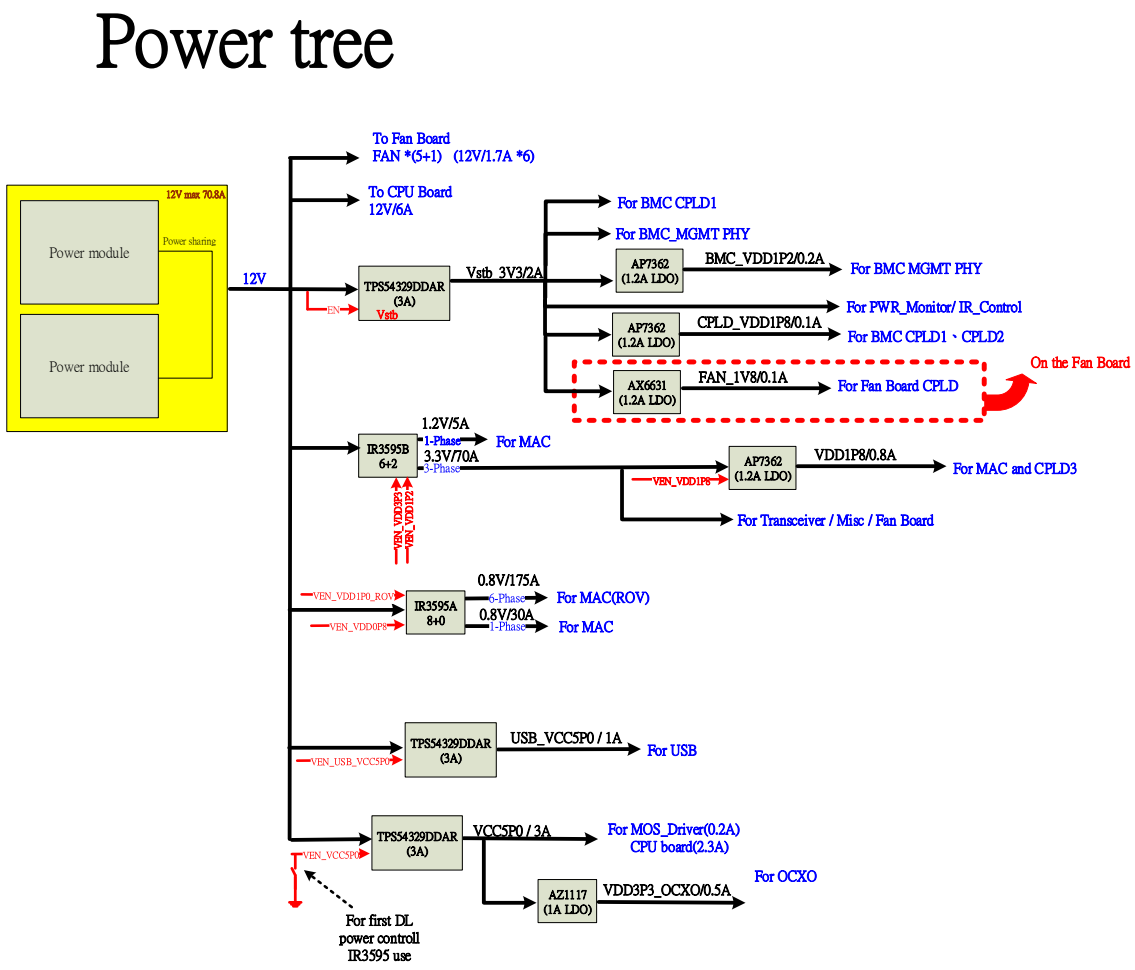
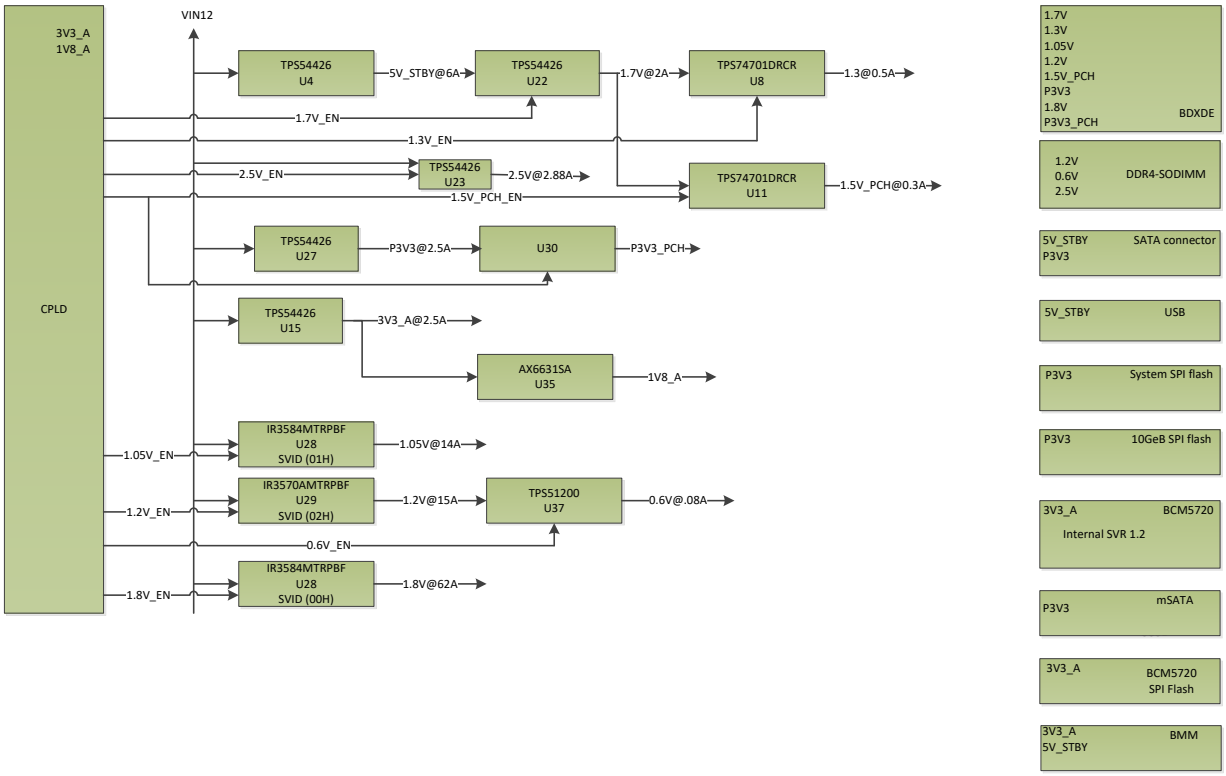


Figure 6 CPU board Power Tree



2.2.3. Reset Tree

The reset system will follow as below.

1. The CPU board and switch board will be power on. And the reset monitor IC will check DC power voltage if reach the threshold.
2. The monitor IC will send Power_RST signal to CPLD if all power is OK.
3. CPLD pass the MANU_RST signal to CPU board, and hold the all reset signals of switch board's device
4. CPU get the switch board's MANU_RST signal from switch board's CPLD, it means switch is ready to boot up. CPU board will check itself status and pull up Reset_SYS_CPLD signal to switch's CPLD to boot up switch board.
5. When switch's CPLD get the Reset_SYS_CPLD signal, switch's CPLD will pass to all device on switch to boot up device.
6. When the system running, the switch's CPLD has different register for every device's rest signal. CPU can reset switch's device separately via switch's CPLD register.

If CPU wants to reset itself without main board system, CPU can set "1" in "reset_lock" register of main board's CPLD1 (0x0B).Main board CPLD1 will block "reset_sys_cpld" signal to CPLD1, and main board CPLD1 will send "reset_lock" signal to CPU to indicate the "reset_lock" register status. The default value of "reset_lock" register is "0".

The following is about the reset tree topology.

Figure 7 Switch board Reset Tree

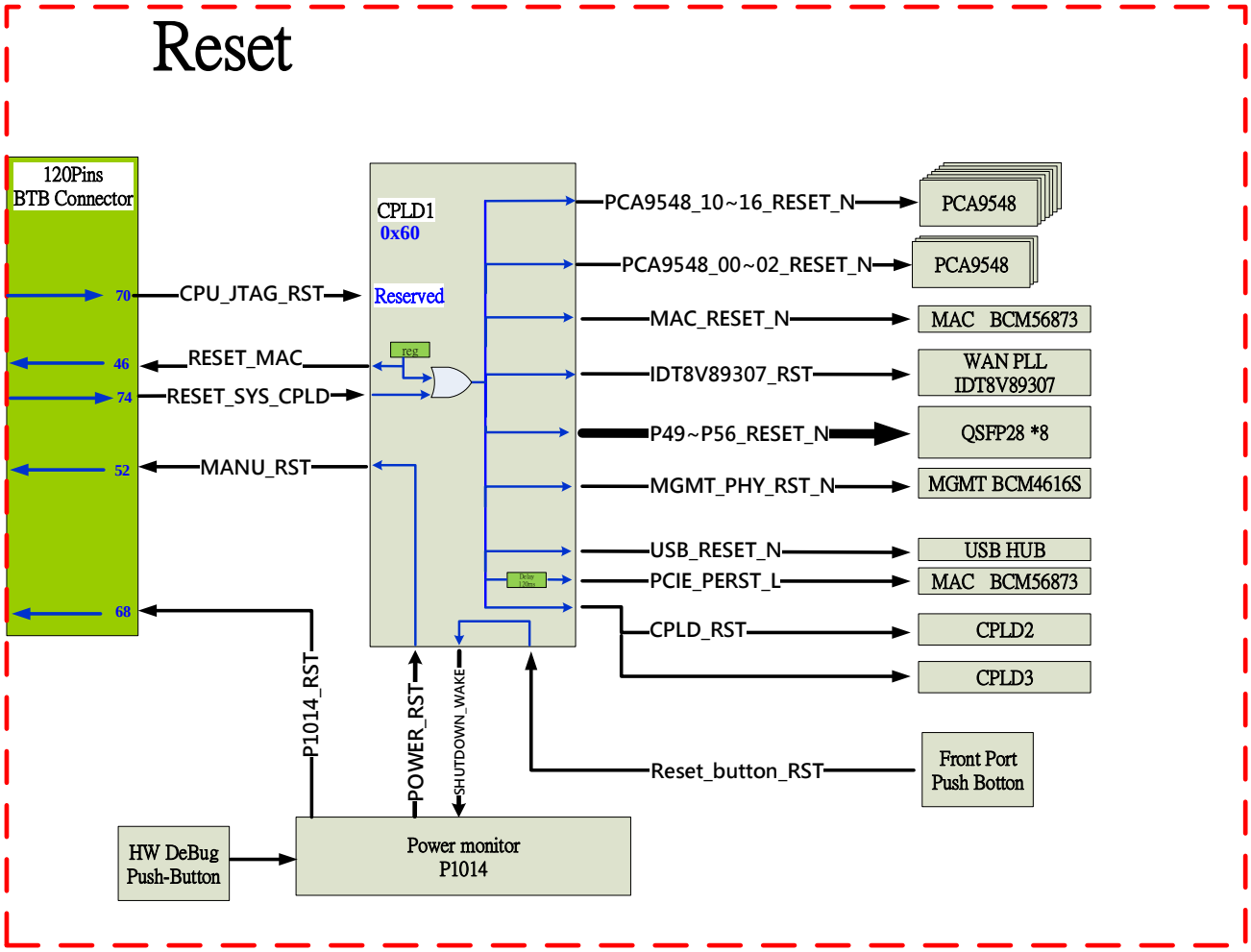
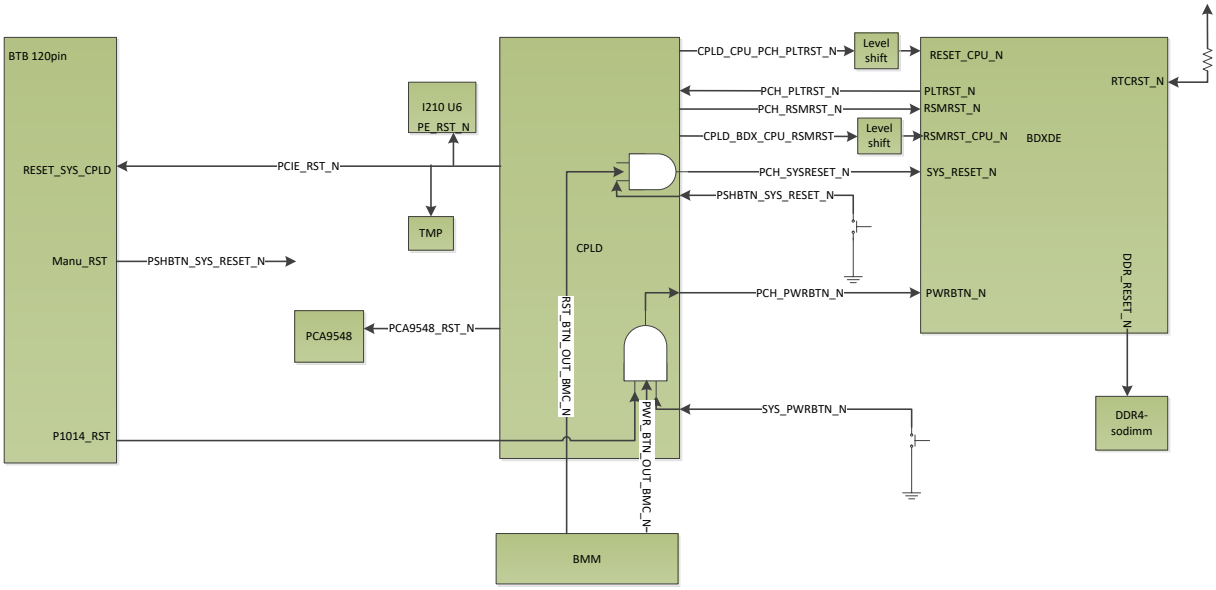


Figure 8 CPU board Reset Tree



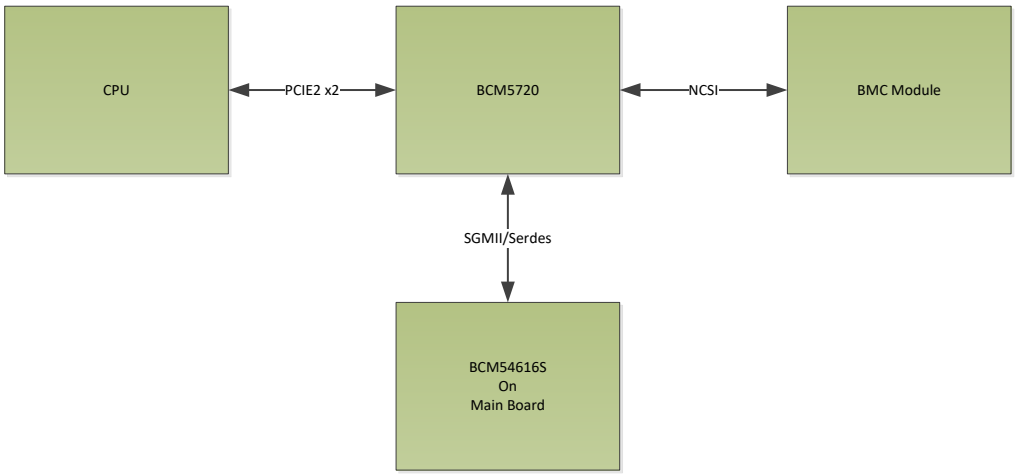
3. Sub-system of CPU Board

The MAC sub-system is used for CPU board to connect the management PHY (BCM54616S) on the main board, the MAC solution is Broadcom BCM56873.

The BMC5720 communicates CPU via PCIE GEN2 x2, and connect to the management port PHY BCM54616S on the main board via SGMII / SERDES.

The NCSI interface is used to connect the BMC module to support share NIC function.

Figure 9 MAC Sub-System Topology



3.1. Configurations of CPU

- 2 DDR channels support DDR4 ECC and non-ECC UDIMM, SODIMM, RDIMM
- Memory speed : DDR4 1600, 1867, 2133, 2400 MT/s
- PCI Express Lanes :
  - 24Gen3, 1x16 and 1x8, 6 controllers x4 granularity (Uncore)
  - 8 Gen2, 2x4, 8controlles x 1 granularity (Integrated PCH logic)
- Integrated 10GbE Controller contains two independent 10GbE MACs that support an XGMII interface link to the either KX4 or KR PHY device interfaces.
  - KX4 PHY supports
    - XAUI for XGMII extension
    - 10GBASE-KX4 for gigabit backplane applications.
    - 2500BASE-KX for gigabit backplane applications.
    - 1000BASE-KX for gigabit backplane applications.
  - KR PHY supports
    - 10GBASE-KR for gigabit backplane application
    - 1000BASE-KX for gigabit backplane application.
    - 10GBASE SFP+ through a XFI compatible interface
    - 10GBASE-T through a XFI compatible interface
- Integrated PCH logic
  - PCI Express Base specification, revision 2.0 support for up to eight ports with transfers up to 5GT/s
  - ACPI power management logic support revision 4.0a
  - Enhanced DMA controller, interrupt controller, and timer function.
  - Integrated Serial ATA host controllers with independent DMA operation on up to six ports.
  - xHCI USB controller provides support for up to 4 USB ports, of which four can be configured as SuperSpeed USB 3.0 ports.
  - One legacy EHCI USB controller provides a USB debug port.
  - Integrated 10/100/1000 Gigabit Ethernet MAC witch system defense.
  - System Management Bus (SMBus) specification, version 2.0 with additional support for I2C devices
  - Supports intel Virtualization Technology for Directed I/O (Intel VT-d)

- Supports intel Trusted Execution Technology (Intel TXT)
- Integrated clock controller
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Serial Peripheral Interface (SPI) support

- JTAG Boundary scan support.

3.1.1. POR of CPU

The cores and uncore supports the following reset types. Note PWRGOOD_CPU is driven by the PCH.

Cold reset is the first time when the platform asserts PWRGOOD_CPU and asserts RESET_CPU_N to the uncore. The platform has to wait for the Base Clock (BCLK) and the power to be stable before asserting PWRGOOD_CPU. This results in reset of all the states in the processor, including the sticky state that is preserved on the other resets. PLLs come up, I/O (DMI2,uncore PCI Express, and DDR) links undergo initialization and calibration. Components in fixed and variable power planes are brought up. Ring, router, SAD, and various lookup tables in the core/Cbo are initialized. Once the uncore initialization has completed, then the power is enabled to the cores and cores are brought out of reset. BIOS is fetched from the PCH.

Warm reset is typically a platform wide event and is indicated by assertion and deassertion of the RESET_CPU_N signal on the socket while PWRGOOD_CPU remains asserted. This reset preserves the error log state and machine check bank states for use by platform debug. The warm reset preserves the error log state and machine check bank states for use by platform for post error event analysis. To maintain the DDR memory attached to the processor self refresh and sticky registers remain valid through out a warm reset, the "Reset_warn" message must complete by the processor. The "Reset_warn" is a message that gets issued from the PCH to all sockets prior to warm reset. BIOS will need to program the FlexRatioMSR/CSR in each socket and invoke the Warm Reset to the platform.

The reset flow is divided into the following 5 phases.

- Phase 0: Expectations from the platform (before assertion of PWRGOOD_CPU)
  - Initially PWRGOOD_CPU signal is deasserted and RESET_CPU_N is asserted to the socket. PWRGOOD_CPU cannot deassert until RESET_CPU_N is asserted.
  - PWRGOOD_CPU must be asserted no sooner than 2 ms after the IVR Vccin supply has fully ramped-up.
  - Vccioin may be brought up before Vccin for IVR is brought up if not at the same time. Vccioin is intended to source the PECI IO.
  - The PWRGOOD_CPU and RESET_CPU_N signals have "clean" edges.
  - The reference clock (BCLK) is stable.
  - All external power rails have ramped as follows: Vccin, Vccioin, VCCD are up and stable at their nominal values
  - Assert PWRGOOD_CPU (RESET_CPU_N still asserted) only after 2 msec of Vccin, Vccioin and VCCD at tolerance.
  - After the power rails are up and stable for 2 msec and reference clocks are stable, platform asserts PWRGOOD_CPU and continues to assert RESET_CPU_N signal to the socket.
  - PWRGOOD_CPU remains asserted as long as Vccin, Vccioin and VCCD remain stable.
  - No power sequencing between Vccin and VCCD is required.
- Phase 1: PCU bring-up

- Phase 1a: Activity Leading to PCU Start-up
  - Assertion of PWRGOOD_CPU (the trigger to move from the end Phase 0 to thestart of Phase 1a).
  - Processor starts a timer (using BCLK) for determinism interval.
  - The PECI and SVID interfaces are held in reset until IVR asserts its power good signal.
  - The PCU PLL is enabled.
- Phase 1b: Pcode Controlled Preparing for Broad uncore Bring-Up
  - Starting at the sub-phase, all steps should be synchronous.
  - PCU micro controller comes out of reset to start reset pcode execution. This is the planned "re-entry" point for Warm Reset processing.
  - Early reset pcode determines that it is at the start of Phase 1b.
  - Pcode brings the rest of the PCU hardware out of reset.
  - Pcode determines the boot config.
  - Pcode issues SVID command to ramp Vccin to 1.8V for cold reset.
  - Pcode reads and compares Vccin MBVR ICCMAX limit (reg 21h) vs its own supported ICCMAX limit:
    - If VR's ICCMAX ≥ supported ICCMAX then bootup continues.
    - If VR's ICCMAX < supported ICCMAX then bootup halts and system shuts down. MSR 411h IA32_MC4_STATUS logs Error code 0x1e - MCA_VR_ICC_MAX_LESS_THAN_FUSED_ICC_MAX in field MSEC_FW.
  - Pcode sequences uncore non-boot IVRs to ramp up.
  - Pcode signals uncore power good to IIO, IMC.
  - Delivery of the uncore power good signals defines the transition from the end of phase 1b to the beginning of phase 1c.
- Phase 1c: PLL locking and IO Calibration
  - Pcode initiates thermal sensors.
  - Pcode locks PLLs in the following order: IIO, and IMC.
  - Pcode instructs the ring PLLs to start locking.
  - RESET_CPU_N signal is deasserted.
  - De-assertion of RESET_CPU_N signal will bring PCU out of reset and signifies the transition from the end of Phase 1c to the beginning of Phase 2.

➢ Phase 2: Uncore initialization and core bring up

- The starting assumptions are:
  - All IVRs except core IVRs have ramped-up and are stable.
  - All PLLs except core PLLs have locked.
  - Phase 2 is entered as a result of de-assertion of external pin RESET_CPU_N.
  - Boot mode related straps have been sampled and are available.
  - Some IO link calibration have started and may or may not have completed by the start of this phase.
- In this phase
  - PCU comes out of reset again and again determines the reset type.
  - Reset is deasserted to the ring units (HA, Cbo, IIO).
  - Reset is de-asserted to System Agents (IMC, IIO).
  - Pcode initializes the ring stops
  - Pcode performs boot mode processing based on straps. Set the advertised firmware, IO, and Intel TXT agent bits appropriately.

        - Pcode services DMI2 handshake protocol. If DMI2 links are used in DMI2 mode, pcode checks if the links have trained to L0. If it's the legacy socket, and if DMI2 links does not reach L0 within 3-4 ms, pcode executes error flow.
        - Pcode determines number of cores, slices and st/mt-threading for the core. In this step pcode also takes into account number of BIOS-disabled cores. Pcode determines whether BIST should be executed. BIST is executed if BIST Strap is set or requested.
        - Pcode programs the logical ids and switches from physical to logical mode.
        - LLC reset and configuration.
        - If it's not service processor boot mode, pcode waits for links to get to parameter exchange.
        - Pcode releases links to get to Normal operation (i.e. L0)
        - Pcode sets core Cstate to C1
- Phase 3: Reset execution (from core reset to fetch boot vector)
    - The starting assumptions are:
        - Before this phase starts, following information is provided to the core: APIC-ID, whether it's the BSP, SMT enable/disable, reset type (cold, warm, C6 exit).
        - Uncore necessary to the get to the BIOS and Intel TXT Address space is fully initialized.
    - In this phase:
        - Initialize core's internal structures, arrays, microarchitectural and architectural state.
        - Execute MLC BIST if BIST enabled.
        - Initialize uncore.
        - Read LLC BIST results from the uncore and report it in the EAX register.
        - Report LLC and MLC BIST results.
        - The core and thread selected as package BSP fetches BIOS or goes to “Wait-for-SIPI” state
        - The end assumption is there is at least one thread that was designated as package BSP.
- Phase 4: BIOS execution

Figure 10 Power Sequencing Diagram G3 with RTC loss to S5

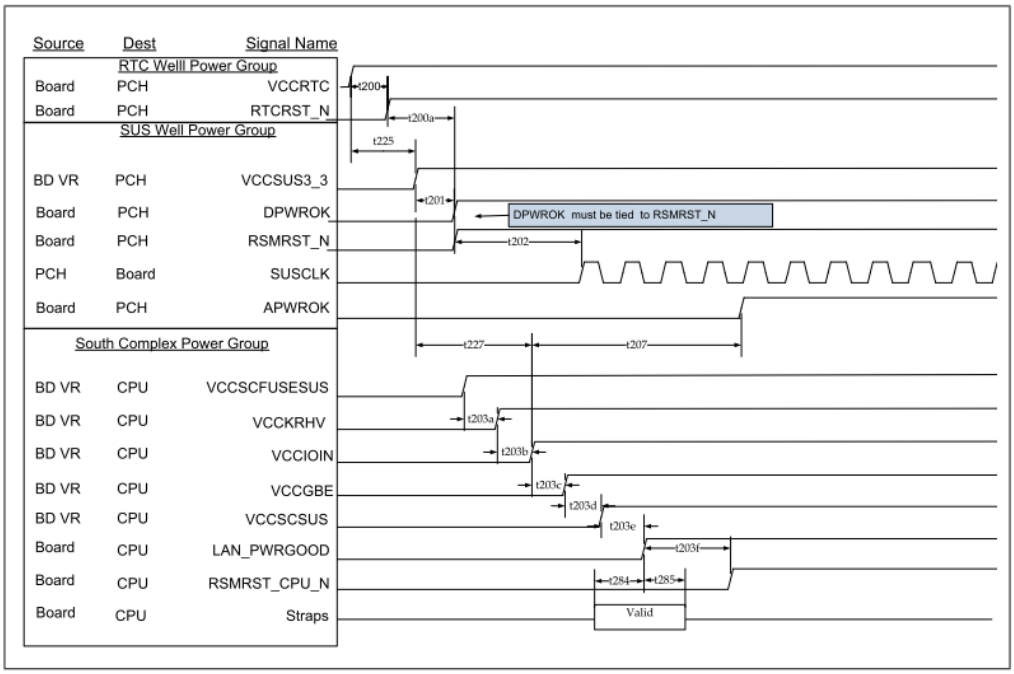
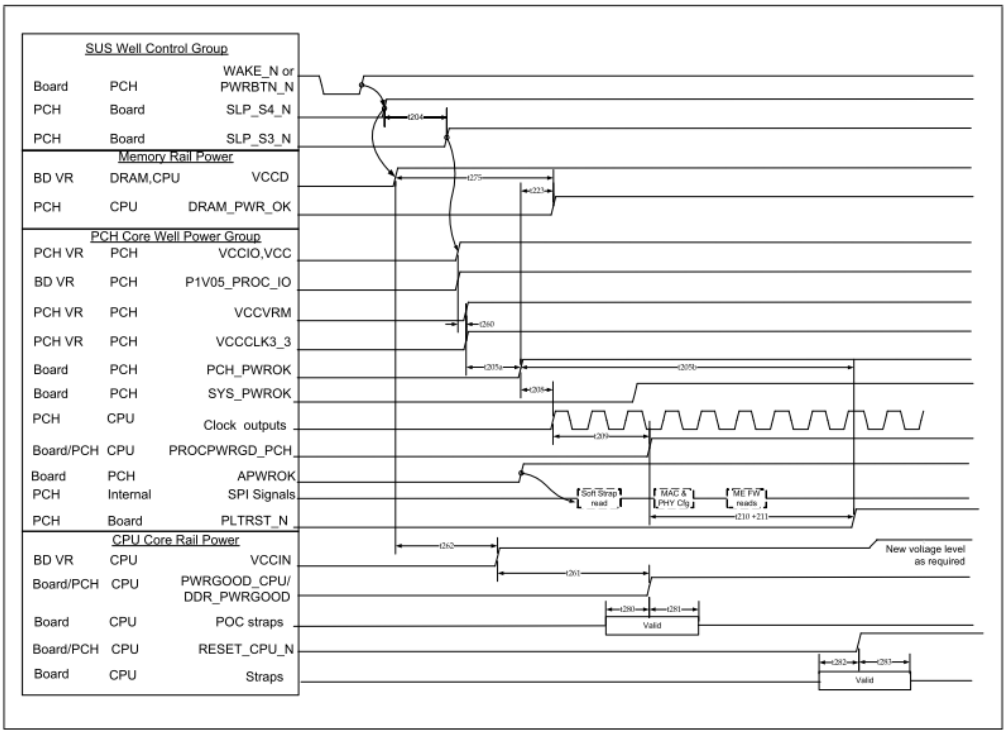


Figure 11 Power Sequencing Diagram S5 to S0



3.2. 1G Interface

The 1G interface could support SGMII or SERDES link, currently configuration is set to SERDES mode to connect BCM54616S in order to support PXE boot function.

Figure 12 Management port function

3.3. Software Configurations of CPU

Figure 13 GPIO

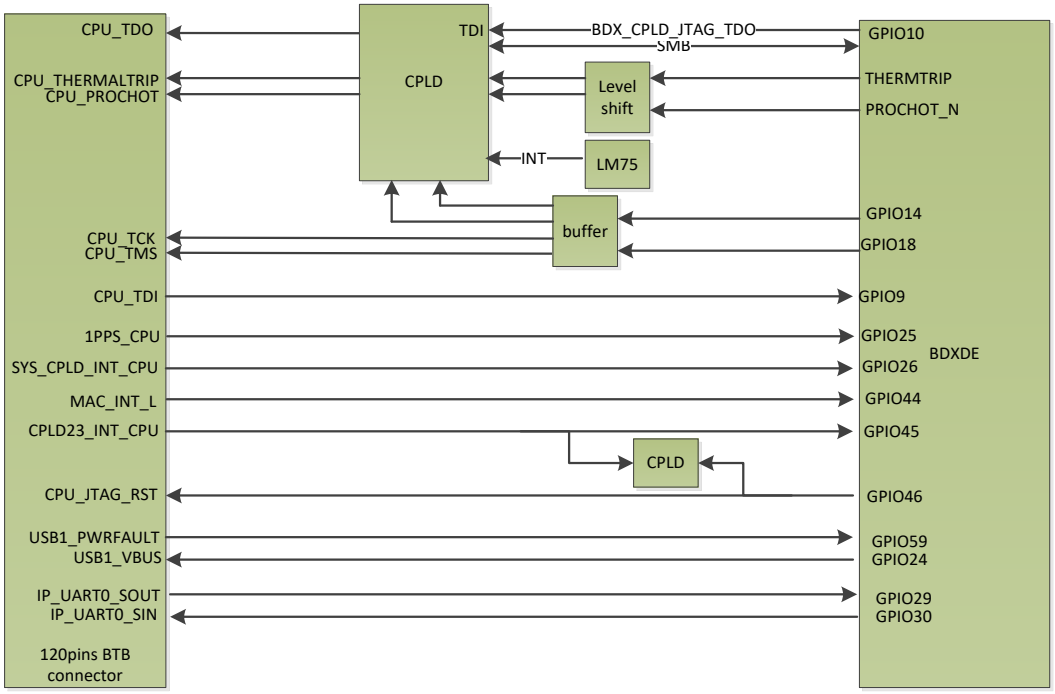


Figure 14 power sequence flow chat

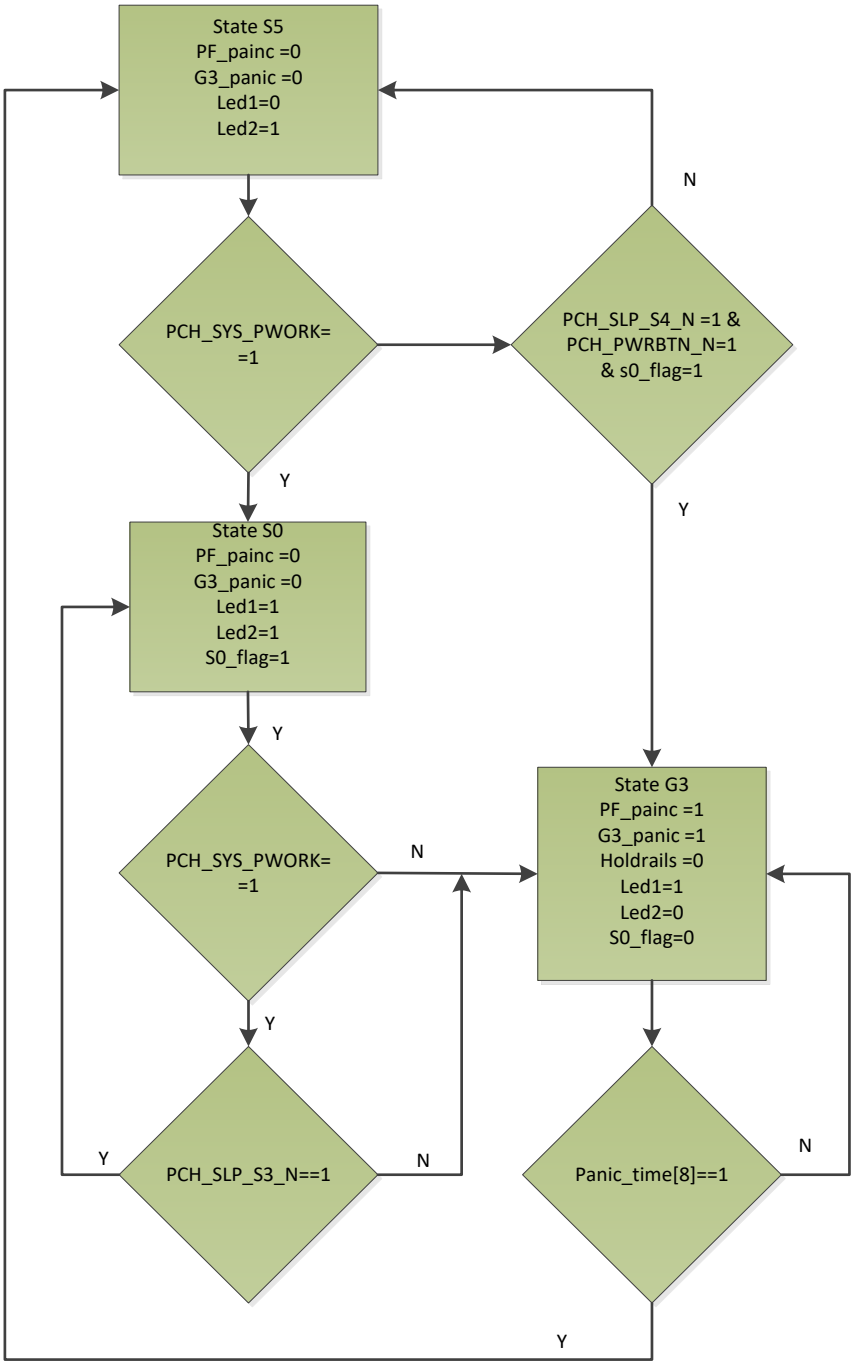


Table 3 GPIO

Pin name	GPIO_USE_SEL 1: GPIO 0: Native	GPIO_IO_SEL 1: input 0: output	function
GPIO0	0	X	BMBUSY#
GPIO1	0	X	TACH1.
GPIO2	0	X	PIRQE#
GPIO3	0	X	PIRQF#.
GPIO4	0	X	PIRQG#
GPIO5	0	X	PIRQH#
GPIO6	0	X	NC
GPIO7	0	X	NC
GPIO8	1	0	PCH_XDP_NCLK1
GPIO9	1	1	XDP_NOA5_PCH/ BDX_CPLD_JTAG_TDI
GPIO10	1	0	XDP_NOA6_PCH/ BDX_CPLD_JTAG_TDO
GPIO11	0	X	SMBALERT#
GPIO12	0	X	LAN_PHY_PWR_CTRL
GPIO14	1	0	XDP_NOA7_PCH/ BDX_CPLD_JTAG_TCK
GPIO15	1	0	SOC_FPGA_CLK
GPIO16	1	0	FM_THROTTLE_PCH_N/ FM_THROTTLE_N
GPIO17	0	X	TACH0
GPIO18	1	0	XDP_NOA14_PCH/ BDX_CPLD_JTAG_TMS
GPIO19	1	BI-DIR	XDP_NOA9_PCH
GPIO20	1	0	FM_SMI_ACTIVE_PCH_N/ FM_SMI_ACTIVE_CPLD_N
GPIO21	1	BI-DIR	XDP_NOA8_PCH
GPIO22	0	X	SCLOCK

GPIO23	X	X	NC
GPIO24	1	0	USB1_VBUS
GPIO25	1	1	1PPS_CPU
GPIO26	1	1	SYS_CPLD_INT_CPU
GPIO27	1	1	SOC_FPGA_DIN
GPIO28	1	0	SOC_FPGA_DOUT
GPIO29	1	1	IP_UART0_SOUT
GPIO30	1	0	IP_UART0_SIN
GPIO31	1	1	SMB_PWR_ALERT
GPIO32	X	X	NC
GPIO33	1	1	4.7K TO GND
GPIO35	1	0	FM_NMI_EVENT_PCH_N/ FM_NMI_EVENT_CPLD_N
GPIO36	1	0	ADR_STATUS_RD
GPIO37	1	1	ADR_STATUS_CLR
GPIO38	0	X	SLOAD
GPIO39	0	X	SDATAOUT0
GPIO40	0	X	OC1#
GPIO41	1	0	XDP_NOA2_PCH/ CPLD_CONFIG_CLK
GPIO42	1	0	XDP_NOA3_PCH/ CPLD_CONFIG_DATA
GPIO43	1	X	XDP_NOA4_PCH_R
GPIO44	1	1	MAC_INT_L
GPIO45	1	1	CPLD23_INT_CPU
GPIO46	1	0	CPU_JTAG_RST
GPIO48	0	X	SDATAOUT1
GPIO49	1	X	FM_CPU_PROCHOT_PCH_N/ FM_PROCHOT_N
GPIO50	X	X	NC
GPIO51	1	1	4.7k pull to 3.3V
GPIO52	1	1	CPU_SV

GPIO53	1	1	1k pull to gnd
GPIO54	X	X	NC
GPIO55	1	1	FM_BIOS_RCRV_BOOT_N
GPIO57	1	1	FM_ME_RCRV_N
GPIO58	0	X	SML1_CLK
GPIO59	1	X	XDP_NOA0_PCH/ USB1_PWRFAULT
GPIO60	0	X	SML0ALERT#
GPIO61	X	X	NC
GPIO62	1	0	PCH_SUSCLK_33K
GPIO65	X	X	NC
GPIO67	X	X	NC
GPIO68	X	X	NC
GPIO69	X	X	NC
GPIO70	X	X	NC
GPIO71	X	X	NC
GPIO72	1	1	1K pull to 3.3V
GPIO74	0	X	SML1ALERT#/TEMP_ALERT#.
GPIO75	0	X	SML1DATA

Table 4 PCH Strap definitions

Strap pin	description	value
SATA1GP/ GPIO19	This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 Reserved 1 1 SPI (default) 0 0 LPC	1
GPIO51	This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 11). This strap is used	1

	in conjunction with Boot BIOS Destination Selection 0 strap.	
SATA3GP /GPIO37	0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).	0
MFG_MODE_STRAP	0 = Enable security measures defined in the Flash Descriptor. 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.	0
INTVRMEN	0 = DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source (should be connected to an external VRM). It should not pull the strap low. 1 = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left as No Connect.	1
GPIO62 / SUSCLK	0 = Disable PLL On-Die voltage regulator. 1 = Enable PLL On-Die voltage regulator.	1
DSWODVREN	0 = Disable Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This mode is only supported for testing environments. 1 = Enable DSW 3.3 V-to-1.05 V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards.	1
SPKR	0 = Disable “No Reboot” mode. 1 = Enable “No Reboot” mode (integrated PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.	
SATA2GP/GPIO36	0 = SoC RX is terminated to VSS. Grangeville platform only supports SoC Rx terminated to VSS. 1 = SoC RX is terminated to VCC/2.	0
GPIO33	0 = SoC TX is terminated to VSS. Grangeville platform only supports SoC Tx terminated to VSS 1 = SoC TX is terminated to VCC/2.	0
GPIO53	0 = SoC is in AC-coupling mode. Grangeville platform only supports AC-coupling mode. 1 = SoC is in DC-coupling mode.	0
GPIO55	0 = Enable “Top Swap” mode. This inverts an address on access to SPI and firmware hub, so the processor believes its fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64 KB blocks in the FWH or the appropriate	1

	address lines (A16, A17, A18, A19, or A20) as selected in Top-Swap Block size soft strap (handled through FITc. 1 = Disable “Top Swap” mode.	
GPIO8	This pin must not be driven low until after rising edge of RSMRST_N.	1
GPIO44	This pin must not be driven low until after rising edge of RSMRST_N.	1
GPIO46	This pin must not be driven low until after rising edge of RSMRST_N.	1
BIST_ENABLE	Build-in Self Test (BIST) enable strap: 0 = BIST Disable 1 = BIST Enable	0
BMCINIT	Integrated Service Processor Boot Mode Selection: 0 = Integrated Service Processor Boot Mode Disabled. 1 = Integrated Service Processor Boot Mode Enable	1
TXT_PLTEN	0 = The platform is not Intel TXT enabled. 1 = Default. The platform is Intel TXT enabled.	0
TXT_AGENT	0 = Default. The SoC is not the Intel TXT Agent. 1 = The SoC is the Intel TXT Agent.	0
SAFE_MODE_BOOT	0 = Safe Mode Boot Disabled 1 = Safe Mode Boot Enabled	1
DEBUG_EN_N	0 = Debug Mode 1 = Normal Mode	XDP_PRESENT_N
DDR3_4_STRAP	Select between DDR4 and DDR3 0 = DDR3, it requires <1K ohm pull down in order to out drive the internal pull up. 1= DDR4 (Default)	1
PECI0 ; PECI1 ; PECI2	In micro-server design space, there will be multiple sockets that share a PECI bus. However these sockets are effectively independent agents. The PECI IDs are used as straps to identify which socket is which in order for PECI bus to work.	000
LAN_MDIO_DIR_CTL_0; LAN_MDIO_DIR_CTL_1	00 = Both LAN ports are disabled. Note: In this mode manageability is not functional and must not be enabled in NVM control word 1. 01 = Port 1 is disabled. Port 0 is enabled. 10 = Reserved 11 = Both Port 0 and 1 are enabled. Recommend 5.1K ohm pull up to VCCIOIN or 5.1K ohm pull down to GND.	11

RSVD12_AJ67	This pin should have a 5.1K ohm pull down to GND.	0
RSVD11_AG67	This pin should have a 5.1K ohm pull down to GND.	0
RSVD10_AN78	This pin should have a 5.1K ohm pull down to GND.	0
RSVD09_AC64	This pin should have a 5.1K ohm pull down to GND.	0
SERIRQ_DIR	Recommend 5.1k ohm pull up to VCCIOIN.	1
UART_TXD[0]	Recommend 5.1k ohm pull down to GND.	0
UART_TXD[1]	Controls the security attributes on the NVM - for pre-production usage only. 0 = Disable NVM Security (Default) 1 = Security Enabled Recommend 5.1K ohm pull down to GND.	0
LAN_NCSI_RXD0	Recommend 5.1K ohm pull up to VCCIOIN.	1
LAN_NCSI_RXD1	Enable/Disable manageability traffic: 0 = LAN available in S5 for WoL (Default) 1 = LAN not available in S5. Manageability is disabled. Recommend 5.1K ohm pull down to GND.	0
LAN_NCSI_ARB_OUT	Selects SVID VR Operating Mode 1 - VCCSCSUS, P1V05_PCH, VCCGBE, VCCIOIN are combined into one SVID controlled supply. 0 - Separate SVID controllers (default).	1
RSVD84	49.9Ω 1% to GND	0
RSVD93	1k - 5.1kΩ to GND	0
RSVD94	1k - 5.1kΩ to GND	0
RSVD00	1k - 5.1kΩ to VCC3_3	1
RSVD18	1k - 5.1kΩ to GND	0
RSVD16	1k - 5.1kΩ to GND	0
RSVD17	1k - 5.1kΩ to GND	0
RSVD21	1k - 5.1kΩ to GND	0
NCTF/TP	1k - 5.1kΩ to VCC3_3	1

3.4. Memory Mapping

Broadwell-DE SoC contains registers that are located in the processor I/O space and memory space and sets of PCI configuration registers that are located in PCI configuration space. This chapter describes Broadwell-DE SoC I/O and memory maps at the register-set level. Register access is also described.

Table 5 PCI devices and functions

Bus:Device:Function	Function Description
Bus0:Device31:Function0	LPC controller
Bus0:Device31:Function2	SATA controller #1
Bus0:Device31:Function3	SMBus controller
Bus0:Device31:Function5	SATA controller#2

Bus0:Device31:Function6	Thermal subsystem
Bus0:Device29:Function0	USB EHCI controller#1
Bus0:Device28:Function0	PCI-e port1
Bus0:Device28:Function1	PCI-e port2
Bus0:Device28:Function2	PCI-e port3
Bus0:Device28:Function3	PCI-e port4
Bus0:Device28:Function4	PCI-e port5
Bus0:Device28:Function5	PCI-e port6
Bus0:Device28:Function6	PCI-e port7
Bus0:Device28:Function7	PCI-e port8
Bus0:Device25:Function0	Gigabit Ethernet controller
Bus0:Device22:Function0	Intel management engine interface#1
Bus0:Device22:Function1	Intel management engine interface#2
Bus0:Device22:Function2	IDE-R
Bus0:Device22:Function3	KT
Bus0:Device20:Function0	xHCI controller

Table 6 Fixed I/O ranges decoded by Broadwell-DE

I/O Address	Read Target	Write Target	Internal Unit
00h-08h	DMA controller	DMA controller	DMA
09h-0Eh	reserved	DMA controller	DMA
0Fh	DMA controller	DMA controller	DMA
10h-18h	DMA controller	DMA controller	DMA
19h-1Eh	reserved	DMA controller	DMA
1Fh	DMA controller	DMA controller	DMA
20h-21h	Interrupt controller	Interrupt controller	interrupt
24h-25h	Interrupt controller	Interrupt controller	interrupt
28h-29h	Interrupt controller	Interrupt controller	interrupt
2Ch-2Dh	Interrupt controller	Interrupt controller	interrupt
2Eh-2Fh	LPC SIO	LPC SIO	Forwarded to LPC
30h-31h	Interrupt controller	Interrupt controller	interrupt
34h-35h	Interrupt controller	Interrupt controller	interrupt
38h-39h	Interrupt controller	Interrupt controller	interrupt
3Ch-3Dh	Interrupt controller	Interrupt controller	interrupt
40h-42h	Timer/Counter	Timer/Counter	PIT
43h	reserved	Timer/Counter	PIT
4Eh-4Fh	LPC SIO	LPC SIO	Forwarded to LPC
50h-52h	Timer/Counter	Timer/Counter	PIT
53h	reserved	Timer/Counter	PIT
60h	microcontroller	microcontroller	Forwarded to LPC
61h	NMI controller	NMI controller	Processor I/F
62h	microcontroller	microcontroller	Forwarded to LPC
64h	microcontroller	microcontroller	Forwarded to LPC
66h	microcontroller	microcontroller	Forwarded to LPC

70h	reserved	NMI and RTC controller	RTC
71h	RTC controller	RTC controller	RTC
72h	RTC controller	NMI and RTC controller	RTC
73h	RTC controller	RTC controller	RTC
74h	RTC controller	NMI and RTC controller	RTC
75h	RTC controller	RTC controller	RTC
76h	RTC controller	NMI and RTC controller	RTC
77h	RTC controller	RTC controller	RTC
80h	DMA controller, LPC, PCI or PCIe	DMA controller, LPC, PCI or PCIe	DMA
81h-83h	DMA controller	DMA controller	DMA
84h-86h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
87h	DMA controller	DMA controller	DMA
88h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
89h-8Bh	DMA controller	DMA controller	DMA
8Ch-8Eh	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
8Fh	DMA controller	DMA controller	DMA
90h-91h	DMA controller	DMA controller	DMA
92h	Reset generator	Reset generator	Processor I/F
93h-9Fh	DMA controller	DMA controller	DMA
A0h-A1h	Interrupt controller	Interrupt controller	interrupt
A4h-A5h	Interrupt controller	Interrupt controller	interrupt
A8h-A9h	Interrupt controller	Interrupt controller	interrupt
ACh-ADh	Interrupt controller	Interrupt controller	interrupt
B0h-B1h	Interrupt controller	Interrupt controller	interrupt
B2h-B3h	Power management	Power management	Power management
B4h-B5h	Interrupt controller	Interrupt controller	interrupt
B8h-B9h	Interrupt controller	Interrupt controller	interrupt
BCh-BDh	Interrupt controller	Interrupt controller	interrupt
C0h-D1h	DMA controller	DMA controller	DMA
D2h-DDh	reserved	DMA controller	DMA
DEh-DFh	DMA controller	DMA controller	DMA
F0h	Ferr#/interrupt controller	Ferr#/interrupt controller	Processor I/F
170h-177h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
1F0h-1F7h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
200h-207h	Gameport low	Gameport low	Forwarded to LPC
208h-20Fh	Gameport high	Gameport high	Forwarded to LPC
376h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
3F6h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
4D0h-4D1h	Interrupt controller	Interrupt controller	interrupt
CF9h	Reset generator	Reset generator	Processor I/F

Table 7 Variable I/O decode ranges

Range name	Mappable	Size (bytes)	Target
ACPI	Anywhere in 64KB I/O space	64	Power management
IDE bus master	Anywhere in 64KB I/O space	1. 16 or 32 2. 16	1. SATA host controller #1, #2 2. IDE-R
Native IDE command	Anywhere in 64KB I/O space	8	1. SATA host controller #1, #2 2. IDE-R
Native IDE control	Anywhere in 64KB I/O space	4	1. SATA host controller #1, #2 2. IDE-R
SATA index/data pair	Anywhere in 64KB I/O space	16	1. SATA host controller #1, #2 2. IDE-R
SMBus	Anywhere in 64KB I/O space	32	SMB unit
TCO	96 bytes above ACPI base	32	TCO unit
GPIO	Anywhere in 64KB I/O space	128	GPIO unit
Parallel port	3 ranges in 64KB I/O space	8	LPC peripheral
Serial port 1	8 ranges in 64KB I/O space	8	LPC peripheral
Serial port 2	8 ranges in 64KB I/O space	8	LPC peripheral
Floppy disk controller	2 ranges in 64KB I/O space	8	LPC peripheral
LAN	Anywhere in 64KB I/O space	32	LAN unit
LPC generic 1	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 2	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 3	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 4	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
I/O trapping ranges	Anywhere in 64KB I/O space	1 to 256	Trap on backbone
PCI bridge	Anywhere in 64KB I/O space	I/O base/limit	PCI bridge
PCI-E root ports	Anywhere in 64KB I/O space	I/O base/limit	PCI-E root ports 1-8
KT	Anywhere in 64KB I/O space	8	KT

Table 8 Memory decode ranges from processor perspective

Memory range	target	Dependency/comments
0000 0000h-000D FFFFh 0010 0000h-TOM	Main memory	TOM registers in host controller
000E 0000h-000E FFFFh	LPC or SPI	Bit 6 in BIOS decode enable register is set
000F 0000h-000F FFFFh	LPC or SPI	Bit 7 in BIOS decode enable register is set
FEC_ _000h-FEC_ _040h	IOx APCI inside broadwell-de SoC	_ _ is controlled using APIC range select (ASEL) field and APIC enable (AEN) bit.
FEC1 0000h-FEC1 7FFFh	PCI-E port 1	PCI-E root port 1 I/OxAPIC enable (PAE) set
FEC1 8000h-FEC1 FFFFh	PCI-E port 2	PCI-E root port 2 I/OxAPIC enable (PAE) set
FEC2 0000h-FEC2 7FFFh	PCI-E port 3	PCI-E root port 3 I/OxAPIC enable (PAE) set
FEC2 8000h-FEC2 FFFFh	PCI-E port 4	PCI-E root port 4 I/OxAPIC enable (PAE) set
FEC3 0000h-FEC3 7FFFh	PCI-E port 5	PCI-E root port 5 I/OxAPIC enable (PAE) set
FEC3 8000h-FEC3 FFFFh	PCI-E port 6	PCI-E root port 6 I/OxAPIC enable (PAE) set
FEC4 0000h-FEC4 7FFFh	PCI-E port 7	PCI-E root port 7 I/OxAPIC enable (PAE) set
FEC4 8000h-FEC4 FFFFh	PCI-E port 8	PCI-E root port 8 I/OxAPIC enable (PAE) set

FFC0 0000h-FFC7 FFFFh FF80 0000h- FF87 FFFFh	LPC or SPI (or PCI)	Bit 8 in BIOS decode enable register is set
FFC8 0000h-FFCF FFFFh FF88 0000h- FF8F FFFFh	LPC or SPI (or PCI)	Bit 9 in BIOS decode enable register is set
FFD0 0000h-FFD7 FFFFh FF90 0000h- FF97 FFFFh	LPC or SPI (or PCI)	Bit 10 in BIOS decode enable register is set
FFD8 0000h-FFDF FFFFh FF98 0000h- FF9F FFFFh	LPC or SPI (or PCI)	Bit 11 in BIOS decode enable register is set
FFE0 0000h-FFE7 FFFFh FFA0 0000h- FFA7 FFFFh	LPC or SPI (or PCI)	Bit 12 in BIOS decode enable register is set
FFE8 0000h-FFEF FFFFh FFA8 0000h- FFAF FFFFh	LPC or SPI (or PCI)	Bit 13 in BIOS decode enable register is set
FFF0 0000h-FFF7 FFFFh FFB0 0000h-FFB7 FFFFh	LPC or SPI (or PCI)	Bit 14 in BIOS decode enable register is set
FFF8 0000h–FFFF FFFFh FFB8 0000h–FFBF FFFFh	LPC or SPI (or PCI)	Always enabled. The top two 64KB blocks of this range can be swapped.
FF70 0000h–FF7F FFFFh FF30 0000h–FF3F FFFFh	LPC or SPI (or PCI)	Bit 3 in BIOS Decode Enable register is set
FF60 0000h–FF6F FFFFh FF20 0000h–FF2F FFFFh	LPC or SPI (or PCI)	Bit 2 in BIOS Decode Enable register is set
FF50 0000h–FF5F FFFFh FF10 0000h–FF1F FFFFh	LPC or SPI (or PCI)	Bit 1 in BIOS Decode Enable register is set
FF40 0000h–FF4F FFFFh FF00 0000h–FF0F FFFFh	LPC or SPI (or PCI)	Bit 0 in BIOS Decode Enable register is set
128 KB anywhere in 4 GB range	Integrated LAN Controller	Enable using BAR in D25:F0 (Integrated LAN Controller MBARA)
4 KB anywhere in 4 GB range	Integrated LAN Controller	Enable using BAR in D25:F0 (Integrated LAN Controller MBARB)
1 KB anywhere in 4 GB range	USB EHCI Controller #1	Enable using standard PCI mechanism (D29:F0)
64 KB anywhere in 4 GB range	USB xHCI Controller	Enable using standard PCI mechanism (D20:F0)
FED0 X000h–FED0 X3FFh	High Precision Event Timers	BIOS determines the “fixed” location which is one of four, 1-KB ranges where X (in the first column) is 0h, 1h, 2h, or 3h.
FED4 0000h–FED4 FFFFh	TPM on LPC	None
Memory Base/Limit anywhere in 4 GB range	PCI Bridge	Enable using standard PCI mechanism (D30:F0)
Prefetchable Memory Base/Limit anywhere in 64-bit address range	PCI Bridge	Enable using standard PCI mechanism (D30:F0)
64 KB anywhere in 4 GB range	LPC	LPC Generic Memory Range. Enable using setting bit[0] of the LPC Generic Memory Range register (D31:F0:offset 98h).
32 Bytes anywhere in 64-bit address range	SMBus	Enable using standard PCI mechanism (D31:F3)
2 KB anywhere above 64 KB to 4 GB range	SATA Host Controller #1	AHCI memory-mapped registers. Enable using standard PCI mechanism (D31:F2)

Memory Base/Limit anywhere in 4 GB range	PCI Express* Root Ports 1-8	Enable using standard PCI mechanism (D28: F 0-7)
Prefetchable Memory Base/Limit anywhere in 64-bit address range	PCI Express Root Ports 1-8	Enable using standard PCI mechanism (D28:F 0-7)
4 KB anywhere in 64-bit address range	Thermal Reporting	Enable using standard PCI mechanism (D31:F6 TBAR/ TBARH)
4 KB anywhere in 64-bit address range	Thermal Reporting	Enable using standard PCI mechanism (D31:F6 TBARB/TBARBH)
16 Bytes anywhere in 64-bit address range	Intel® MEI #1, #2	Enable using standard PCI mechanism (D22:F 1:0)
4 KB anywhere in 4 GB range	KT	Enable using standard PCI mechanism (D22:F3)
16 KB anywhere in 4 GB range	Root Complex Register Block (RCRB)	Enable using setting bit[0] of the Root Complex Base Address register (D31:F0:offset F0h).

3.5. FLASH

There are four SPI flashs, 2 x 128Mb for BIOS, 1 x 32Mb for 10GBE controller +and 1 x 16Mb for BCM5720.

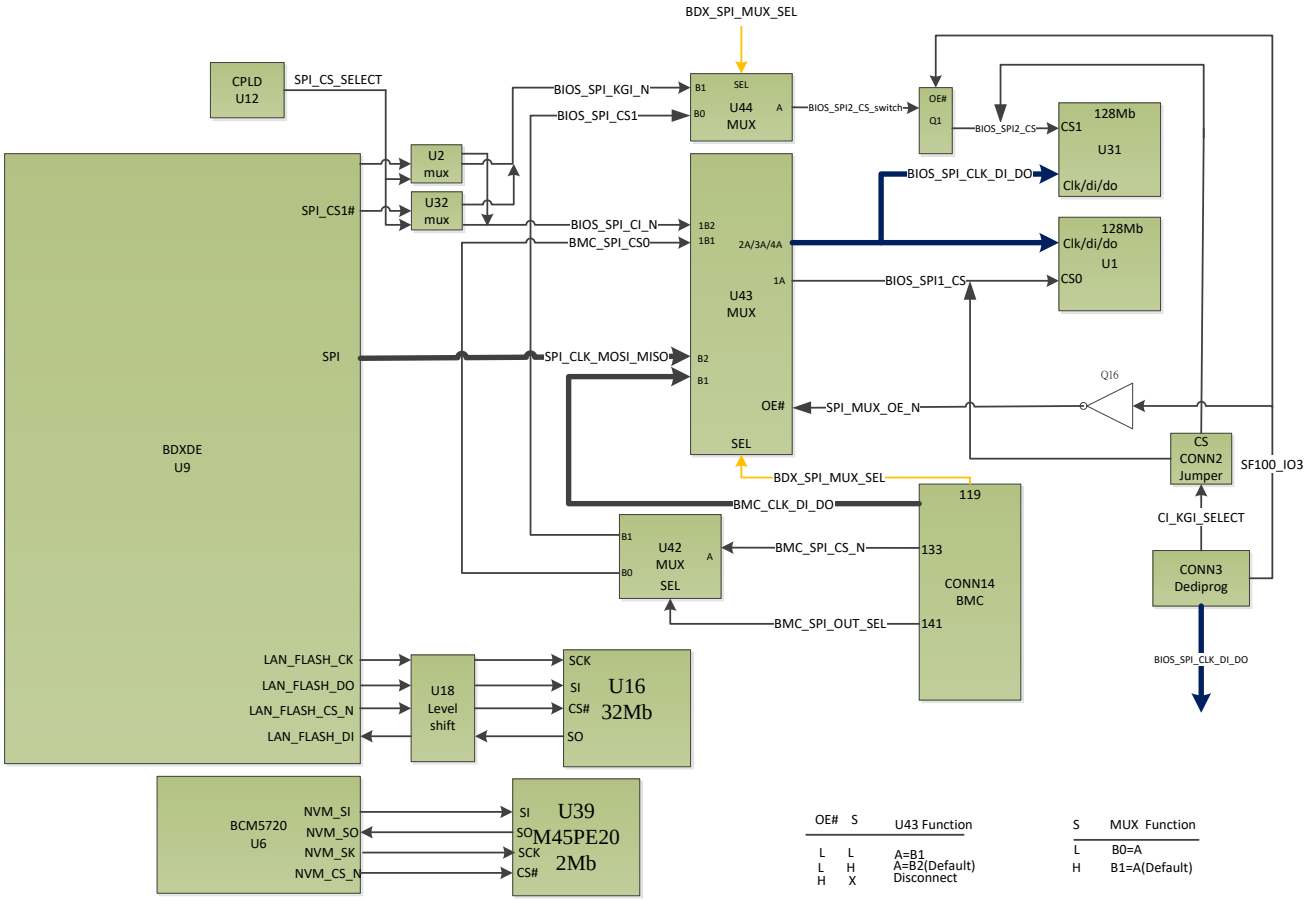
The two 128Mb flash are for system boot BIOS, one is primary another one is backup.

There are two ways that can update the BIOS flash, one is via dediprog , the other is via BMC module. If user want to update bios from BMC, the “BDX_SPI_MUX_SEL” would be pull low from high.

The 32Mb flash is for 10G controller setup and the 16Mb flash is for BCM5720 MAC setup.

The system boot flash SPI clock rate is 20MHz via the SPI memory mapped configuration register SSFC[18:16] = “000” setting and the CPU GbE LAN SPI flash clock rate is 20MHz via the GBE LAN memory mapped configuration register SSFC[18:16] = “000” setting.

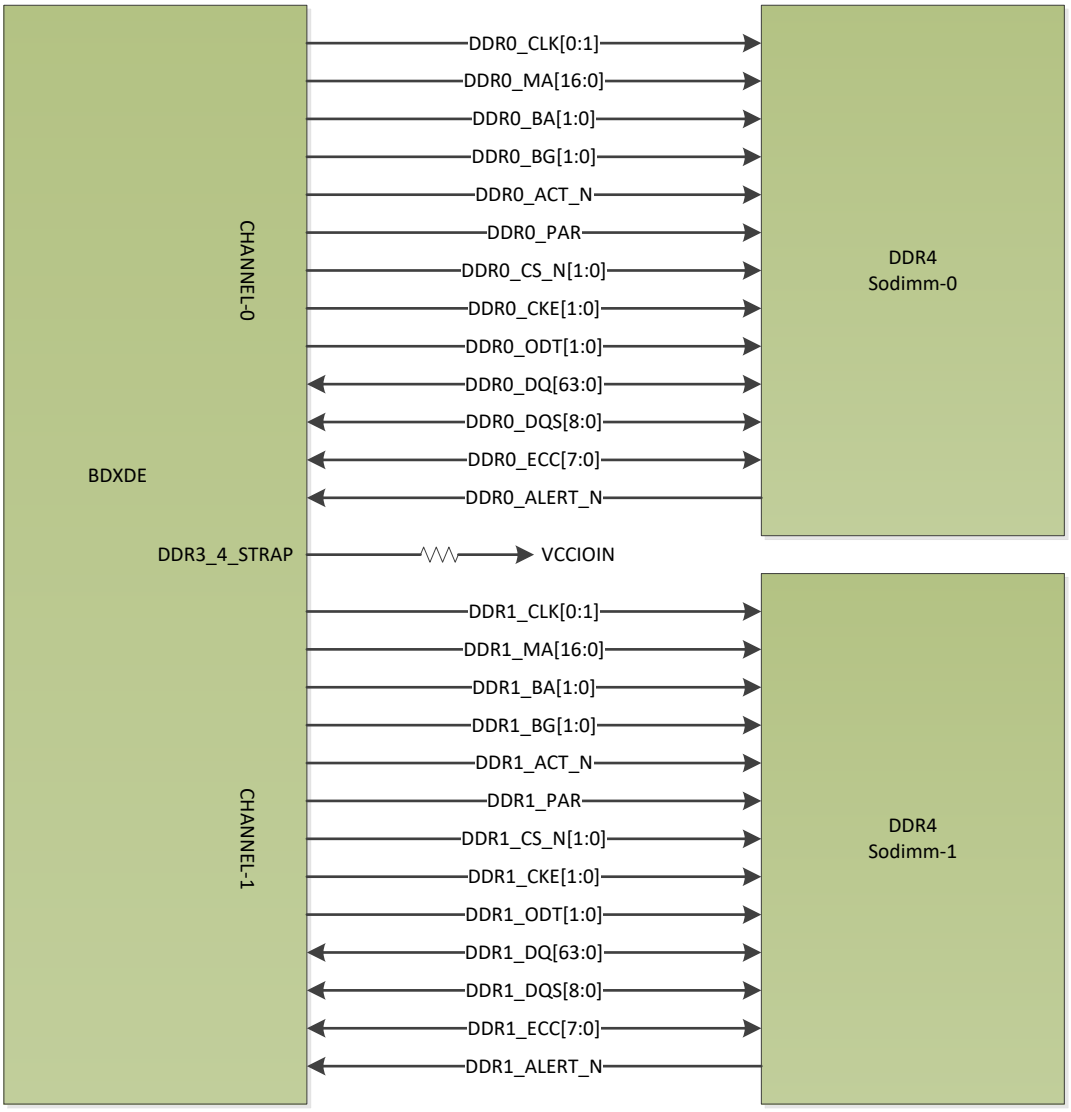
Figure 15 FLASH Connection



3.6. RAM

The BDXDE can support memory DDR3 and DDR4 that need via strap pin DDR3_4_STRAP to configure which one be supported. The project support two DDR4 SODIMM with ECC that has to pull DDR3_4_STRAP to high.

Figure 16 RAM Connection



3.7. PCIe

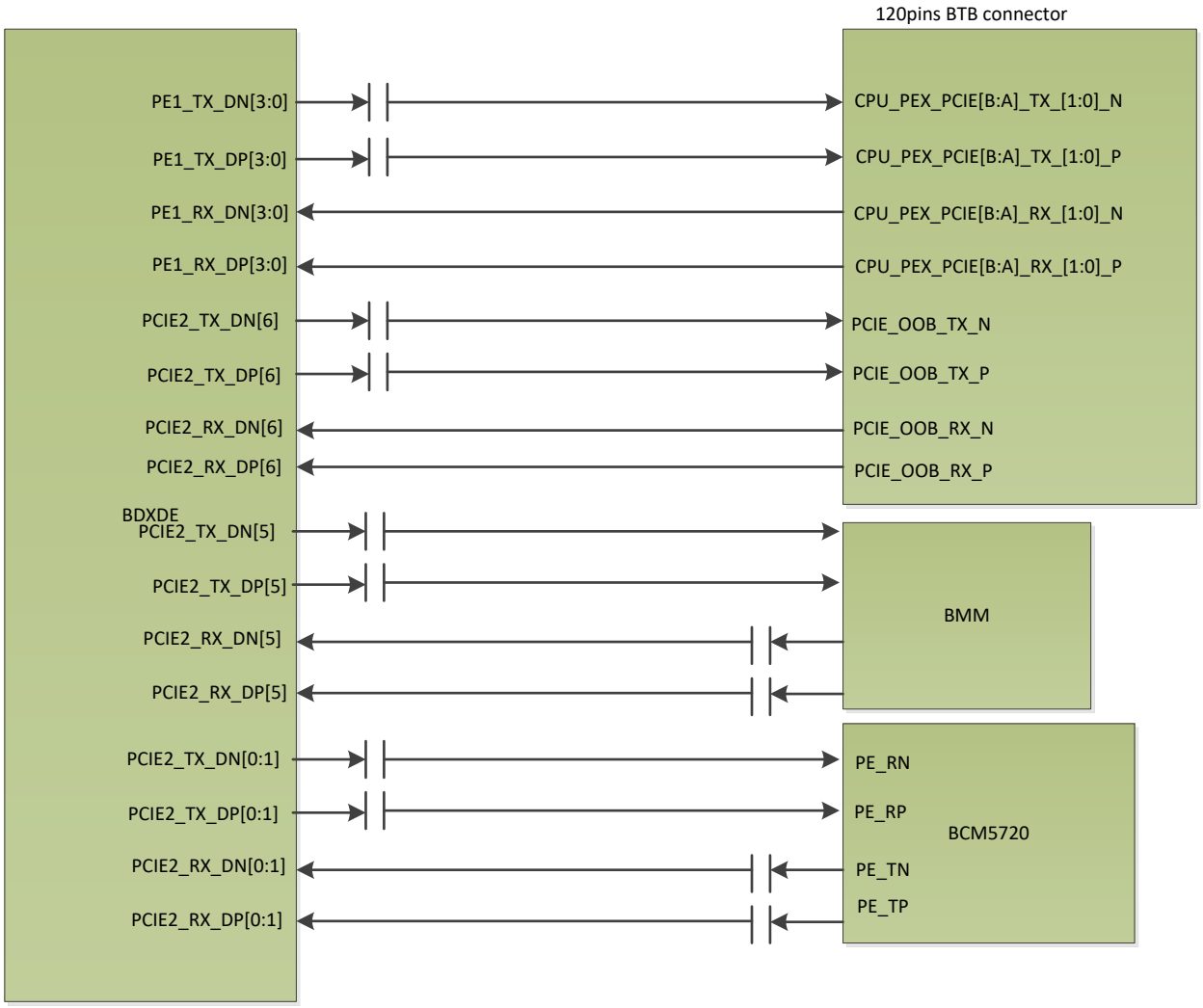
The CPU board has to provide the x4 PCIE Gen3 and x1 PCIE Gen2 to main board. The x4 PCIE GEN3 is used to connect the NP8365 for control path, the PCIE GEN2 x1 is sued to communicate the OOB.

There are other PCIE GEN2 that connect to on board MAC BCM5720 and BMC module.

The PCIE interface connected to BCM5720 is PCIE GEN2 x2.

The PCIE interface connected to BMC module is PCIE GEN2 x1, which is used to active the graphic inside the BMC chip to achieve the vKVM and vMedia function through IPMI when the BMC chip uses AST2400.

Figure 17 PCIe Connection



3.8. I2C/SMBus Architecture

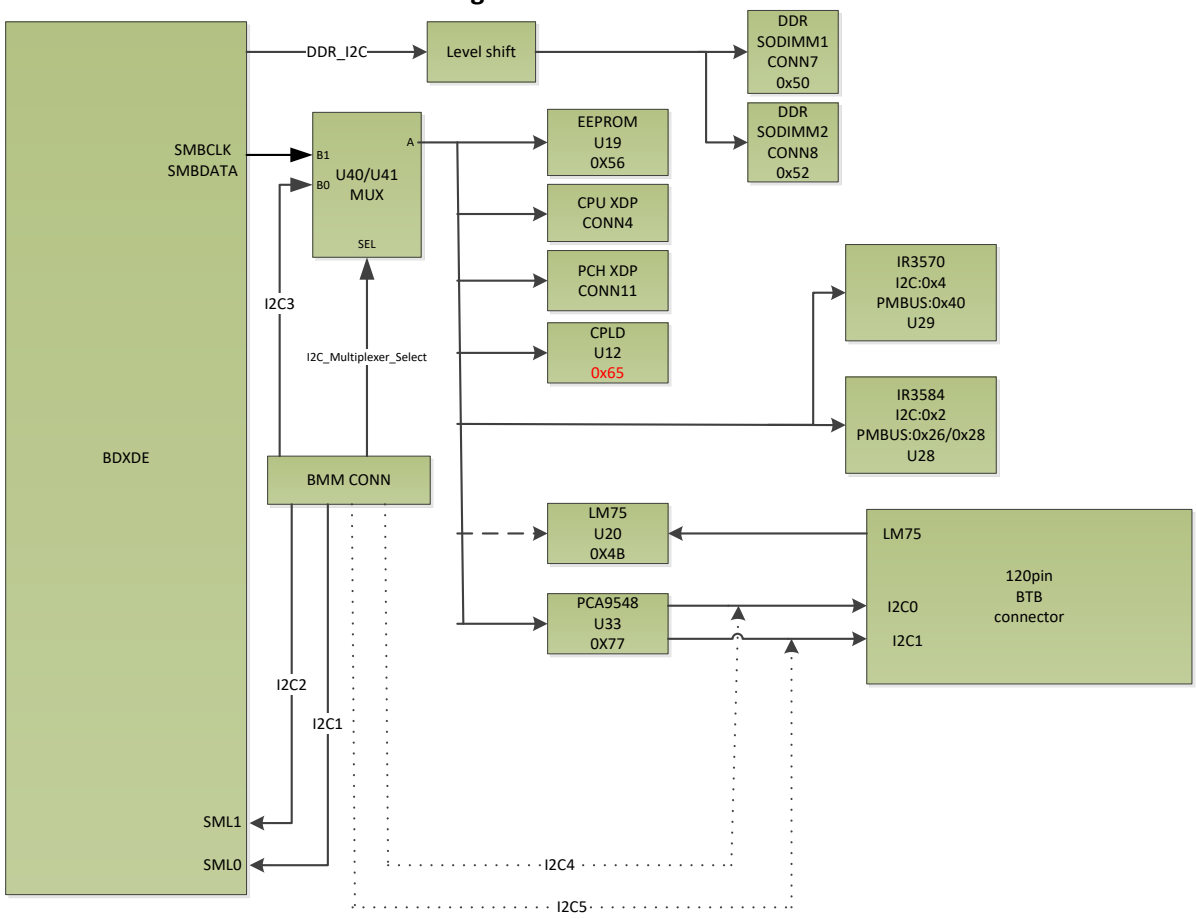
The SMbus from Broadwell-DE can access the CPU board and main board device via SMBUS0.

The multiplexers(MUX) are used to prevent multi-master issues on the SMBUS.

The BMC module could use the SMBUS when the I2C_multiplexer_select pin is driven from high to low.

In order to prevent the hang-up issue which occurred when the CPU is accessing the SMBUS and BMC module want to take the bus master (I2C_multiplexer_select would be driven low), if the BMC module is installed, BMC would be the master for all SMBUS, CPU would ask BMC for SMBUS information via LPC by IPMI.

Figure 18 I2C Connection



Note: I2C[1:5] are from the BMM point of view, not related to the I2C[0:1] through the B2B CONN

Table 9 SMBus 0 Address Table

Device	I2C address	Note
DDR4 SODIMM 1	0x50	This device need to be accessed by DDR_I2C interface
DDR4 SODIMM 2	0x52	This device need to be accessed by DDR_I2C interface
LM75	0x4B	This device need to be accessed by main board CPLD, and not display at SMBus 0.
EEPROM	0x56	
IR3584 (I2C)	0x02	

IR3584 (PMBUS-Loop1)	0x26	
IR3584 (PMBus-Loop2)	0x28	
IR3570 (I2C)	0x4	
IR3570 (PMBus Loop1)	0x42	
PCA9548	0X77	For main board

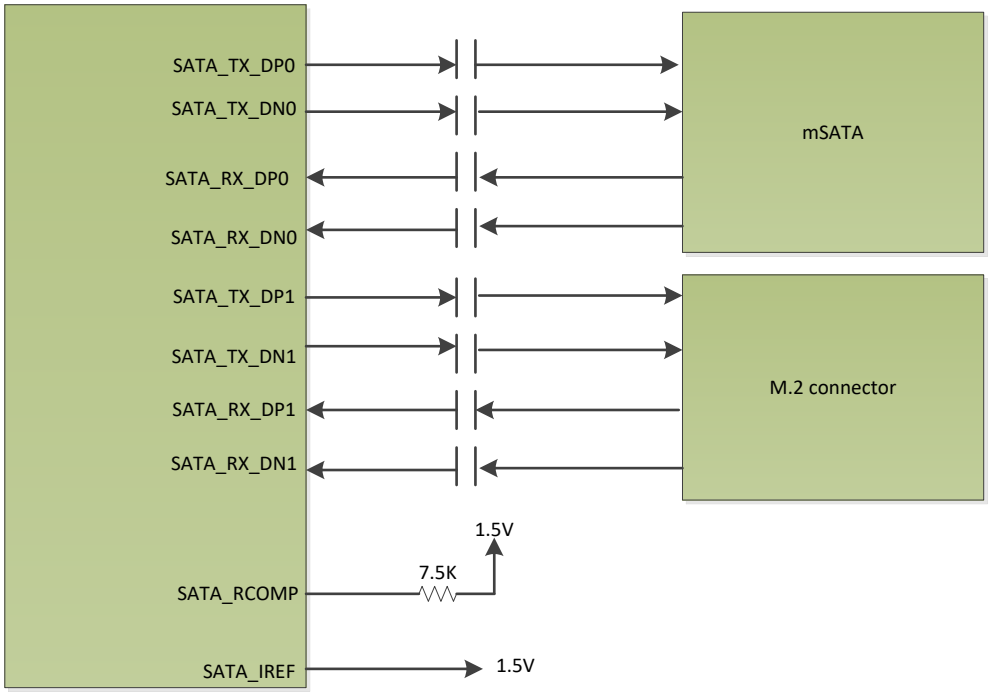
3.9. SATA

The CPU board supports 2 SATA SSD devices via SATA 3.0 interface.
SATA 3.0 CH0 support mSATA SSD module.
SATA 3.0 CH1 support m.2 SSD module.
The following table shows the mSATA and m.2 SSD module dimension and size.

Table 10 SATA SSD Module Table

Type	Dimension	Capacity
mSATA SSD	50.8mm x 29.85mm x 4.0mm	16GB~512GB (option)
M.2 SSD	42.0mm × 22.0mm × 3.5mm	32GB~256GB (default)
	80.0mm x 22.0mm	32GB~512GB (option)

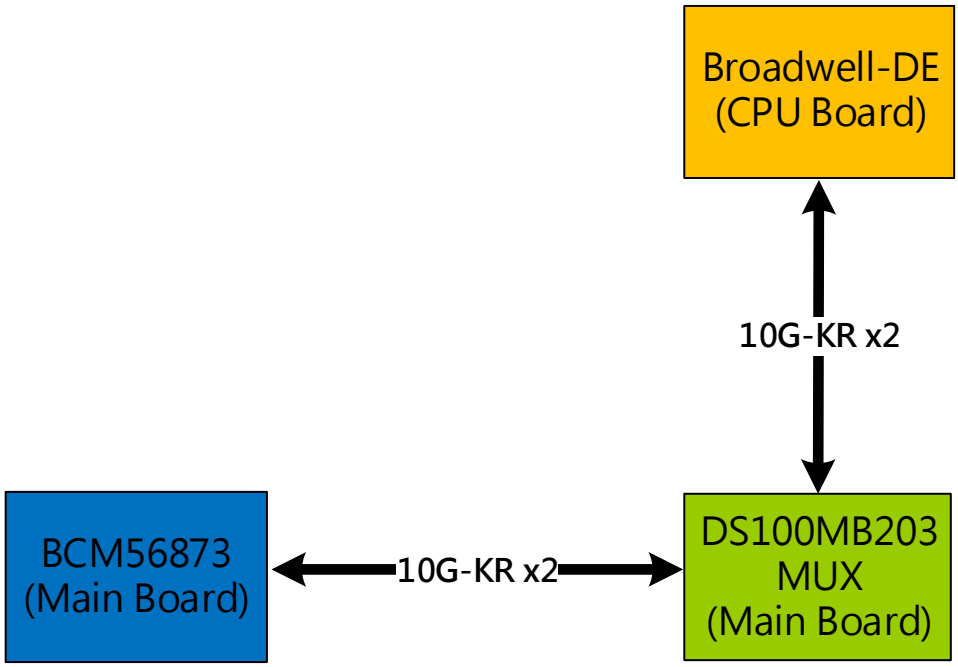
Figure 19 SATA Connection



3.10. 10G-Base-KR

The 10GBE interface of the multiplexer switches Broadwell-DE CPU uses 10G-KR to communicate with the MAC BCM56873 to support additional high speed datalink between CPU and MAC.

Figure 20 10GBase-KR Connection



3.11. BMC Module (Option)

The BMC (Baseboard management controller) is used for monitoring the system HW information including thermal, power, FAN and CPU status, even if the CPU is under sleeping mode.

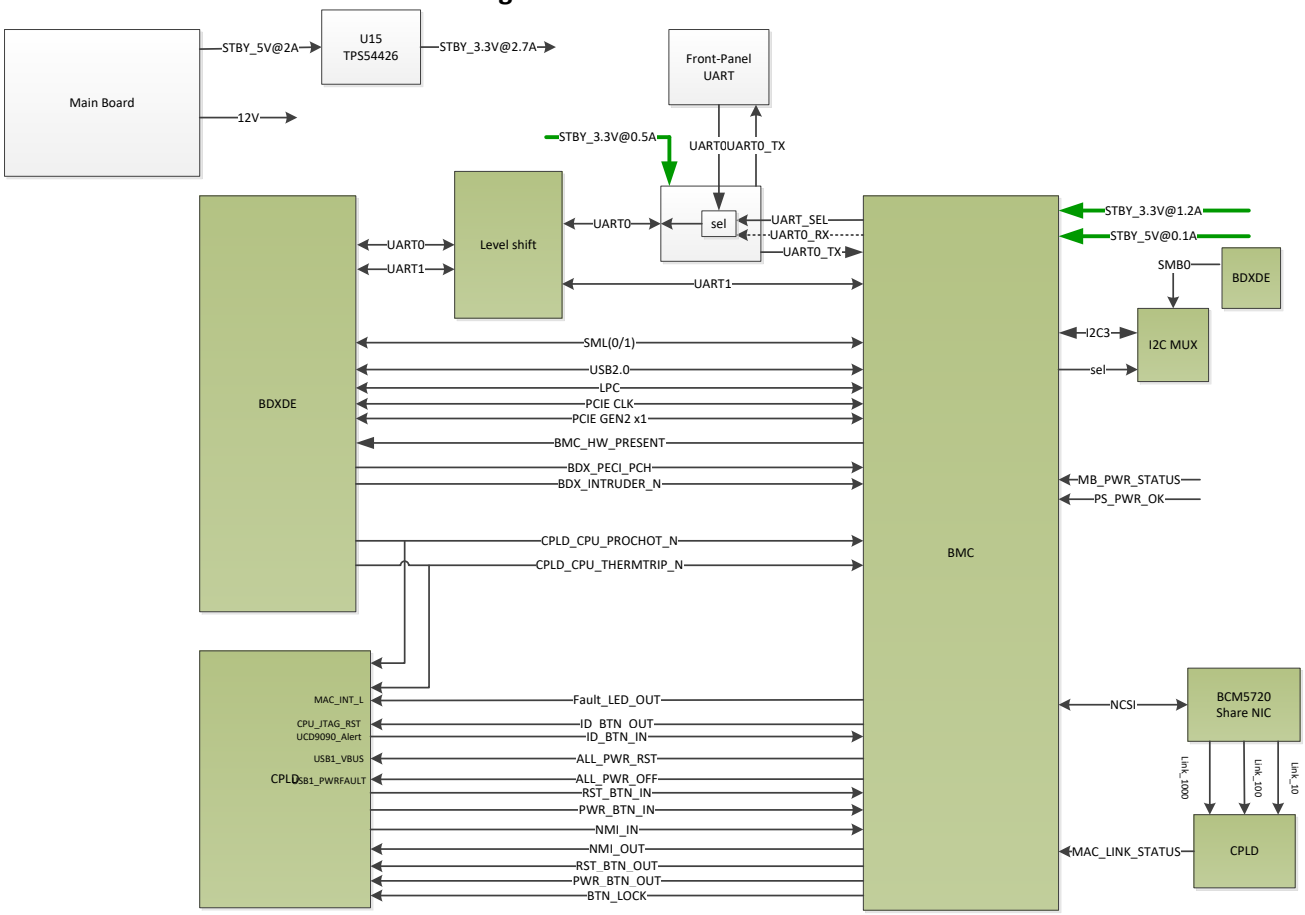
There are 2 kinds of BMC module solution, one is AST2400, the other is AST1250.

The difference between AST2400 and AST1250 is that only AST2400 has embedded graphic chip (VGA) and can support vKVM function.

The BMC module would be installed in CONN14 for corresponding SKU.

The following brief descriptions are for the interface between BMC module and CPU board in following sections

Figure 21 BMM connection



3.11.1. LPC

The LPC interface is the main communication channel for CPU to get the whole system information from BMC via IPMI protocol, like SMBUS.

BMC would also listen the information from CPU via LPC, such as port 80 status and serial messages for SOL function.

3.11.2. PCIE

The PCIe interface is used to achieve the vKVM function and only available when the AST2400 BMC module be installed.

3.11.3. SPI

The SPI interface of BMC module is used for upgrade the system bios on CPU board.

When BMC want to upgrade the system bios on CPU board, “BDX_SPI_MUX_SEL” would be driven by BMC from high to low.

3.11.4. SMBUS

In order to prevent the multi master hang-up issue, if BMC module is installed, the SMBUS host would change to BMC, not CPU.

When the BMC is installed, the “I2C_Multiplexer_select” would be driven to low to let BMC be the only host on SMBUS.

CPU would change to via LPC to get the SMBUS information from BMC.

3.11.5. UART

The UART interface is used to achieve SOL function.
CPU UART0 is connected to BMC uart1 block, and is used for SOL.
If BMC want to send UART message to CPU via UART0 of CPU, “BMC_UART0_DIR_SEL” would be driven to “0” from “1”.

Figure 22 UART connection

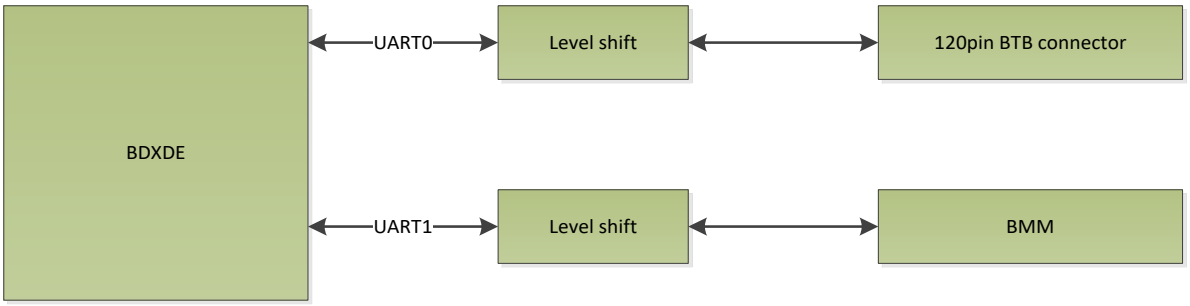


Table 11 CONN18 PIN ASSIGNMENT

Pin Number	Description
1	VCC
2	TX
3	RX
4	GND

3.11.6. USB

The USB interface is 2.0 and used for vMEDIA function defined by IPMI.

3.11.7. GPIO

The BMC module achieves several functions via GPIO to control the whole chassis.
The following table shows the brief description for these functions.

Table 12 BMC GPIO Definition

Signal name	Function	pin	pin	Function	Signal name
CPLD_CPU_PROCHOT_N	CPU PROCHOT event indicator	29	30	UART0 RX is sent by front panel UART console or BMC module 1: from BMC 0: From CPU	BMC_UART0_DIR_SEL_R
CPLD_CPU_THERMTRIP_N	THERMTRIP event indication	31	32	BMC present 1: no BMC present 0: BMC present	BMC_HW_present

TPM_DET_N	TPM module detect	33	34	I2C mux select 1: host is CPU 0: host is BMC	I2C multipleixer select
BDX_PECI_PCH	PECI_CPU detect	35	36	CPLD interrupt to CPU	CPLD_interrupt
PS_PWROK	PS_PWROK signal from CPLD	37	38	All the power in the chassis would be reset when this pin is "0"	All_power_reset
BDX_INTRUDER_N	INTRUDER# function	39	40	All the power in the chassis would be off when this pin is "0"	All_power_off
ID_LED status sense	ID_LED status sense	41	56	BCM5720 link indicator	BCM5720_link_status
PWRGD_P3V3_A	MB power status sense	43	170	This pin is acted as BMC push the RST BTN. 1: nothing 0: active	RST_BTN_OUT_BMC_N
BDX_SPI_MUX_SEL	Controlled by BMC, select the SPI bus host is CPU or BMC 1: From CPU 0: From BMC	119	172	This pin is acted as BMC push the PWR BTN. 1: nothing 0: active	PWR_BTN_OUT_BMC_N
BMC_SPI_OUT_SEL	BMC select to CI flash or KGI flash 1: CI 0: KGI	141	174	This pin is acted as BMC generate the NMI to CPU. 1: nothing 0: active	NMI_BTN_OUT_BMC_N
RST_BTN_IN_BMC_N	When the RST BTN has been pushed, BMC need to know this action	169	176	This pin is acted as BMC want to light on the fault LED. 1: nothing 0: light on fault led	FAULT_LED_OUT_N
PWR_BTN_IN_BMC_N	When the RWR BTN has been pushed, BMC need to know this action	171	178	This pin is acted as BMC want to light on the ID LED. 1: nothing 0: active	ID_LED_BMC_N

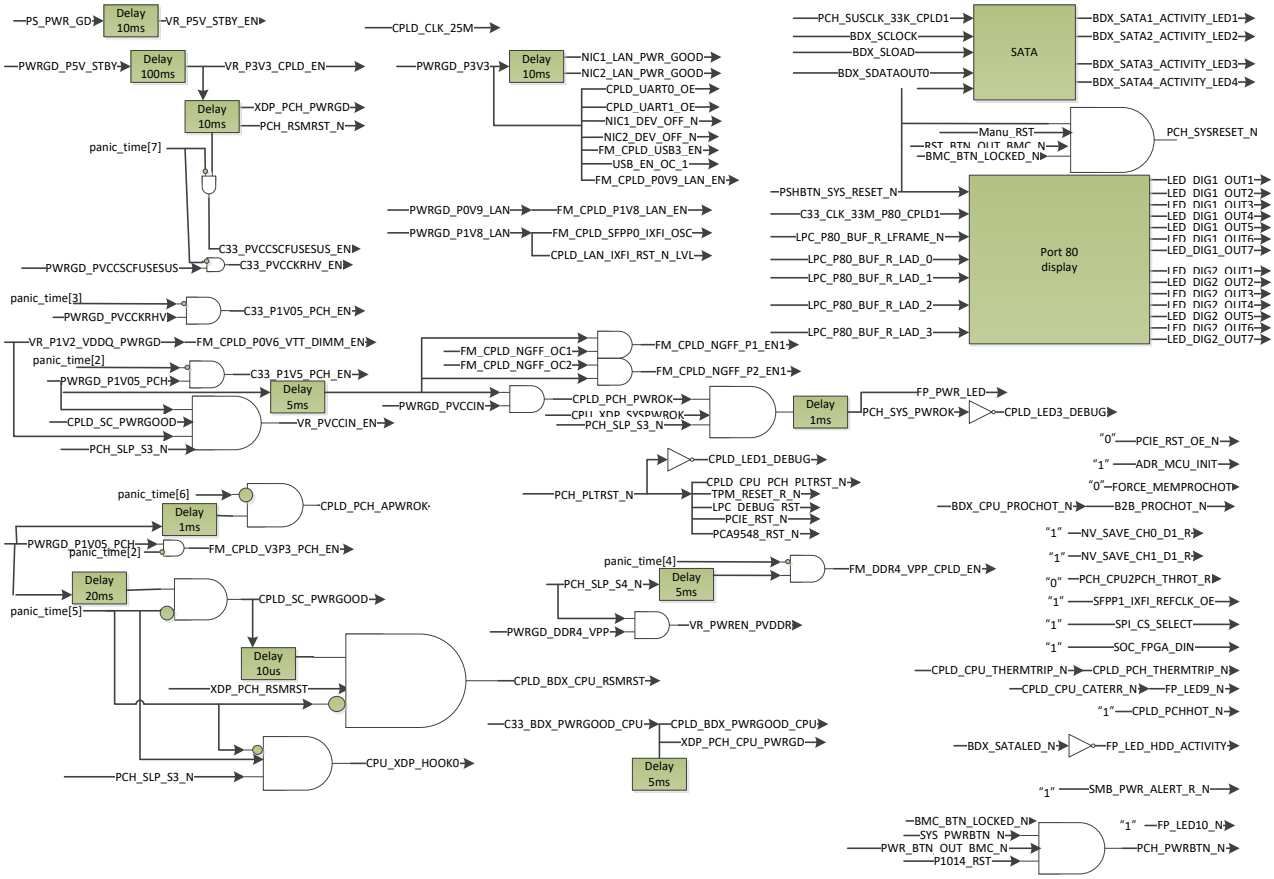
ID_BTN_BMC_N	When the ID BTN has been pushed, BMC need to know this action	173			
NMI_BTN_IN_BMC_N	When the NMI event has been sent to CPU, BMC need to know this event	175			

3.12. CPLD (For CPU Board)

The aim of the CPLD on the BDXDE CPU Board in the AS7326-56x chassis is major for power sequence, reset system, system interrupt, and BMC module function support. The I2C address info of the CPLD is 0x65.

The CPLD has registers to record the board status, including error function , power status , interrupt event , thermal event from CPU , and also the board ID and CPLD version.

Figure 23 CPLD block diagram



3.13. CPLD Architecture (For CPU Board)

3.13.1. Power Sequence

The most important function of the CPLD is to control the whole board power sequence based on the power sequence requirement of Intel Broadwell-DE.
CPLD would base on the power good signals from the VRs on the board and then drives the enable signals to enable the VRs.
The “PWROK” signals are used to indicate PCH and PCU of BDXDE that the related power are ok.

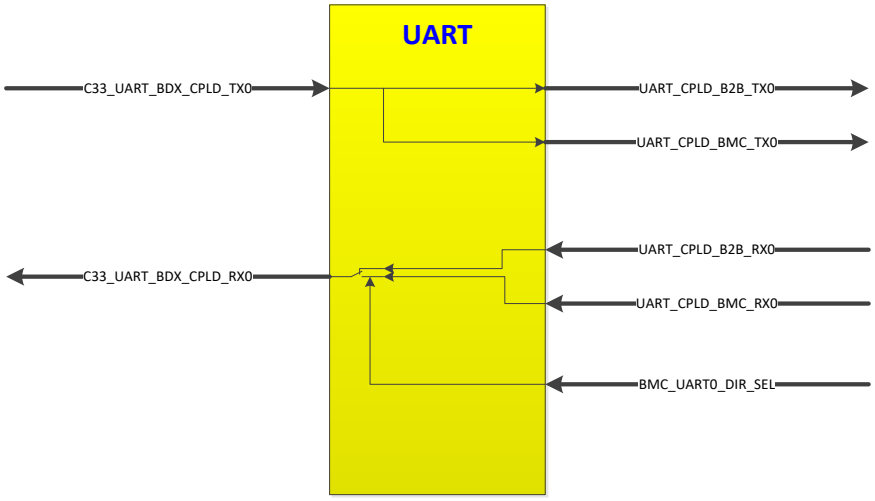
3.13.2. Reset

There are three reset sources in the ES7654NT chassis: one is from BMC module as “BMC_RST_BTN”, one is from MB as “MANU_RST”, the other one is from reset bottom on the board.
When the three reset signals have been triggered, CPLD would announce the BDXDE CPU by “PCH_SYSRESET_N” and let BDXDE PCU drive “PCH_PLTRST_N” to low to reset whole chassis.
Also, when the “BMC_PWR_BTN” is been driven from BMC or the the “SYS_PWRBTN_N” is been driven by power button, the chassis would enter the sleep mode until the event has been triggered again.
The “PCH_RSMRST_N” is used for power up sequence.

3.13.3. UART

The UART block is used to control the system UART message that would go to front panel console port or connect to BMC.
When BMC_UART0_DIR_SEL is driven high, that allowed BMC to send UART message to CPU.

Figure 24 UART Overview



3.13.4. BMC

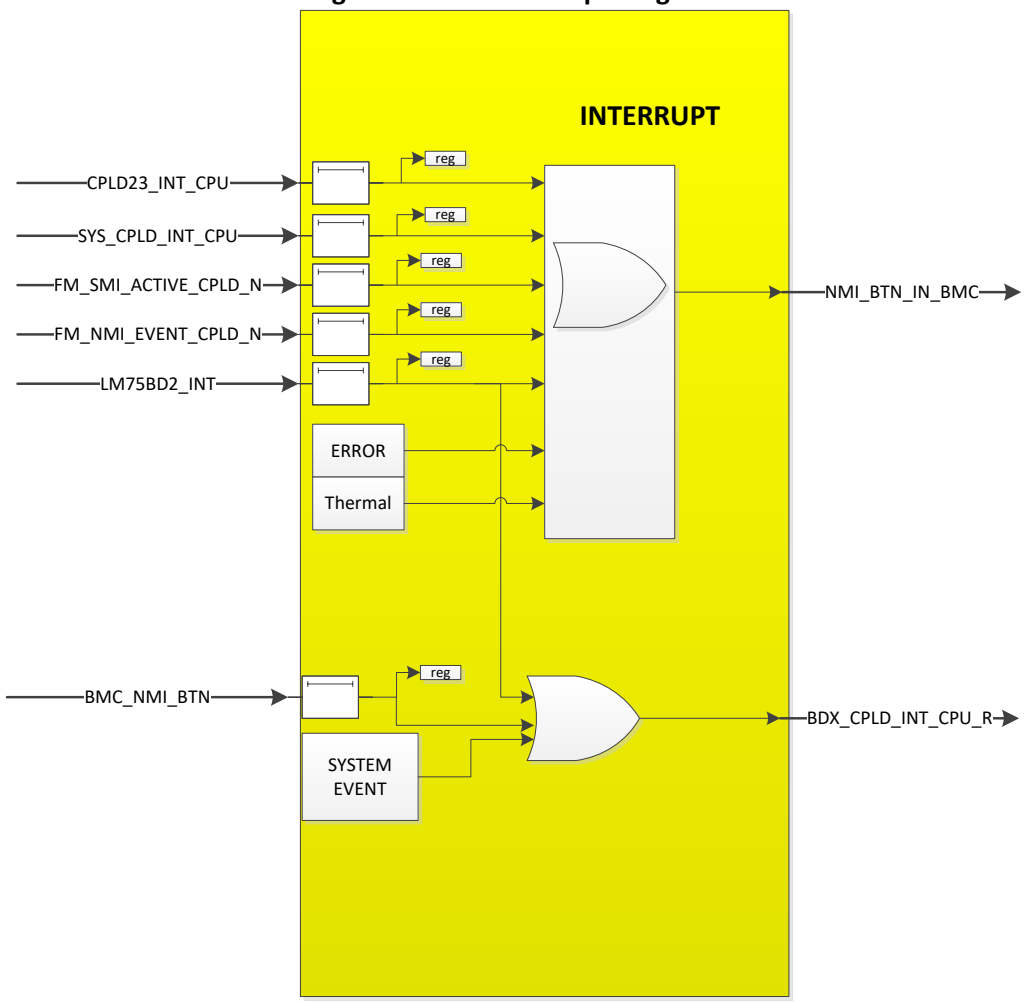
The main function of the BMC block in CPLD is used to receive and response the BMC control function for all the system.

"CPU_JTAG_RST" is used to announce MB that BMC want to light the ID led.
"MAC_INT_L" is used to announce MB that BMC want to light off the DIAG led.
"USB1_VBUS" is used for the "power on reset" request from BMC.
"USB1_PWRFAULT" is used for the "all power off" request from BMC
"USD9090_ALERT_L" is the announcement from MB that the front panel ID button has been pushed. The CPLD has to announce BMC by "BMC_ID_BTN".

3.13.5. Interrupt

The interrupt block in CPLD is used to record the interrupt event that came from CPU and MB then announce the interrupt event to BMC.
Also, when the BMC announces the interrupt event by "BMC_NMI_BTN" or some system events, CPLD would announced CPU by "BDX_CPLD_INT_CPU".

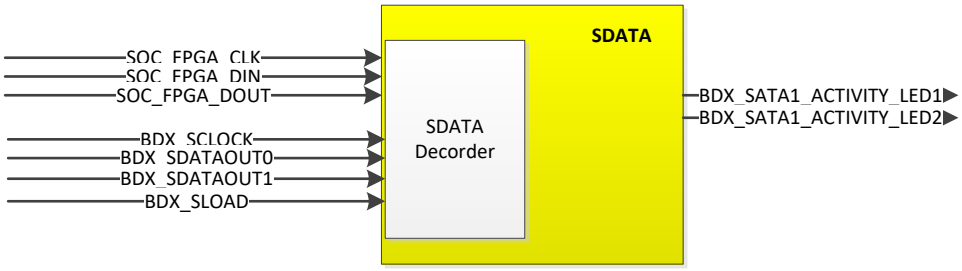
Figure 25 CPLD Interrupt Diagram



3.13.6. SDATA

The SDATA block is used to light the SATA led when the CPU is read/write SATA disk.

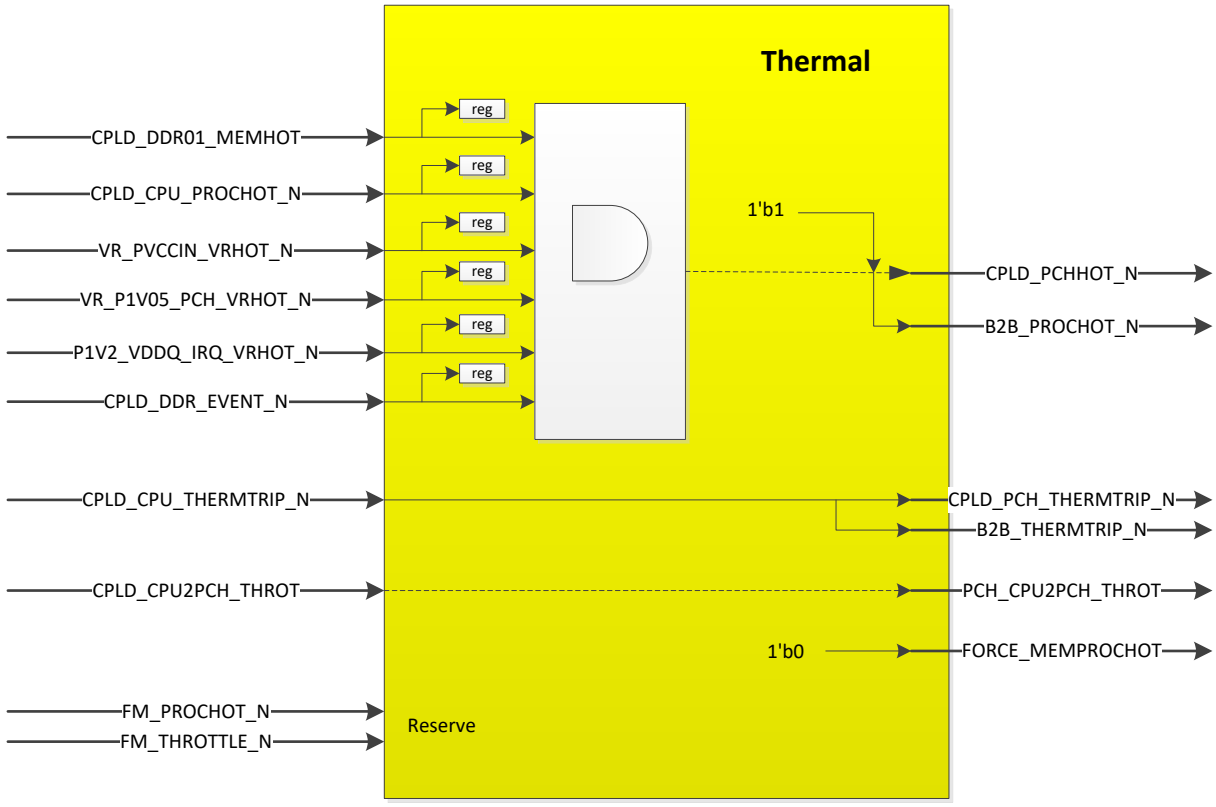
Figure 26 CPLD SDATA Diagram



3.13.7. Thermal

The thermal block is used to monitor the thermal event driven from CPU by "CPLD_CPU_PROCHOT_N" / "CPLD_DDR01_MEMHOT", "VR_PVCCIN_VRHOT_N" / " VR_P1V05_PCH_VRHOT_N" / " P1V2_VDDQ_IRQ_VRHOT_N" from VRs, and "CPLD_DDR_EVENT_N" from DDR memory, then use "CPLD_PCHHOT_N" and "B2B_PROCHOT_N" to announce PCH and MB. "CPLD_CPU_THERMTRIP_N" is driven from CPU to indicate THERMTRIP event then use "CPLD_PCH_THERMTRIP_N" and "B2B_THERMTRIP_N" to announce PCH and MB

Figure 27 CPLD Thermal Diagram



3.14. LED

There are several LEDs on the CPU board to indicate the system status.

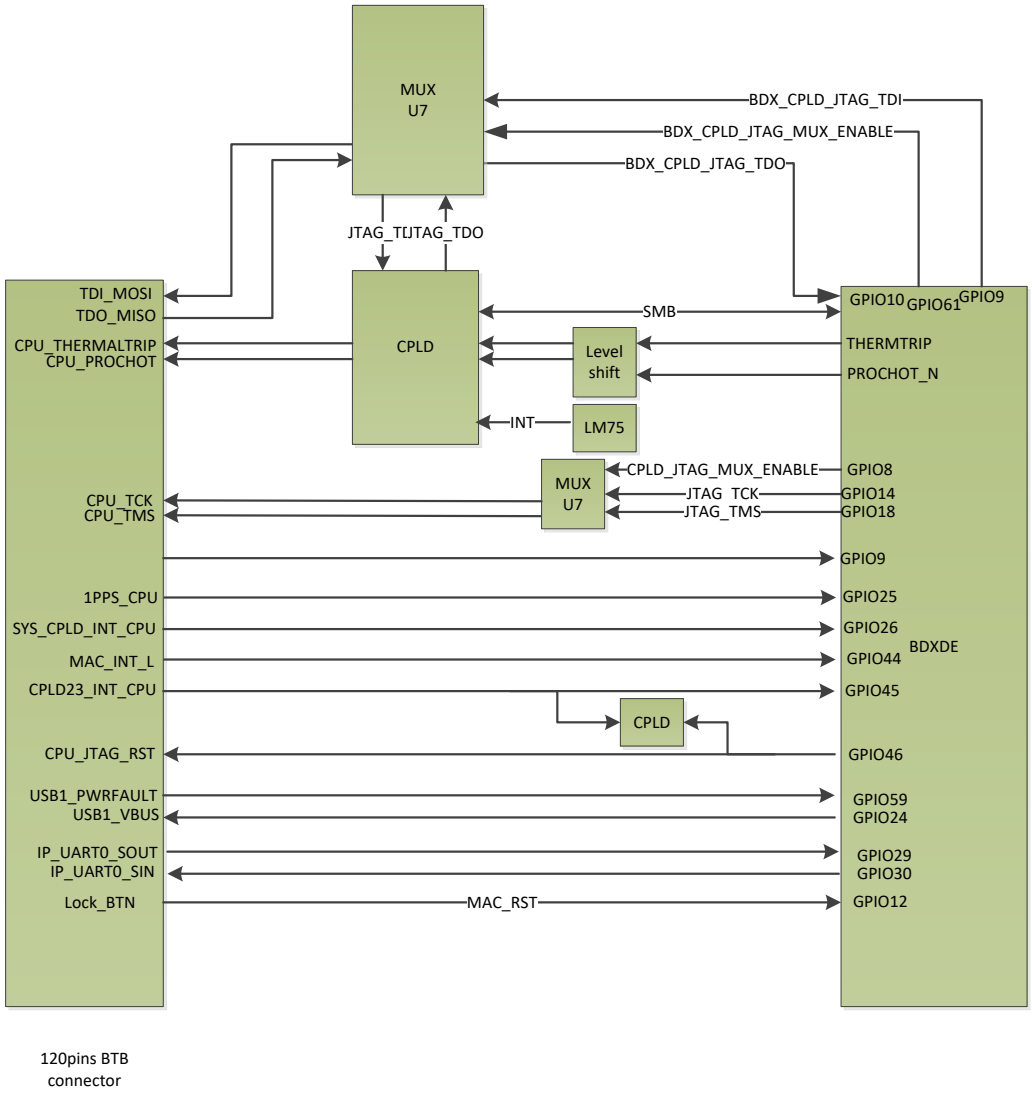
Table 13 LED Table

LED Name	Function
LED1	P3V3 power LED Color: Red Light: P3V3 power fail OFF: P3V3 power ok
LED2	P1V7 (VCCSCFUSESUS) power LED Color: Red Light: P1V7 power fail OFF: P1V7 power ok
LED3	P1V3 (VCCKRHV) power LED Color: Red Light: P1V3 power fail OFF: P1V3 power ok
LED4	P1V05 power LED Color: Red Light: P1V05 power fail OFF: P1V05 power ok
LED5	P2V5(DDR4_VPP) power LED Color: Red Light: P2V5 power fail OFF: P2V5 power ok
LED6	P1V2 (DDR4_VDDQ) power LED Color: Red Light: P1V2 power fail OFF: P1V2 power ok
LED7	P0V6 (DDR4_VTT) power LED, red Color: Red Light: P0V6 power fail OFF: P0V6 power ok
LED8	P1V5 (P1V5_PCH) power LED Color: Red Light: P1V5 power fail OFF: P1V5 power ok
LED9	P1V8 (VCCIN) power LED Color: Red Light: P1V8 power fail OFF: P1V8 power ok
LED10	P5V power LED Color: Red Light: P5V0 power fail OFF: P5V0 power ok
LED11	System LED Color: Green

	Light: System ok OFF: System fail
LED13	mSATA LED Color: Green Bright: SATA DATA transmission OFF: no mSATA data transmission
LED14	M.2 LED Color: Green Bright: M.2 DATA transmission OFF: no M.2 data transmission
LED15	No function.
LED17	PCH_SYS_PWROK LED Color: Green Light: pch system power ok OFF: pch system power fail
LED18	MAC link LED Color: Green Light: MAC link up OFF: MAC link down
LED19	System State LED Color: Bi, O , R O: System in S5 state R: System in G3 state OFF: System in S0 state

3.15. GPIO

Figure 28 GPIO function



The following table is the GPIO function description of BDXDE CPU.

Table 14 GPIO Table

Pin name	GPIO_USE_SEL 1: GPIO 0: Native	GPIO_IO_SEL 1: input 0: output	function

GPIO0	0	X	BMBUSY#
GPIO1	1	0	NC
GPIO2	0	X	NC
GPIO3	0	X	NC
GPIO4	1	1	CPU to PCH Throttle event interrupt
GPIO5	0	X	NC
GPIO6	1	0	JTAG enable, enable JTAG multiplexer to update CPLD code from CPU. 1: enable the JTAG multiplexer 0: disable the JTAG multiplexer
GPIO7	0	X	NC
GPIO8	1	0	JTAG Multiplexer select, which select the JTAG signals from CPU would go to CPLD or main board 1: to CPLD (default) 0: to Main board
GPIO9	1	0	XDP_NOA5_PCH/ BDX_CPLD_JTAG_TDI When configure to be BDX_CPLD_JTAG_TDI, which is CPU JTAG output
GPIO10	1	1	XDP_NOA6_PCH/ BDX_CPLD_JTAG_TDO When this pin configure to BDX_CPLD_JTAG_TDO , which is CPU JTAG input
GPIO11	0	X	SMBALERT#
GPIO12	1	0	Reset MAC, to do the sleep function.
GPIO14	1	0	XDP_NOA7_PCH/ BDX_CPLD_JTAG_TCK
GPIO15	1	0	SOC_FPGA_CLK
GPIO16	1	0	FM_THROTTLE_PCH_N/

			FM_THROTTLE_N
GPIO17	1	1	BMC present detect
GPIO18	1	0	XDP_NOA14_PCH/ BDX_CPLD_JTAG_TMS
GPIO19	1	BI-DIR	XDP_NOA9_PCH
GPIO20	1	0	FM_SMI_ACTIVE_PCH_N/ FM_SMI_ACTIVE_CPLD_N
GPIO21	1	BI-DIR	XDP_NOA8_PCH
GPIO22	1	0	SCLOCK
GPIO23	0	X	NC
GPIO24	0	0	NC
GPIO25	1	1	1PPS_CPU (no use)
GPIO26	1	1	SYS_CPLD_INT_CPU
GPIO27	1	1	SOC_FPGA_DIN
GPIO28	1	0	SOC_FPGA_DOUT
GPIO29	1	0	IP_UART0_SOUT(no use)
GPIO30	1	1	IP_UART0_SIN(no use)
GPIO31	1	1	SMB_PWR_ALERT
GPIO32	X	X	NC
GPIO33	X	X	NC
GPIO35	1	0	FM_NMI_EVENT_PCH_N/ FM_NMI_EVENT_CPLD_N
GPIO36	1	0	ADR_STATUS_RD
GPIO37	1	1	ADR_STATUS_CLR
GPIO38	0	0	SLOAD
GPIO39	0	0	SDATAOUT0
GPIO40	0	BI	XDP_NOA1_PCH
GPIO41	1	0	XDP_NOA2_PCH/ CPLD_CONFIG_CLK
GPIO42	1	BI	XDP_NOA3_PCH/ CPLD_CONFIG_DATA
GPIO43	1	0	XDP_NOA4_PCH / ADR_MCU_INIT

GPIO44	0	1	NC
GPIO45	1	1	CPLD23_INT_CPU
GPIO46	1	0	CPU_JTAG_RST(no use)
GPIO48	1	0	SDATAOUT1
GPIO49	1	0	FM_CPU_PROCHOT_PCH_N/ FM_PROCHOT_N
GPIO50	X	X	NC
GPIO51	1	1	4.7k pull to 3.3V
GPIO52	1	1	CPU_SV
GPIO53	1	1	1k pull to gnd
GPIO54	X	X	NC
GPIO55	1	1	FM_BIOS_RCRV_BOOT_N
GPIO57	1	1	FM_ME_RCRV_N
GPIO58	0	X	SML1_CLK
GPIO59	1	BI	XDP_NOA0_PCH
GPIO60	0	X	SML0ALERT#
GPIO61	X	X	NC
GPIO62	0	X	SUSCLK_33K
GPIO65	0	X	NC
GPIO67	0	X	NC
GPIO68	1	1	CPLD interrupt
GPIO69	0	X	NC
GPIO70	0	X	NC
GPIO71	0	X	NC
GPIO72	1	1	1K pull to 3.3V
GPIO74	0	X	SML1ALERT#/TEMP_ALERT#.
GPIO75	0	X	SML1DATA

4. Sub-system of MAC (BCM56873)

The BCM56873 incorporates 20 FalconCore, where 12 FalconCore can operate at 25Gbps and 8 FalconCore can operate at 40G/ 100Gbps.The PCIe interfaces the high bandwidth to transfer any packet to or from CPU. The PCI interface is configured at PCIe Gen2. It is to directly connect to CPU, and the bandwidth can be reached PCI2 Gen2 4 lanes.

4.1. Configurations of MAC (BCM56873)

Table 15 MAC Configurations Table

Pin Number	Pin Name	Function Description
BG24 A40 A41	BOOT_DEV[2:0]	Selects the boot flow for mHost0 (the first internal ARM R5): 3'b000: Load all necessary code from QSPI flash attached to IP_QSPI interface and begin execution. (others): Reserved **Note:** These signals have no effect if MHOST0_BOOT_DEV is pulled low
BF25 BF26	IP_BSC2_SA[1:0]	Selects the lower two bits of the BSC slave address used on the BSC2 interface.
BG22	IP_QSPI_4BYTE_ADDR	Selects the operating mode of the QSPI flash device connected to the IP_QSPI interface: 1'b0= QSPI flash is operating in 3 byte address mode 1'b1= QSPI flash is operating in 4 byte address mode
BF23	IP_QSPI_ADDR_BPC_MODE	Selects the mode that is used for sending commands and addresses to the QSPI flash device connected to the IP_QSPI interface: 1'b0: Commands and addresses are sent serially, data is sent in parallel 1'b1: Commands, addresses, and data are sent in parallel
BB23	IP_QSPI_DUAL_LANE	Selects the IP_QSPI interface's operating mode: 1'b0: IP_QSPI interface operates using a serial interface 1'b1: IP_QSPI interface operates using a two bit parallel interface **Note:** If this signal is pulled high, the IP_QSPI_QUAD_LANE signal must be pulled low
BD23	IP_QSPI_QUAD_LANE	Selects the IP_QSPI interface's operating mode: 1'b0: IP_QSPI interface operates using a serial interface 1'b1: IP_QSPI interface operates using a four bit parallel interface **Note:** If this signal is pulled high, the IP_QSPI_DUAL_LANE signal must be pulled low
BE24	MHOST0_BOOT_DEV	Selects the way that mHost0 (the first internal ARM R5) is brought out of reset: 1'b0: mHost0 is held in reset 1'b1: mHost0 comes out of reset and begins executing code

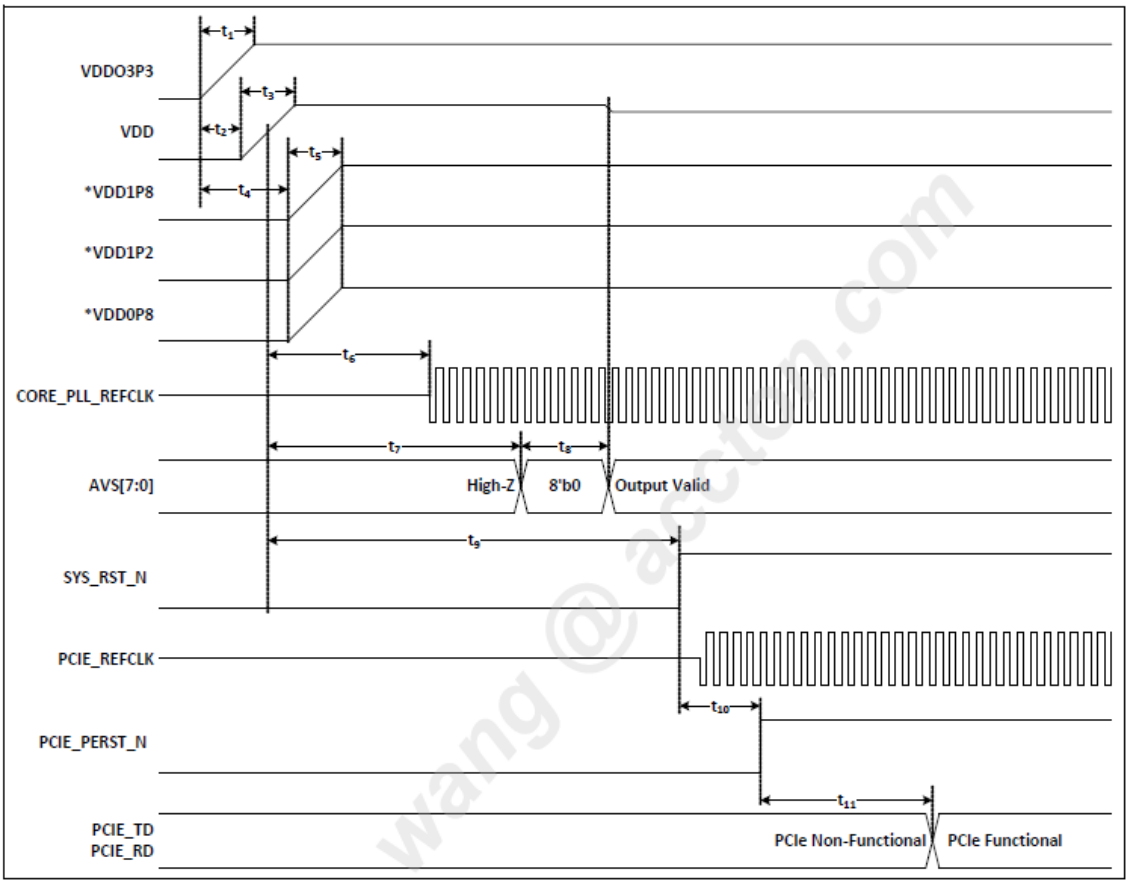
		based on the setting of the BOOT_DEV[2:0] strap signals
BA24 BB24	PCIE_FORCE_GENTYPE[1:0]	Selects the maximum operating rate of the PCI Express interface: 2'b00: Interface can operate at PCI Express Gen1, Gen2, or Gen3 speeds 2'b01: Interface can operate at PCI Express Gen1 speed 2'b10: Interface can operate at PCI Express Gen1, Gen2 speeds (others): Reserved Note: When the PCI Express interface is configured to support Gen3 speeds, it is a requirement that the MHOST0_BOOT_DEV strap signal is pulled high, the BOOT_DEV[2:0] signals are all pulled low, and a QSPI flash memory is connected to the IP_QSPI interface and contains the PCIe Gen3 microcode.
BC24 BD24	PCIE_FORCE_LANE[1:0]	Selects the maximum link width of the PCI Express interface: 2'b00: Interface can operate at x1, x2, or x4 link widths 2'b01: Interface can operate at x1 link width only 2'b10: Interface can operate at x1 or x2 link widths (others): Reserved

4.2. POR of MAC (BCM56873)

The detailed power-on reset (POR) flow is as follows:

1. The recommend power-up voltage sequence is from highest 3.3V to VDD1V0_ROV and 0.8V, 1.2V, 1.8V can ramp up until VDD1V0_ROV reaches 0.55V.
2. 3.3V : ramp up time min = 660us , max = 10ms.
3. VDD1V0_ROV : ramp up time min = 50us , max = 10ms.
4. 0.8V, 1.2V, 1.8V : ramp up time min = 100us , max = 10ms.
5. Minimum system reset de-asserted time is 80ms.

Figure 29 MAC Power-on Sequence



4.3. Port Mapping

Figure 30 Physical Port mapping

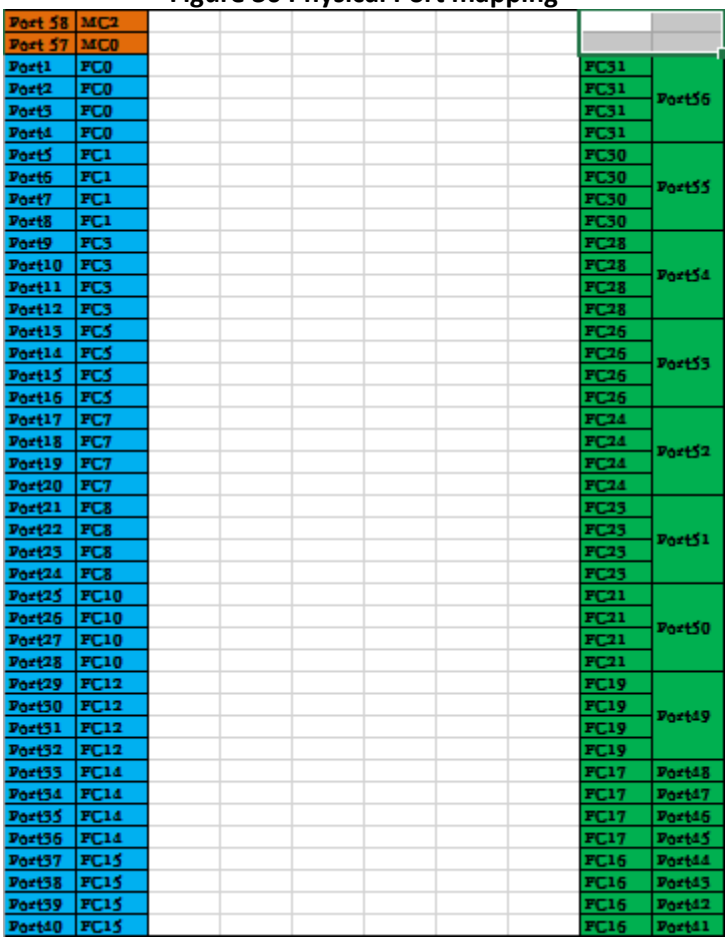


Table 16 MAC Mapping Table

FalconCore	Mac(BCM56873)		SFP28 Connector Location	Connector		Port Number (front-end)
	TX polarity (TD)	RX polarity (RD)		TX polarity	RX polarity	
FC0	FC0_TD2[P/N]	FC0_RD2[P/N]	CONN20A	TD[+/-]#1T	RD[+/-]#1T	Port1
	FC0_TD1[P/N]	FC0_RD3[P/N]	CONN20A	TD[+/-]#1L	RD[+/-]#1L	Port2
	FC0_TD3[P/N]	FC0_RD1[P/N]	U68	T_TD[+/-]	T_RD[+/-]	Port3
FC1	FC1_TD3[N/P]	FC1_RD3[P/N]	CONN20B	TD[+/-]#2T	RD[+/-]#2T	Port4
FC1	FC1_TD2[N/P]	FC1_RD2[N/P]	CONN20B	TD[+/-]#2L	RD[+/-]#2L	Port5
FC0	FC0_TD0[N/P]	FC0_RD0[P/N]	U69	T_TD[+/-]	T_RD[+/-]	Port6

FC1	FC1_TD0[N/P]	FC1_RD0[P/N]	CONN21A	TD[+/-]#1T	RD[+/-]#1T	Port7
FC3	FC3_TD3[N/P]	FC3_RD3[N/P]	CONN21A	TD[+/-]#1L	RD[+/-]#1L	Port8
FC1	FC1_TD1[P/N]	FC1_RD1[P/N]	U70	T_TD[+/-]	T_RD[+/-]	Port9
FC3	FC3_TD1[P/N]	FC3_RD1[N/P]	CONN21B	TD[+/-]#2T	RD[+/-]#2T	Port10
	FC3_TD0[P/N]	FC3_RD2[N/P]	CONN21B	TD[+/-]#2L	RD[+/-]#2L	Port11
	FC3_TD2[P/N]	FC3_RD0[N/P]	U71	T_TD[+/-]	T_RD[+/-]	Port12
FC5	FC5_TD2[N/P]	FC5_RD2[P/N]	CONN22A	TD[+/-]#1T	RD[+/-]#1T	Port13
	FC5_TD1[N/P]	FC5_RD3[P/N]	CONN22A	TD[+/-]#1L	RD[+/-]#1L	Port14
	FC5_TD3[N/P]	FC5_RD1[P/N]	U72	T_TD[+/-]	T_RD[+/-]	Port15
FC7	FC7_TD3[P/N]	FC7_RD3[P/N]	CONN22B	TD[+/-]#2T	RD[+/-]#2T	Port16
	FC7_TD2[P/N]	FC7_RD2[N/P]	CONN22B	TD[+/-]#2L	RD[+/-]#2L	Port17
FC5	FC5_TD0[P/N]	FC5_RD0[P/N]	U73	T_TD[+/-]	T_RD[+/-]	Port18
FC7	FC7_TD0[N/P]	FC7_RD0[N/P]	CONN23A	TD[+/-]#1T	RD[+/-]#1T	Port19
FC8	FC8_TD3[N/P]	FC8_RD3[N/P]	CONN23A	TD[+/-]#1L	RD[+/-]#1L	Port20
FC7	FC7_TD1[N/P]	FC7_RD1[P/N]	U74	T_TD[+/-]	T_RD[+/-]	Port21
FC8	FC8_TD1[P/N]	FC8_RD1[P/N]	CONN23B	TD[+/-]#2T	RD[+/-]#2T	Port22
	FC8_TD0[P/N]	FC8_RD2[N/P]	CONN23B	TD[+/-]#2L	RD[+/-]#2L	Port23
	FC8_TD2[P/N]	FC8_RD0[N/P]	U75	T_TD[+/-]	T_RD[+/-]	Port24
FC10	FC10_TD2[N/P]	FC10_RD2[P/N]	CONN24A	TD[+/-]#1T	RD[+/-]#1T	Port25
	FC10_TD1[N/P]	FC10_RD3[P/N]	CONN24A	TD[+/-]#1L	RD[+/-]#1L	Port26
	FC10_TD3[N/P]	FC10_RD1[P/N]	U76	T_TD[+/-]	T_RD[+/-]	Port27
FC12	FC12_TD3[P/N]	FC12_RD3[N/P]	CONN24B	TD[+/-]#2T	RD[+/-]#2T	Port28
	FC12_TD2[P/N]	FC12_RD2[N/P]	CONN24B	TD[+/-]#2L	RD[+/-]#2L	Port29
FC10	FC10_TD0[P/N]	FC10_RD0[N/P]	U77	T_TD[+/-]	T_RD[+/-]	Port30
FC12	FC12_TD0[N/P]	FC12_RD0[P/N]	CONN25A	TD[+/-]#1T	RD[+/-]#1T	Port31
FC14	FC14_TD3[N/P]	FC14_RD3[P/N]	CONN25A	TD[+/-]#1L	RD[+/-]#1L	Port32
FC12	FC12_TD1[N/P]	FC12_RD1[P/N]	U78	T_TD[+/-]	T_RD[+/-]	Port33
FC14	FC14_TD1[P/N]	FC14_RD1[N/P]	CONN25B	TD[+/-]#2T	RD[+/-]#2T	Port34
	FC14_TD0[P/N]	FC14_RD2[N/P]	CONN25B	TD[+/-]#2L	RD[+/-]#2L	Port35
	FC14_TD2[P/N]	FC14_RD0[N/P]	U79	T_TD[+/-]	T_RD[+/-]	Port36
FC15	FC15_TD1[P/N]	FC15_RD1[P/N]	CONN26A	TD[+/-]#1T	RD[+/-]#1T	Port37
	FC15_TD2[P/N]	FC15_RD3[N/P]	CONN26A	TD[+/-]#1L	RD[+/-]#1L	Port38
	FC15_TD3[N/P]	FC15_RD2[P/N]	U80	T_TD[+/-]	T_RD[+/-]	Port39
FC16	FC16_TD0[P/N]	FC16_RD0[P/N]	CONN26B	TD[+/-]#2T	RD[+/-]#2T	Port40
	FC16_TD1[P/N]	FC16_RD1[P/N]	CONN26B	TD[+/-]#2L	RD[+/-]#2L	Port41
FC15	FC15_TD0[P/N]	FC15_RD0[P/N]	U81	T_TD[+/-]	T_RD[+/-]	Port42

FC16	FC16_TD3[N/P]	FC16_RD3[N/P]	CONN27A	TD[+/-]#1T	RD[+/-]#1T	Port43
FC17	FC17_TD0[N/P]	FC17_RD0[N/P]	CONN27A	TD[+/-]#1L	RD[+/-]#1L	Port44
FC16	FC16_TD2[N/P]	FC16_RD2[P/N]	U82	T_TD[+/-]	T_RD[+/-]	Port45
FC17	FC17_TD2[P/N]	FC17_RD2[N/P]	CONN27B	TD[+/-]#2T	RD[+/-]#2T	Port46
	FC17_TD3[P/N]	FC17_RD1[N/P]	CONN27B	TD[+/-]#2L	RD[+/-]#2L	Port47
	FC17_TD1[P/N]	FC17_RD3[N/P]	U83	T_TD[+/-]	T_RD[+/-]	Port48

FalconCore	Mac(BCM56873)		QSFP28 Connector Location	Connector		Port Number (front-end)
	TX polarity (TD)	RX polarity (RD)		TX polarity	RX polarity	
FC19	FC19_TD3[P/N]	FC19_RD3[P/N]	CONN44	TX1_[P/N]	RX1_[P/N]	Port49
	FC19_TD2[P/N]	FC19_RD2[P/N]		TX2_[P/N]	RX2_[P/N]	
	FC19_TD1[P/N]	FC19_RD1[P/N]		TX3_[P/N]	RX3_[P/N]	
	FC19_TD0[P/N]	FC19_RD0[P/N]		TX4_[P/N]	RX4_[P/N]	
FC21	FC21_TD0[P/N]	FC21_RD0[P/N]	CONN45	TX1_[P/N]	RX1_[P/N]	Port50
	FC21_TD1[P/N]	FC21_RD1[P/N]		TX2_[P/N]	RX2_[P/N]	
	FC21_TD2[P/N]	FC21_RD2[P/N]		TX3_[P/N]	RX3_[P/N]	
	FC21_TD3[P/N]	FC21_RD3[P/N]		TX4_[P/N]	RX4_[P/N]	
FC23	FC23_TD0[P/N]	FC23_RD0[P/N]	CONN46	TX1_[P/N]	RX1_[P/N]	Port51
	FC23_TD1[P/N]	FC23_RD1[P/N]		TX2_[P/N]	RX2_[P/N]	
	FC23_TD2[P/N]	FC23_RD2[P/N]		TX3_[P/N]	RX3_[P/N]	
	FC23_TD3[P/N]	FC23_RD3[P/N]		TX4_[P/N]	RX4_[P/N]	
FC24	FC24_TD0[P/N]	FC24_RD0[P/N]	CONN47	TX1_[P/N]	RX1_[P/N]	Port52
	FC24_TD1[P/N]	FC24_RD1[P/N]		TX2_[P/N]	RX2_[P/N]	
	FC24_TD2[P/N]	FC24_RD2[P/N]		TX3_[P/N]	RX3_[P/N]	
	FC24_TD3[P/N]	FC24_RD3[P/N]		TX4_[P/N]	RX4_[P/N]	
FC26	FC26_TD3[P/N]	FC26_RD3[P/N]	CONN48	TX1_[P/N]	RX1_[P/N]	Port53
	FC26_TD2[P/N]	FC26_RD2[P/N]		TX2_[P/N]	RX2_[P/N]	
	FC26_TD1[P/N]	FC26_RD1[P/N]		TX3_[P/N]	RX3_[P/N]	
	FC26_TD0[P/N]	FC26_RD0[P/N]		TX4_[P/N]	RX4_[P/N]	
FC28	FC28_TD0[P/N]	FC28_RD0[P/N]	CONN49	TX1_[P/N]	RX1_[P/N]	Port54
	FC28_TD1[P/N]	FC28_RD1[P/N]		TX2_[P/N]	RX2_[P/N]	
	FC28_TD2[P/N]	FC28_RD2[P/N]		TX3_[P/N]	RX3_[P/N]	
	FC28_TD3[P/N]	FC28_RD3[P/N]		TX4_[P/N]	RX4_[P/N]	
FC30	FC30_TD0[P/N]	FC30_RD0[P/N]	CONN50	TX1_[P/N]	RX1_[P/N]	Port55
	FC30_TD1[P/N]	FC30_RD1[P/N]		TX2_[P/N]	RX2_[P/N]	
	FC30_TD2[P/N]	FC30_RD2[P/N]		TX3_[P/N]	RX3_[P/N]	

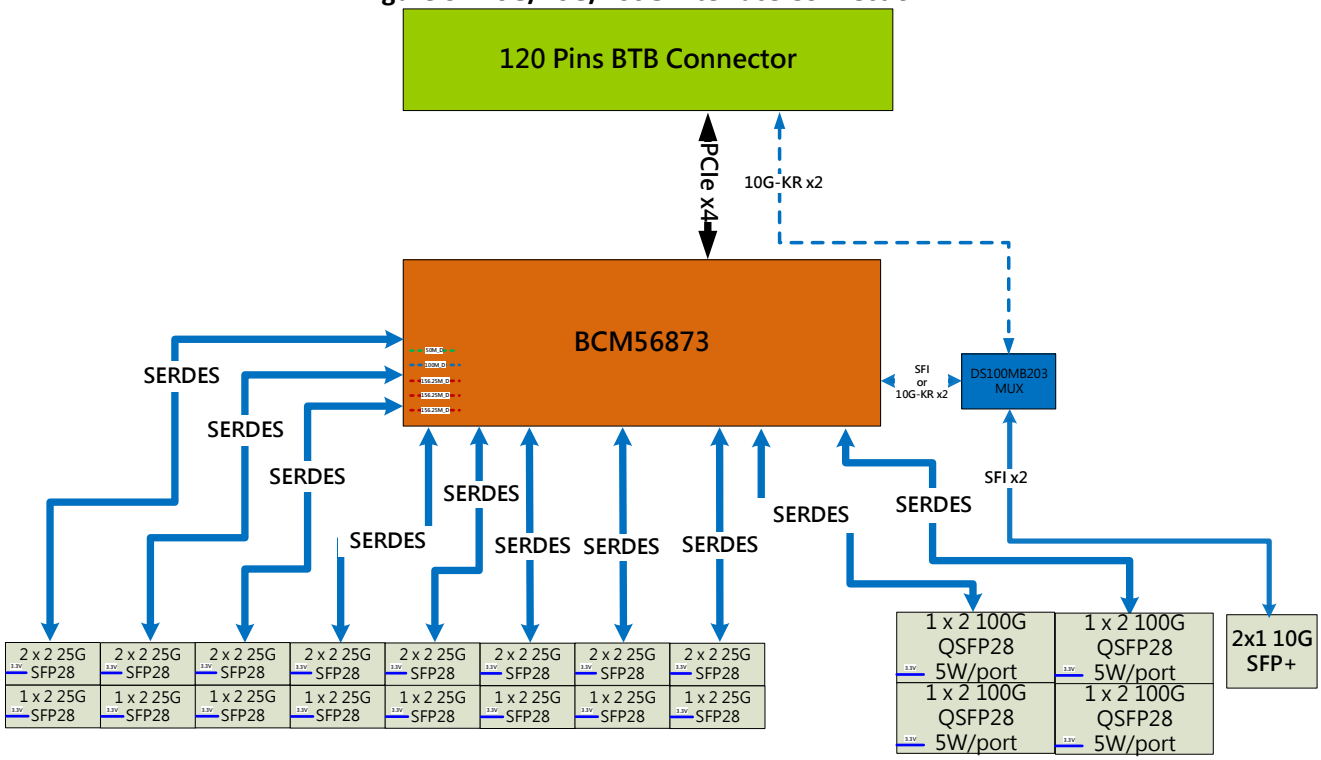
	FC30_TD3[P/N]	FC30_RD3[P/N]		TX4_[P/N]	RX4_[P/N]	
FC31	FC31_TD3[P/N]	FC31_RD3[P/N]	CONN51	TX1_[P/N]	RX1_[P/N]	Port56
	FC31_TD2[P/N]	FC31_RD2[P/N]		TX2_[P/N]	RX2_[P/N]	
	FC31_TD1[P/N]	FC31_RD1[P/N]		TX3_[P/N]	RX3_[P/N]	
	FC31_TD0[P/N]	FC31_RD0[P/N]		TX4_[P/N]	RX4_[P/N]	

FalconCore	Mac(BCM56873)		SFP+ Connector Location	Connector		Port Number (front-end)
	TX polarity (TD)	RX polarity (RD)		TX polarity	RX polarity	
MC0	MC_TD0[P/N]	MC_RD0[P/N]	CONN66	TD[+/-]#1T	RD[+/-]#1T	Port57
MC2	MC_TD2[P/N]	MC_RD2[P/N]		TD[+/-]#1L	RD[+/-]#1L	Port58

4.4. 10G/25G/40G/100G Interface

The AS7326-56x is phy-less system, BCM56873 connects with SFP28、QSFP28 and SFP+ directly and CPU control transceiver's I2C and status via CPLD.

Figure 31 10G/40G/100G Interface Connection



4.5. LED interface

The BCM56873's five separate LED interfaces: IP_LED_clk/data[4:0].

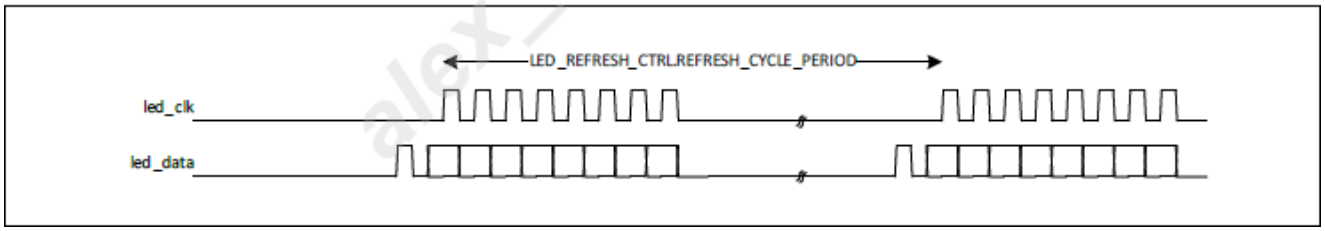
- IP_LED_clk/data0 provides port status for SFP28 ports 1-39.
- IP_LED_clk/data1 provides port status for SFP28 ports 40-48.
- IP_LED_clk/data1 provides port status for QSFP28 ports 49-56.
- IP_LED_clk/data1 provides port status for SFP+ ports 57-58.

Port status information includes link status, transmit and receive activity, and speed settings

The interface to the LED status indicators is implemented through a serial protocol carried out on two pins: LED_CLK and LED_DATA. If there are n LED status lights, it takes clock cycles to shift the data out of the LED interface. The shifted-out LED data is out-of-phase with respect to the LED_CLK. After all n bits have been shifted out, the LED_CLK and LED_DATA lines go idle until the next time the LED status is refreshed. An external shift register is responsible for holding the state of the LED status between scan (refresh) events.

Figure 32 LED bus

Figure 24: led_clk/led_data Refresh Interval



LED stream format:

There have four lanes per port. MAC will send lane[1:0] first, then send speed[1:0] and link-up/activity information per lane. A port will have 14 bits information. A LED bus is for 16 ports, so the total bits per led bus is 224 bits.

Table 17 LED stream format

Bit0	1	2	3	4	5	6	7	8	9	10	11	12	13
Lane[1:0]		Port A			Port B			Port C			Port D		
		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity

Speed [1:0] shows the lane speed. Lane[1:0] shows the lane number for a port. So the lane[1:0] and speed[1:0] shows the port configuration.
The bit of link-up/ Activity control the LED on/ off / toggle.

Table 18 LED Bit Description

Port configuration	Lane [1:0]	Speed [1:0]
100G	10	10
40G	10	00

10G	00	00
1G	00	11
4 x 25G	00	10
4 x 10G	00	00
2 x 50G	01	10

Link-up/ Activity	LED
1	ON
0	OFF
Toggle	Activity

Type	LED bit stream(b0 … b13)	SFP+	QSFP
OFF	00-000-000-000-000	off	off
1G	00-111-111-111-111	N/A(off)	N/A (off)
10G	00-001-001-001-001	Amber/Yellow	Purple
25G	00-101-101-101-101	Green	Amber/Yellow
40G	10-001-001-001-001	N/A(off)	Blue
100G	10-101-101-101-101	N/A(off)	Green
xxG	xx-xxx-xxx-xxx-xxx	N/A(off)	Green

If the lane[1:0] is “10”, the link-up/ activity bit of first lane will be active and other lanes will be inactive. If the lane[1:0] is “01”, the link-up/ activity bit of first and three lane will be active and other lanes will be inactive. If the lane[1:0] is ‘00”, the link-up/ activity bit of all lanes will be active.

4.6. QSFP28

The system has 8x QSFP28 ports can support 100Gbps(4x25Gbps or 2x50Gbps Fanout)/ 40Gbps(4x10Gbps Fanout). The QSFP28 port support optical transceiver and DAC. The power class can support up to 5W.

4.7. SFP28

The system has 48 x SFP28 ports can support 25Gbps/10Gbps/1Gbps. The SFP28 port support optical transceiver and DAC. The power class can support up to 2W.

4.8. SFP+

The system has 2 x SFP+ OOB ports can support 10Gbps/1Gbps. The SFP+ port support optical transceiver and DAC. The power class can support up to 1.5W.

5. Sub-system

5.1. Management PHY (BCM54616S)

The management port support 10/ 100/ 1000M Ethernet speed.

5.2. Configurations of MGMT PHY (BCM54616S)

Table 19 MGMT PHY Configurations Table

Pin Number	Pin Name	Function Description
G7 G6 H6 G10	LED1 LED2 LED3 LED4	LED1 High >> Copper AN enable LED2 High >> Full-duplex LED3 High >> LED4 High >> AN at 10/100/1000BASE-T
A8 B7	INTERF_SEL0 INTERF_SEL1	INTERF_SEL[1:0] 00 = RGMII-Copper (Copper mode) 01 = RGMII-Fiber (Fiber mode) *10 = SGMII-Copper (SGMII mode) 11 = Serdes-Copper (Media Converter mode)
H10 J0 J9 K10 K9	PHY_ADDR_0 PHY_ADDR_1 PHY_ADDR_2 PHY_ADDR_3 PHY_ADDR_4	ADDR = 111111

5.3. POR of MGMT PHY (BCM54616S)

The detailed power-on reset (POR) flow is as follows:

1. 3.3V up and Ref clock up
2. 3.3V enable MPS1484 to generate 2.5V
3. All powers are stable, POWR607 inform CPLD
4. CPLD receive the signal, CPLD assert Reset_N high

5.4. I2C

The CPU board has three I2C channels for our application. The Channel 1 used for Power Supply, Clock GEN, DC/DC, thermal sensor, CPLD2 and Fan CPLD. The channel 2 used for Power Supply, CPLD 1,3, USB HUB, DC/DC, Multiplexer, Retimer, port 49~56 QSFP28 and port 57~58 SFP+. The channel 2 used for port 1~48 SFP28.

Figure 33 Switch board I2C Connection

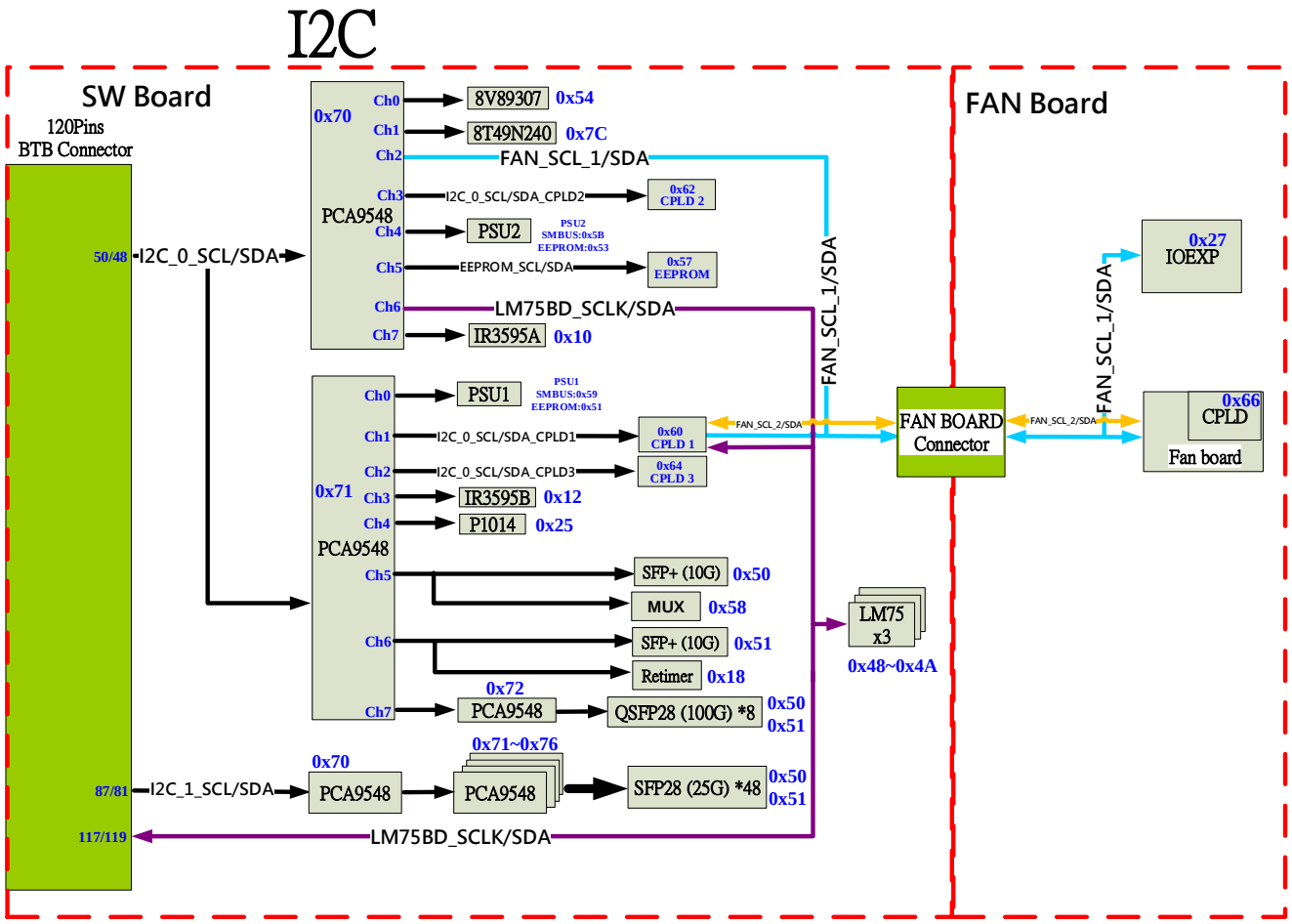


Table 20 Switch board I2C Address Table

	Channel	Device	Address
CPU	I2C 0	I2C switch (70)	0x70
		I2C switch (71)	0x71
	I2C 1	I2C switch (70)	0x70
I2C 0 I2C switch (70)	switch_CH0	8V89307	0x54
	switch_CH1	8T49N240	0x7C
	switch_CH2	FAN_CPLD	0x66
	switch_CH3	CPLD2	0x62
	switch_CH4	PSU2	SMBUS:0x5B EEPROM:0x53
	switch_CH5	EEPROM (Reserved)	0x57
	switch_CH6	LM75BD *3 LM75BD_CPU	0x48,0x49,0x4A

			4B
	switch_CH7	IR3595A	0x10
I2C 0 I2C switch (71)	switch_CH0	PSU1	SMBUS:0x59 EEPROM:0x51
	switch_CH1	CPLD1	0x60
	switch_CH2	CPLD3	0x64
	switch_CH3	IR3595B	0x12
	switch_CH4	P1014	0x25
	switch_CH5	SFP+ MUX	SFP+:0x50 MUX:0x58
	switch_CH6	SFP+ Retimer	SFP+:0x51 Retimer:0x18
	switch_CH7	I2C switch (72)	0x72
I2C 0 I2C switch (72)	switch_CH0	QSFP28 PORT 49	0x50, 0x51
	switch_CH1	QSFP28 PORT 50	0x50, 0x51
	switch_CH2	QSFP28 PORT 51	0x50, 0x51
	switch_CH3	QSFP28 PORT 52	0x50, 0x51
	switch_CH4	QSFP28 PORT 53	0x50, 0x51
	switch_CH5	QSFP28 PORT 54	0x50, 0x51
	switch_CH6	QSFP28 PORT 55	0x50, 0x51
	switch_CH7	QSFP28 PORT 56	0x50, 0x51
I2C 1 I2C switch (70)	switch_CH0	I2C switch (71)	0x71
	switch_CH1	I2C switch (72)	0x72
	switch_CH2	I2C switch (73)	0x73
	switch_CH3	I2C switch (74)	0x74
	switch_CH4	I2C switch (75)	0x75
	switch_CH5	I2C switch (76)	0x76
	switch_CH6	N/A	N/A
	switch_CH7	N/A	N/A
I2C 1 I2C switch (71)	switch_CH0	SFP28 PORT 2	0x50, 0x51
	switch_CH1	SFP28 PORT 1	0x50, 0x51
	switch_CH2	SFP28 PORT 4	0x50, 0x51
	switch_CH3	SFP28 PORT 3	0x50, 0x51
	switch_CH4	SFP28 PORT 6	0x50, 0x51

	switch_CH5	SFP28 PORT 7	0x50, 0x51
	switch_CH6	SFP28 PORT 5	0x50, 0x51
	switch_CH7	SFP28 PORT 9	0x50, 0x51
I2C 1 I2C switch (72)	switch_CH0	SFP28 PORT 10	0x50, 0x51
	switch_CH1	SFP28 PORT 8	0x50, 0x51
	switch_CH2	SFP28 PORT 12	0x50, 0x51
	switch_CH3	SFP28 PORT 11	0x50, 0x51
	switch_CH4	SFP28 PORT 13	0x50, 0x51
	switch_CH5	SFP28 PORT 16	0x50, 0x51
	switch_CH6	SFP28 PORT 15	0x50, 0x51
	switch_CH7	SFP28 PORT 14	0x50, 0x51
I2C 1 I2C switch (73)	switch_CH0	SFP28 PORT 18	0x50, 0x51
	switch_CH1	SFP28 PORT 17	0x50, 0x51
	switch_CH2	SFP28 PORT 20	0x50, 0x51
	switch_CH3	SFP28 PORT 19	0x50, 0x51
	switch_CH4	SFP28 PORT 21	0x50, 0x51
	switch_CH5	SFP28 PORT 23	0x50, 0x51
	switch_CH6	SFP28 PORT 22	0x50, 0x51
	switch_CH7	SFP28 PORT 24	0x50, 0x51
I2C 1 I2C switch (74)	switch_CH0	SFP28 PORT 27	0x50, 0x51
	switch_CH1	SFP28 PORT 25	0x50, 0x51
	switch_CH2	SFP28 PORT 28	0x50, 0x51
	switch_CH3	SFP28 PORT 26	0x50, 0x51
	switch_CH4	SFP28 PORT 29	0x50, 0x51
	switch_CH5	SFP28 PORT 32	0x50, 0x51
	switch_CH6	SFP28 PORT 30	0x50, 0x51
	switch_CH7	SFP28 PORT 31	0x50, 0x51
I2C 1 I2C switch (75)	switch_CH0	SFP28 PORT 34	0x50, 0x51
	switch_CH1	SFP28 PORT 33	0x50, 0x51
	switch_CH2	SFP28 PORT 36	0x50, 0x51
	switch_CH3	SFP28 PORT 35	0x50, 0x51
	switch_CH4	SFP28 PORT 37	0x50, 0x51
	switch_CH5	SFP28 PORT 39	0x50, 0x51

	switch_CH6	SFP28 PORT 38	0x50, 0x51
	switch_CH7	SFP28 PORT 40	0x50, 0x51
I2C 1 I2C switch (76)	switch_CH0	SFP28 PORT 41	0x50, 0x51
	switch_CH1	SFP28 PORT 42	0x50, 0x51
	switch_CH2	SFP28 PORT 45	0x50, 0x51
	switch_CH3	SFP28 PORT 43	0x50, 0x51
	switch_CH4	SFP28 PORT 44	0x50, 0x51
	switch_CH5	SFP28 PORT 48	0x50, 0x51
	switch_CH6	SFP28 PORT 46	0x50, 0x51
	switch_CH7	SFP28 PORT 47	0x50, 0x51

Note. PSU1 DC48V and DC12V power supply address – 0x50
PSU2 DC48V and DC12V power supply address – 0x53
PSU1 AC power supply address – 0x59/0x51
PSU2 AC power supply address – 0x5B/0x53

5.5. UART

The UART port will be configured to enable UART1 only and support RJ45 or micro-usb type.
The console port interface conforms to the RJ45 and USB electrical specification.
The console port is located on the front panel. The interface supports asynchronous mode with default eight data bits, one stop bit, and no parity. The unit will operate at the following baud rates:

- **115200 (Default)**

Figure 34 Uart Connection

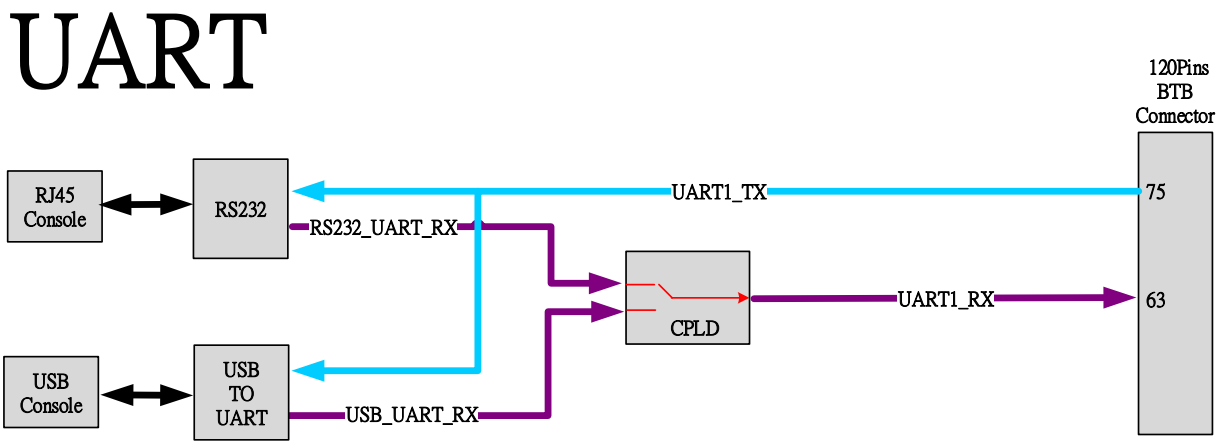


Table 21 RS-232 Pin definition (RJ45)

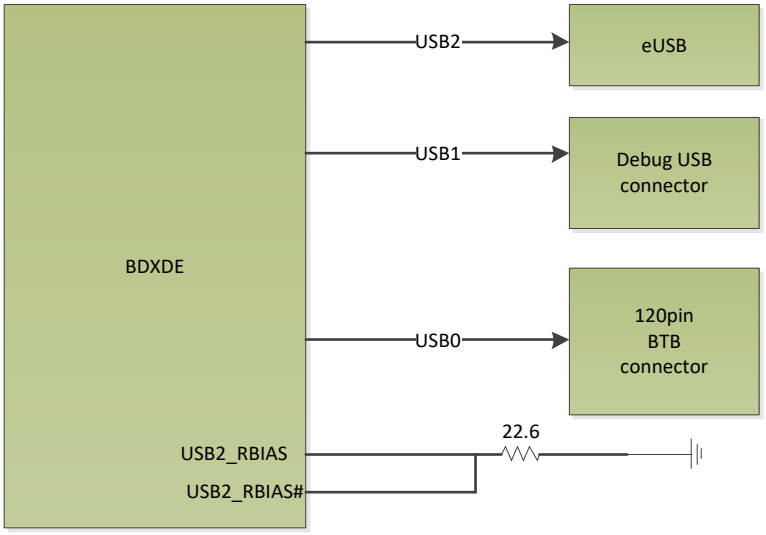
Pin number	Pin name	Pin number	Pin name
1	RJ45_RTS	2	RJ45_DTR
3	RJ45_TXD	4	GND
5	GND	6	RJ45_RXD

7	RJ45_DSR	**8**	RJ45_CTS

5.6. USB

There are three USB 2.0 interfaces in the project. The USB-0 via the 120pins BTB connector to switch board for chassis external type A USB connector, USB-1 is for debug function and USB-2 connect to eUSB module for internal USB access.
The mapping table and connection are as below.

Figure 35 USB connection



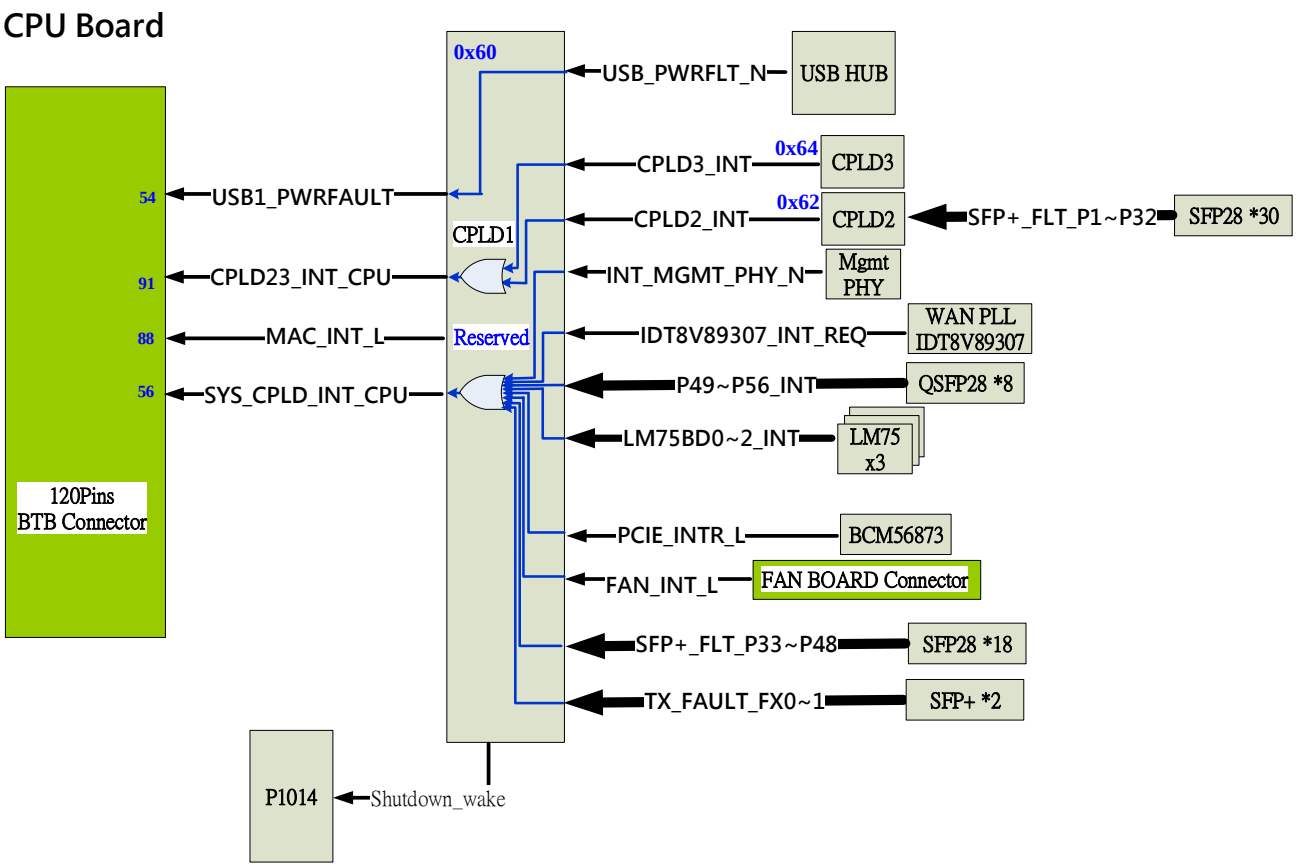
5.7. Interrupt

CPLD in Switch board will collect all interrupts in Switch board from different devices, and then pass to CPU. Those devices are as below.

- MAC (BCM56873)
- MGMT Phy(BCM54616s)
- Thermal sensor(LM75)
- Fan
- IDT 8V89307
- QSFP28 Transceiver
- SFP28 Transceiver
- SFP+ Transceiver

Figure 36 Interrupt Connection

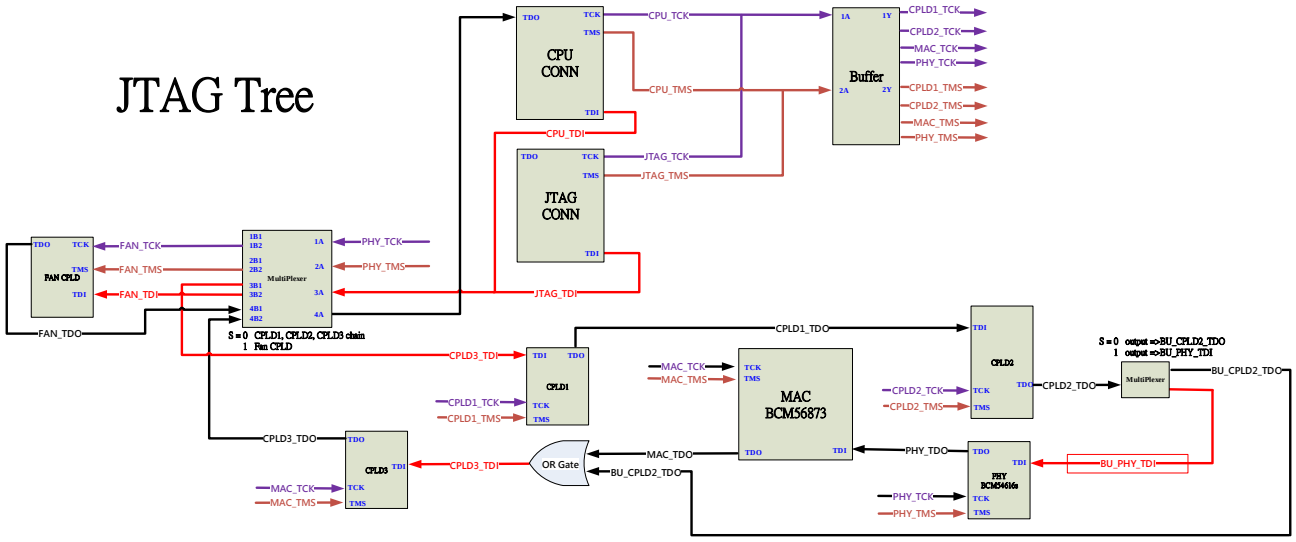
Interrupt



5.8. JTAG

ES7656BT3 had only done the JTAG download chain for three CPLD with JTAG interface, it make the CPLD programing more quickly. The TCK and TMS pass to all devices by buffer. TDI and TDI are connecting directly.

Figure 37 JTAG chain



5.9. LED Indicator

The system has 5 status LEDs and 60 port LEDs. The 5 status LEDs are for PWR1, PWR2, Fan, Diag and LOG. The 60 port LEDs are for 8 40G/100G Ethernet ports, 48 25G/10G Ethernet ports, 2 1G/10G SFP+ ports and 2 LEDs are for 10/100/1000BASE-T RJ45 ports.

5.9.1. Status LED

Figure 38 Status LED

Table 22 Status LED Definition

LED	Color	Description
PS1 (Power Supply Status)	Green	This power is operating normally.
	Red	PWR present but not power on or this power is fault.
	Off	Power supply not present.
PS2 (Power Supply	Green	This power is operating normally.
	Red	PWR present but not power on or this power is fault.
	Off	Power supply not present.

Status)		
FAN	Green	System FAN operating normally.
	Red	Fan tray present buy system FAN is fault.
	OFF	System OFF
Diag (Diagnostic)	Green	System self-diagnostic test successfully completed.
	Red	System self-diagnostic test has detected a fault. (Fan, thermal or any interface fault.)
	OFF	System OFF
LOC	Yellow Flashing	Flashing by remote management command. Assists the technician in finding the right device for service in the rack.
	OFF	Not a particular switch that technician need to find

5.9.2. Port LED

There are 80 tri-color(Red/Green/Blue) LEDs for 25G SFP28 48 ports, 100G QSFP28 8 ports with 4 lanes per port and SFP+ 2 ports, so 1 tri-color LED indicates 1 SFP28 port, 1 SFP+ port or 1 Lane per QSFP port. The QSFP28 port can run in 40G/4x10G or 100G/4x25G breakout mode. Note: The LEDs flash to indicate activity.

Figure 39 QSFP28 Port LED

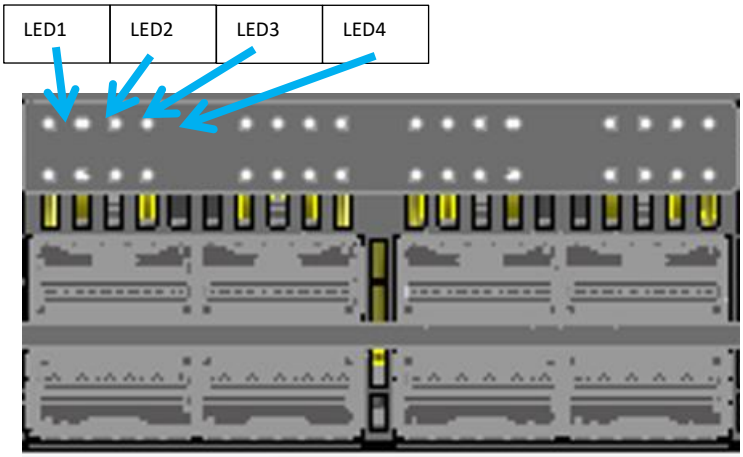


Table 23 QSFP28 Port LED Definition

LED	Color	Mode
LED 1~4 (Port 49~56)	On/Flashing Green	QSFP28 port has a valid link at 100G. Flashing indicates activity.
	OFF	There is no link on the port.
	On/Flashing Blue	QSFP28 port has a valid link at 40G. Flashing indicates activity.
	OFF	There is no link on the port.
	On/Flashing	QSFP28 port has a valid link at 25G via

	Yellow	break out cable. The LED on 100G QSFP end is also present OFF. Flashing indicates activity. (With Breakout cable)
	OFF	There is no link on the port.
	On/Flashing Purple	QSFP28 port has a valid link at 10G via break out cable. The LED on 40G QSFP end is also present OFF. Flashing indicates activity. (With Breakout cable)
	OFF	There is no link on the port.

The CPLD drives the R/G/B LED by de-coding the MAC's LED bus.

Figure 40 SFP28 Port LED

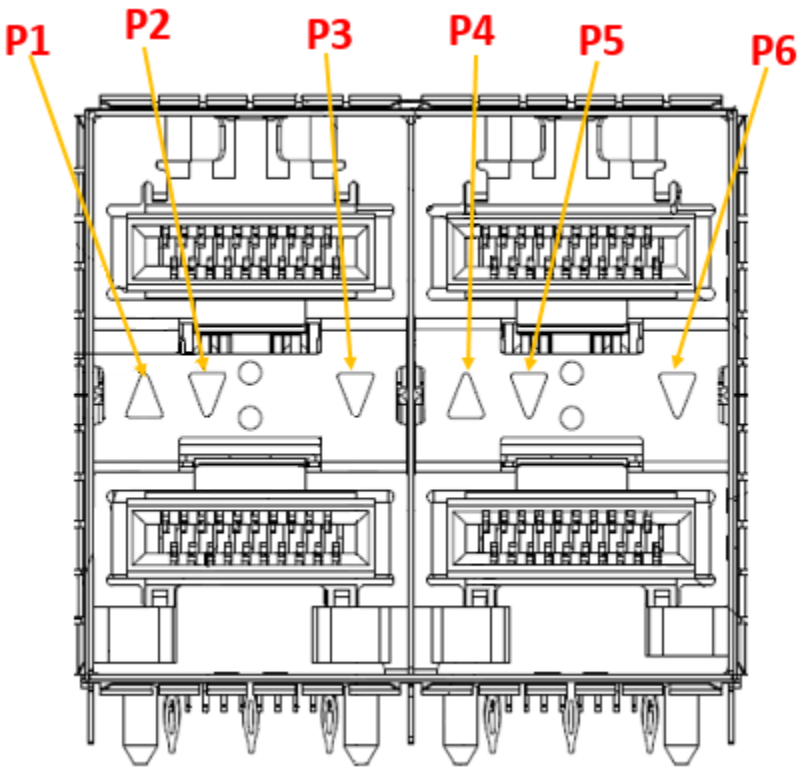


Table 24 SFP28 Port LED Definition

LED	Color	Mode
SFP28 Port LED	On/Flashing Green	SFP28 port has a valid link at 25G. Flashing indicates activity.
	On/Flashing Yellow	SFP28 port has a valid link at 10G. Flashing indicates activity.
	OFF	There is no link on the port.

Figure 41 SFP+ Port LED

Table 25 SFP+ Port LED Definition

LED	Color	Mode
SFP+ Port LED	On/Flashing Green	SFP+ port has a valid link at 10G. Flashing indicates activity.
	On/Flashing Yellow	SFP+ port has a valid link at 1G. Flashing indicates activity.
	OFF	There is no link on the port.

5.9.3. Management Port LED

The management port support 1G/ 100M / 10M speed. Two port LEDs are reserved and integrated into the RJ-45, yellow at the left side and green at the right side.

Figure 42 Management Port LED

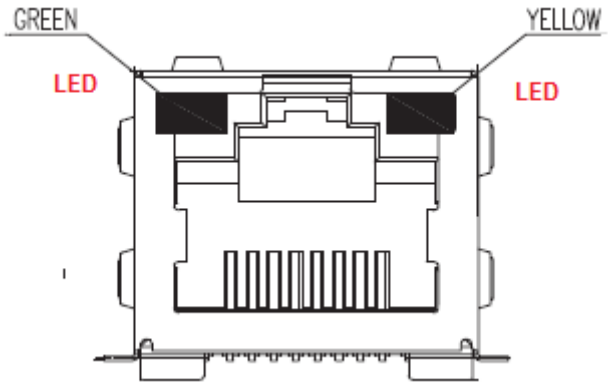


Table 26 Management Port LED Definition

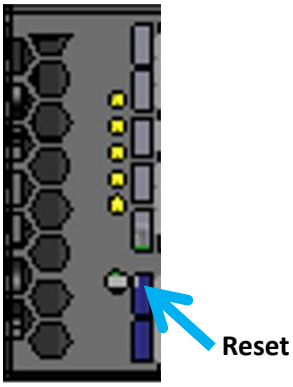
LED	Color	Mode
MGMT Port LED	On Green	Port has a valid link
	Flashing Yellow	Flashing indicates activity

	OFF	There is no link on the port.

5.10. Button

A reset button is reserved on the front panel to reboot the system.

Figure 43 Front reset button



5.11. Thermal system

5.11.1. Temperature sensor

There are five temperature sensors in AS7326-56x system, and the locations are shown in the picture below. CPU can access the sensor via I2C interface, and the sensor has the interrupt signal connect with CPLD for over-temp event application.

The temp sensor solution is “LIN LM75BD 2.8-5.5V TEMP MINOTOR SO8 LT/LF NXP”

The thermal alarm will be 70 degree at initial value and it is via thermal sensor’s interrupt to CPU module. But the temperature value will be optimized after thermal test result.

Figure 44 Temp sensor location

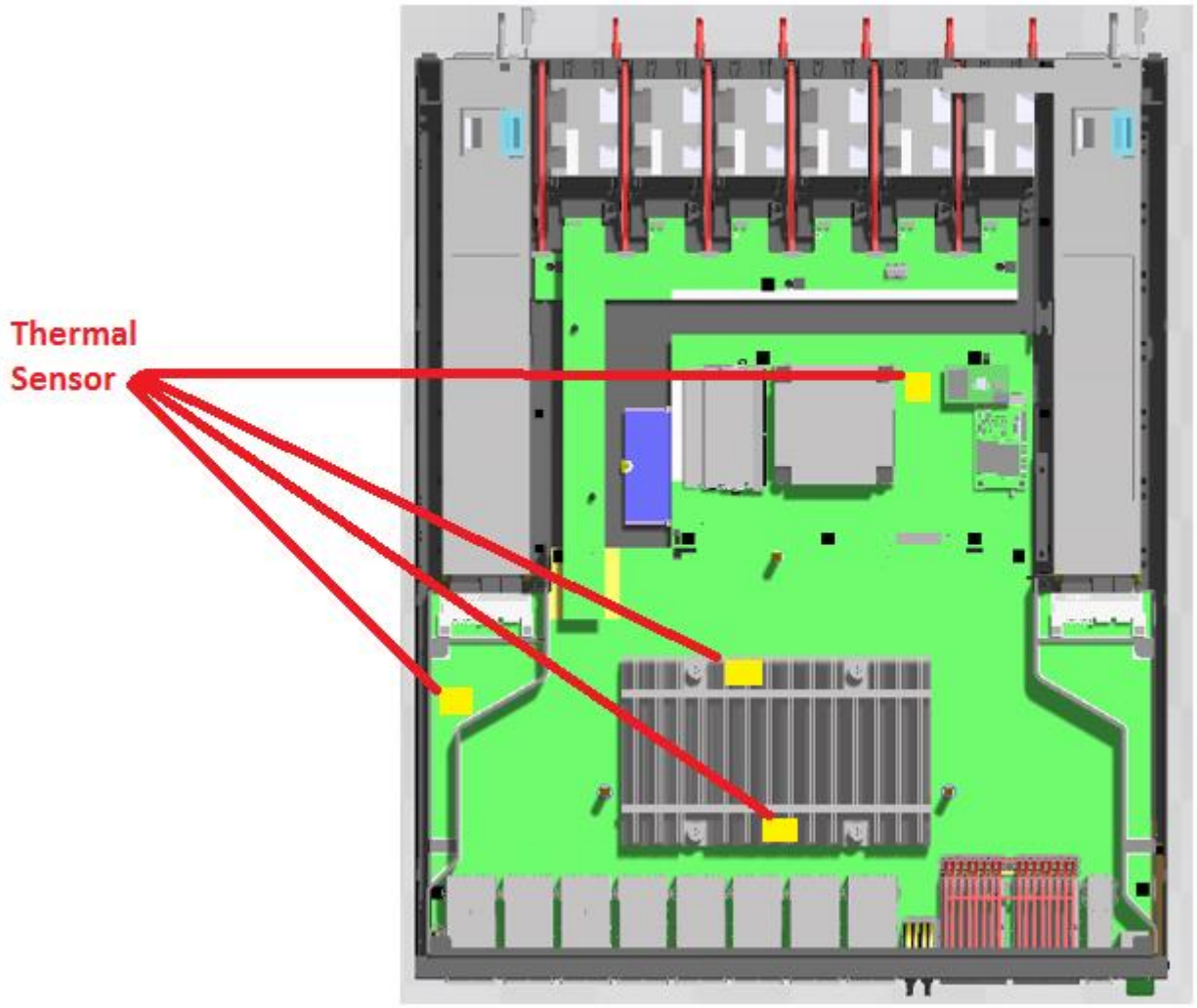
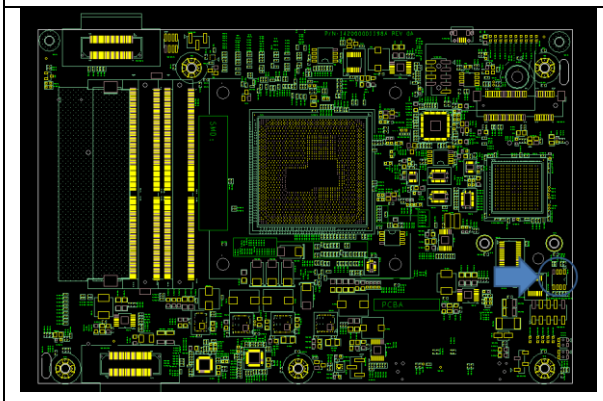


Figure 45 CPU board - Temp sensor location

Top	Bottom
	

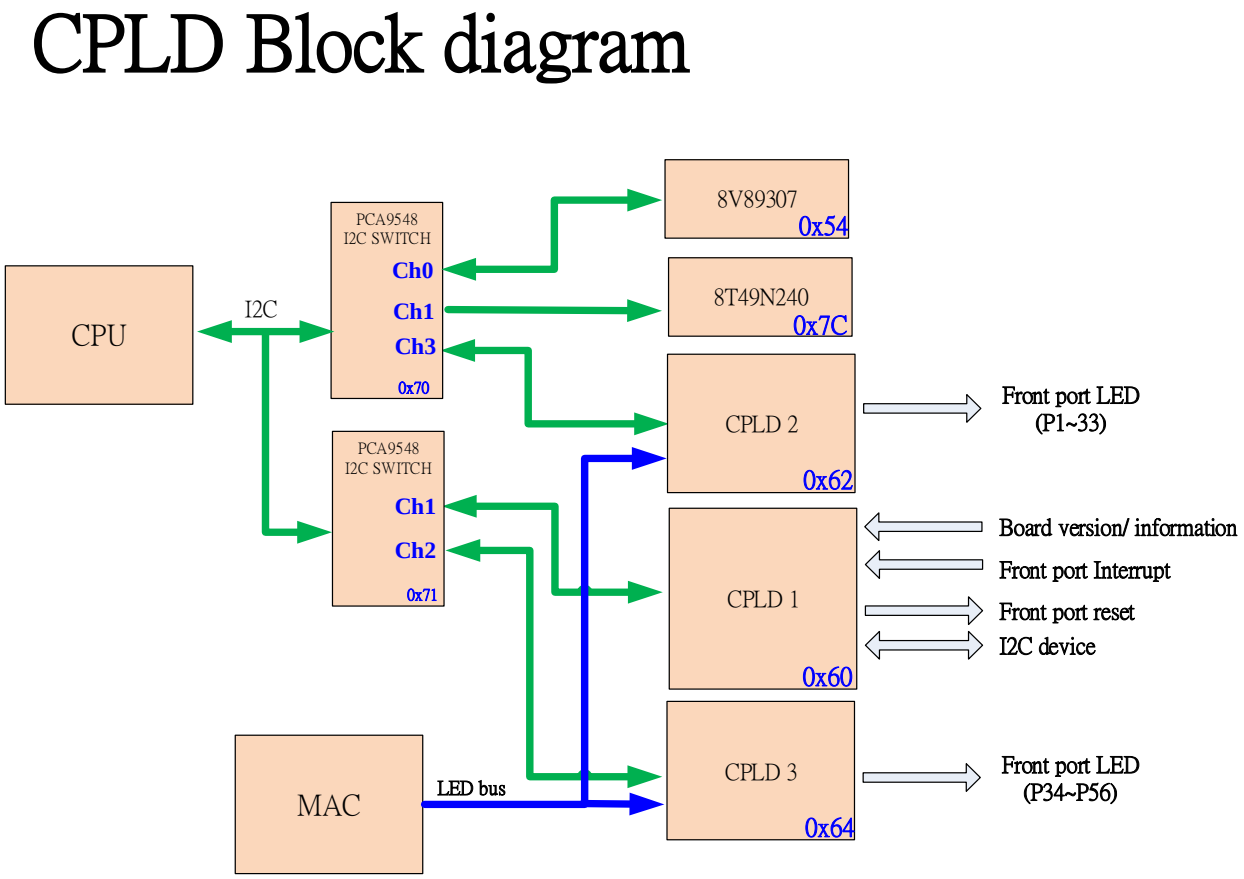
5.12. CPLD

The AS7326-56x has three CPLD devices for decoding, Fan module status, reset system, power module status and System interrupt.

I2C address info:

*CPLD1:0x60
*CPLD2:0x62
*CPLD3:0x64
*Fan_CPLD:0x66

Figure 46 CPLD Block Diagram



The CPLD on the CPU board is Altera 5M1270ZF256C5N.The CPLD has registers to monitor the status of the fan module, thermal sensors and power module.
The CPLD also has the circuit of registers of CPLD code version and board ID.

Table 27 CPLD2,3 to LED Port Mapping

CPLD2		CPLD3	
Register	CPLD LED Port Name	Register	CPLD LED Port Name
0x20	Port1	0x10	Port34
0x21	Port2	0x11	Port35
0x22	Port3	0x12	Port37

0x23	Port4	0x13	Port38
0x24	Port5	0x14	Port40
0x25	Port6	0x15	Port41
0x26	Port7	0x16	Port43
0x27	Port8	0x17	Port44
0x28	Port9	0x18	Port46
0x29	Port10	0x19	Port47
0x2A	Port11	0x30	Port49 LED0
0x2B	Port12	0x31	Port49 LED1
0x2C	Port13	0x32	Port49 LED2
0x2D	Port14	0x33	Port49 LED3
0x2E	Port15	0x34	Port50 LED0
0x2F	Port16	0x35	Port50 LED1
0x30	Port17	0x36	Port50 LED2
0x31	Port18	0x37	Port50 LED3
0x32	Port19	0x38	Port51 LED0
0x33	Port20	0x39	Port51 LED1
0x34	Port21	0x3A	Port51 LED2
0x35	Port22	0x3B	Port51 LED3
0x36	Port23	0x3C	Port52 LED0
0x37	Port24	0x3D	Port52 LED1
0x38	Port25	0x3E	Port52 LED2
0x39	Port26	0x3F	Port52 LED3
0x3A	Port27	0x40	Port53 LED0
0x3B	Port28	0x41	Port53 LED1
0x3C	Port29	0x42	Port53 LED2
0x3D	Port30	0x43	Port53 LED3
0x3E	Port31	0x44	Port54 LED0
0x3F	Port32	0x45	Port54 LED1
0x40	Port33	0x46	Port54 LED2
0x41	Port36	0x47	Port54 LED3
0x42	Port39	0x48	Port55 LED0
0x43	Port42	0x49	Port55 LED1
0x44	Port45	0x4A	Port55 LED2
0x45	Port48	0x4B	Port55 LED3
		0x4C	Port56 LED0
		0x4D	Port56 LED1

0x4E	Port56 LED2
0x4F	Port56 LED3
0x50	Port57
0x51	Port58

5.12.1. CPLD1 pin-out list

Table 28 CPLD1 Pin-out List

Pin	Net name	IN/ OUT	
J5	1PPS_CLK	IN	
R16	CPLD3_INT	IN	
D15	RESET_SYS_CPLD	IN	
F14	RESET_MAC	OUT	
F15	Manu_RST	OUT	
G16	CPU_THERMALTRIP	IN	
H5	CPLD1_25MHz	IN	
L16	Board_ID1	IN	
E14	USB1_PWRFAULT	OUT	
L15	SFP+_MOD_ABS_P29	IN	
C3	FAN_G	OUT	
J14	SFP+_RXLOS_P36	IN	
M12	SFP+_DIS_P36	OUT	
C8	PCA9548_14_RESET_N	OUT	
N15	P53_RESET_N	OUT	
P15	BU_SEL_2	OUT	
C9	PCA9548_13_RESET_N	OUT	
F11	PCIE_PERST_L	OUT	
N8	P55_MODPRSNT_N	IN	
H12	SFP+_RXLOS_P30	IN	
N16	P54_MODPRSNT_N	IN	
E16	IP_TS_GPIO1_2	IN	Reserved
H16	PCB_Version2	IN	
E15	SYS_CPLD_INT_CPU	OUT	
D16	I2C_0_SDA_CPLD1	IN/OUT	
M15	UART1_RX	OUT	
N2	SFP+_MOD_ABS_P37	IN	

F12	MAC_RESET_N	OUT	
T15	SFP+_MOD_ABS_P30	IN	
L4	P52_MODPRSNT_N	IN	
J13	SFP+_FLT_P29	IN	
K14	SFP+_DIS_P29	OUT	
H14	PS1_PDB_ALERT	OUT	
M8	RX_LOSS_FX1	IN	
M9	TX_FAULT_FX0	IN	
C14	PS2_EEPROM_WP	OUT	Reserved
D14	CPU_JTAG_RST	IN	
G14	POWER_RST	IN	
E1	CPLD2_INT	IN	
K16	Board_ID2	IN	
G12	FAN_INT_L	IN	
D10	P49_MODPRSNT_N	IN	
D11	P50_MODPRSNT_N	IN	
G15	USB1_VBUS	IN	
P10	PRESENT_FX0	IN	
M16	1PPS_CPU	OUT	
G13	PS2_12V_PG	IN	
K12	PS1_AC-OK	IN	Reserved
L12	USB_UART_RX	IN	
P11	TX_FAULT_FX1	IN	
T5	SFP+_MOD_ABS_P38	IN	
T7	SFP+_MOD_ABS_P39	IN	
T11	SFP+_FLT_P34	IN	
A12	FAN_SDA_2	IN/OUT	
R6	SFP+_FLT_P38	IN	
R10	SFP+_MOD_ABS_P33	IN	
B13	EE_WP	OUT	
B11	FAN_SCL_2	OUT	
T10	SFP+_RXLOS_P33	IN	
D1	SFP+_FLT_P47	IN	
E2	shutdown_wake	OUT	
R1	SFP+_FLT_P37	IN	

E4	FAN_B	OUT	
E3	SFP+_DIS_P40	OUT	
T4	SFP+_DIS_P42	OUT	
F2	SFP+_DIS_P47	OUT	
F3	SFP+_DIS_P48	OUT	
T9	SFP+_FLT_P35	IN	
R5	SFP+_FLT_P39	IN	
D13	PS1_PRESENT	IN	
R7	SFP+_RXLOS_P39	IN	
G3	SFP+_MOD_ABS_P46	IN	
G4	SFP+_DIS_P46	OUT	
A5	PSU1_G	OUT	
F4	SFP+_RXLOS_P46	IN	
B5	PSU1_R	OUT	
B6	PSU1_B	OUT	
R8	SFP+_DIS_P38	OUT	
E11	1PPS_GPIO2	OUT	
M11	SFP+_FLT_P36	IN	
J12	USB_UART_SUSPEND_L	IN	Reserved
E10	PCIE_WAKE_L	IN	Reserved
K13	PS1_ON	OUT	
E9	PCIE_INTR_L	IN	
E6	PCA9548_02_RESET_N	OUT	
A9	PCA9548_12_RESET_N	OUT	
F1	SFP+_RXLOS_P48	IN	
G2	SFP+_MOD_ABS_P48	IN	
A11	IP_BS0_CLK_2	IN	Reserved
E12	CPLD_USB_VBUS_DET	IN	
B10	PCA9548_00_RESET_N	OUT	
M10	SFP+_MOD_ABS_P40	IN	
H1	SFP+_FLT_P45	IN	
J1	SFP+_FLT_P43	IN	
A15	CPLD23_INT_CPU	OUT	
H2	SFP+_MOD_ABS_P44	IN	
G1	SFP+_DIS_P45	OUT	

B14	MAC_INT_L	IN	Reserved
A10	PCA9548_10_RESET_N	OUT	
B9	PCA9548_11_RESET_N	OUT	
A8	CPLD_RST	OUT	
B12	PCA9548_01_RESET_N	OUT	
A13	N/A(CPLD_IP_BS0)	OUT	
B8	PCA9548_15_RESET_N	OUT	
E8	SFP+_FLT_P41	IN	
E7	PCA9548_16_RESET_N	OUT	
E5	LM75BD0_INT	IN	
A7	PSU2_G	OUT	
D9	IDT8V89307_RST	OUT	
R4	SFP+_RXLOS_P41	IN	
B4	DIAG_G	OUT	
B3	FAN_R	OUT	
A2	Reset_button_RST	IN	
H3	SFP+_FLT_P46	IN	
F6	IP_CPLD_BS0_HB	IN	Reserved
T13	SFP+_MOD_ABS_P34	IN	
B7	PSU2_B	OUT	
A6	PSU2_R	OUT	
B1	SFP+_MOD_ABS_P47	IN	
L2	SFP+_RXLOS_P43	IN	
M1	SFP+_MOD_ABS_P45	IN	
L1	SFP+_FLT_P44	IN	
J15	SFP+_MOD_ABS_P36	IN	
K5	SFP+_RXLOS_P42	IN	
K2	SFP+_DIS_P43	OUT	
C7	LOC_B	OUT	
M7	SFP+_DIS_P39	OUT	
R13	SFP+_FLT_P33	IN	
M6	SFP+_FLT_P40	IN	
R12	SFP+_RXLOS_P34	IN	
T8	SFP+_DIS_P33	OUT	
R14	SFP+_RXLOS_P29	IN	

N1	SFP+_DIS_P44	OUT	
K1	SFP+_MOD_ABS_P43	IN	
T12	SFP+_MOD_ABS_P35	IN	
R11	SFP+_RXLOS_P35	IN	
F5	L1_RCVRD_CLK_VALID	IN	
J2	SFP+_RXLOS_P44	IN	
K4	P52_INT	IN	
M2	SFP+_RXLOS_P45	IN	
E13	PS2_AC-OK	IN	Reserved
A4	DIAG_B	OUT	
L5	SFP+_MOD_ABS_P42	IN	
C13	PS2_PDB_ALERT	OUT	
C4	BU_SEL_1	OUT	
C5	LOC_R	OUT	
C6	System_B	OUT	Reserved
H4	P50_INT	IN	
L11	RS232_UART_RX	IN	
C15	UCD9090_ALERT_L	IN	Reserved
B16	I2C_0_SCL_CPLD1	IN	
F13	PS2_ON	OUT	
K3	P51_INT	IN	
J16	PCB_Version1	IN	
K15	LM75BD1_INT	IN	
P7	P56_MODPRSNT_N	IN	
P5	P54_RESET_N	OUT	
P2	SFP+_RXLOS_P37	IN	
P9	P55_INT	IN	
P6	P53_MODPRSNT_N	IN	
P4	P54_INT	IN	
N3	P51_RESET_N	OUT	
P8	P56_RESET_N	OUT	
D12	LM75BD_SDA	IN/OUT	
D4	DIAG_R	OUT	
D5	System_R	OUT	Reserved
D6	System_G	OUT	Reserved

D7	LOC_G	OUT	
D8	LM75BD2_INT	IN	
L3	P49_INT	IN	
H15	PS1_AC_ALERT	IN	
C12	PS2_AC_ALERT	IN	
M3	P51_MODPRSNT_N	IN	
H13	PS1_EEPROM_WP	OUT	Reserved
C2	SFP+_FLT_P48	IN	
D2	SFP+_RXLOS_P47	IN	
D3	LM75BD_SCLK	OUT	
N5	P53_INT	IN	
N12	TX_DIS_FX1	OUT	
N11	RX_LOSS_FX0	IN	
F16	CPU_PROCHOT	IN	
N6	P56_INT	IN	
N7	P55_RESET_N	OUT	
L10	SFP+_RXLOS_P40	IN	
J3	P50_RESET_N	OUT	
C11	PS2_PRESENT	IN	
C10	IDT8V89307_INT_REQ	IN	
J4	P49_RESET_N	OUT	
N13	USB_PWRON_N	OUT	
F7	IP_CPLD_BS0_TC	IN	Reserved
G11	Fan_idle	OUT	Reserved
G6	L1_RCVRD_CLK_VALID_BKUP	IN	
L7	SFP+_DIS_P41	OUT	
N10	PRESENT_FX1	IN	
N9	TX_DIS_FX0	OUT	
P12	USB_RESET_N	OUT	
P13	USB_PWRFLT_N	IN	
K6	SFP+_FLT_P42	IN	
M4	P52_RESET_N	OUT	
F10	FAN_SDA_1	IN/OUT	
K11	FAN_SCL_1	OUT	
L13	PS1_12V_PG	IN	

L14	SFP+_DIS_P34	OUT	
M13	SFP+_DIS_P30	OUT	
M14	SFP+_FLT_P30	IN	
N14	MGMT_PHY_RST_N	OUT	
P14	INT_MGMT_PHY_N	IN	
R3	SFP+_MOD_ABS_P41	IN	
R9	SFP+_DIS_P35	OUT	
T2	SFP+_DIS_P37	OUT	
T6	SFP+_RXLOS_P38	IN	

5.12.2. CPLD2 pin-out list

Table 29 CPLD2 Pin-out List

Pin	Net name	IN/ OUT
C2	P3_Lane2_LED_B	OUT
C3	P46_Lane1_LED_R	OUT
D1	P2_Lane1_LED_R	OUT
D2	P2_Lane1_LED_B	OUT
D3	SFP+_RXLOS_P2	IN
D4	SFP+_MOD_ABS_P2	IN
E1	P3_Lane2_LED_R	OUT
E2	P2_Lane1_LED_G	OUT
E3	SFP+_DIS_P3	OUT
E4	SFP+_FLT_P3	IN
E5	SFP+_DIS_P31	OUT
F1	P4_Lane3_LED_B	OUT
F2	P4_Lane3_LED_G	OUT
F3	P8_Lane3_LED_B	OUT
F4	SFP+_RXLOS_P3	IN
F5	SFP+_FLT_P31	IN
F6	IP_LED_DATA2	IN
G1	P4_Lane3_LED_R	OUT
G2	P7_Lane2_LED_G	OUT
G3	SFP+_MOD_ABS_P3	IN
G4	SFP+_FLT_P2	IN
G5	SFP+_MOD_ABS_P28	IN
G6	SFP+_MOD_ABS_P21	IN

G7	SFP+_RXLOS_P21	IN
H1	P7_Lane2_LED_B	OUT
H2	P8_Lane3_LED_G	OUT
H3	SFP+_RXLOS_P4	IN
H4	SFP+_MOD_ABS_P4	IN
H5	SFP+_DIS_P25	OUT
H6	SFP+_FLT_P24	IN
J1	P1_Lane0_LED_B	OUT
J2	P8_Lane3_LED_R	OUT
J3	SFP+_FLT_P4	IN
J4	SFP+_DIS_P4	OUT
J5	SFP+_RXLOS_P27	IN
K1	P1_Lane0_LED_R	OUT
K2	P7_Lane2_LED_R	OUT
K3	SFP+_RXLOS_P7	IN
K4	SFP+_MOD_ABS_P7	IN
K5	SFP+_DIS_P2	OUT
L1	SFP+_DIS_P8	OUT
L2	P1_Lane0_LED_G	OUT
L3	SFP+_FLT_P8	IN
L4	SFP+_RXLOS_P1	IN
L5	SFP+_MOD_ABS_P32	IN
L6	SFP+_FLT_P25	IN
M1	P5_Lane0_LED_B	OUT
M2	P12_Lane3_LED_B	OUT
M3	SFP+_MOD_ABS_P1	IN
M4	SFP+_DIS_P1	OUT
M5	SFP+_FLT_P28	IN
M6	SFP+_DIS_P18	OUT
N1	P5_Lane0_LED_G	OUT
N2	P12_Lane3_LED_G	OUT
N3	SFP+_FLT_P1	IN
N4	SFP+_RXLOS_P8	IN
N5	SFP+_DIS_P28	OUT
P1	P5_Lane0_LED_R	OUT
P2	P12_Lane3_LED_R	OUT
P3	SFP+_MOD_ABS_P8	IN

P4	SFP+_FLT_P7	IN
R1	P6_Lane1_LED_B	OUT
R2	P6_Lane1_LED_G	OUT
R3	SFP+_DIS_P7	OUT
T2	P6_Lane1_LED_R	OUT
T3	SFP+_MOD_ABS_P12	IN
A10	IP_LED_CLK1	IN
A11	P23_Lane2_LED_B	OUT
A12	P22_Lane1_LED_G	OUT
A13	IP_LED_DATA1	IN
A14	SFP+_RXLOS_P25	IN
A15	P22_Lane1_LED_B	OUT
A17	P18_Lane1_LED_G	OUT
A2	P29_Lane0_LED_G	OUT
A4	P32_Lane3_LED_R	OUT
A5	P36_Lane3_LED_R	OUT
A6	P36_Lane3_LED_B	OUT
A7	P32_Lane3_LED_B	OUT
A8	P28_Lane3_LED_R	OUT
A9	P31_Lane2_LED_B	OUT
B1	P3_Lane2_LED_G	OUT
B10	P31_Lane2_LED_G	OUT
B11	P22_Lane1_LED_R	OUT
B12	P23_Lane2_LED_G	OUT
B13	P21_Lane0_LED_R	OUT
B14	P21_Lane0_LED_G	OUT
B15	P21_Lane0_LED_B	OUT
B16	P18_Lane1_LED_R	OUT
B18	P35_Lane2_LED_R	OUT
B3	P25_Lane0_LED_B	OUT
B4	P25_Lane0_LED_G	OUT
B5	P25_Lane0_LED_R	OUT
B6	P31_Lane2_LED_R	OUT
B7	P36_Lane3_LED_G	OUT
B8	P32_Lane3_LED_G	OUT
B9	P28_Lane3_LED_B	OUT
C10	P19_Lane2_LED_G	OUT

C11	P27_Lane2_LED_R	OUT
C12	P27_Lane2_LED_B	OUT
C13	N/A	
C14	P30_Lane1_LED_B	OUT
C15	P30_Lane1_LED_R	OUT
C4	P46_Lane1_LED_G	OUT
C5	P43_Lane2_LED_R	OUT
C6	P43_Lane2_LED_B	OUT
C7	P40_Lane3_LED_R	OUT
C8	P40_Lane3_LED_B	OUT
C9	P29_Lane0_LED_R	OUT
D10	P20_Lane3_LED_B	OUT
D11	P28_Lane3_LED_G	OUT
D12	P27_Lane2_LED_G	OUT
D13	P23_Lane2_LED_R	OUT
D14	P30_Lane1_LED_G	OUT
D5	P46_Lane1_LED_B	OUT
D6	SFP+_RXLOS_P28	IN
D7	P43_Lane2_LED_G	OUT
D8	P40_Lane3_LED_G	OUT
D9	P29_Lane0_LED_B	OUT
E10	P19_Lane2_LED_B	OUT
E11	SFP+_FLT_P18	IN
E12	SFP+_FLT_P22	IN
E13	SFP+_RXLOS_P26	IN
E6	IP_LED_CLK2	IN
E7	IP_LED_DATA0	IN
E8	IP_LED_CLK0	IN
E9	SFP+_MOD_ABS_P20	IN
F10	SFP+_FLT_P27	IN
F11	SFP+_DIS_P27	OUT
F12	SFP+_RXLOS_P23	IN
F7	SFP+_MOD_ABS_P23	IN
F8	IP_LED_CLK4	IN
F9	IP_LED_DATA4	IN
C16	P26_Lane1_LED_G	OUT
C17	P17_Lane0_LED_R	OUT

D15	P26_Lane1_LED_B	OUT
D16	P26_Lane1_LED_R	OUT
D17	P24_Lane3_LED_G	OUT
D18	P24_Lane3_LED_R	OUT
E14	SFP+_DIS_P23	OUT
E15	SFP+_FLT_P23	IN
E16	SFP+_RXLOS_P20	IN
E17	P17_Lane0_LED_G	OUT
E18	P24_Lane3_LED_B	OUT
F13	SFP+_RXLOS_P22	IN
F14	SFP+_FLT_P20	IN
F15	SFP+_RXLOS_P32	IN
F16	SFP+_MOD_ABS_P25	IN
F17	SFP+_DIS_P32	OUT
F18	P17_Lane0_LED_B	OUT
G12	SFP+_MOD_ABS_P26	IN
G13	N/A	
G14	SFP+_MOD_ABS_P22	IN
G15	SFP+_RXLOS_P19	IN
G16	SFP+_DIS_P20	OUT
G17	SFP+_FLT_P32	IN
G18	SFP+_MOD_ABS_P31	IN
H13	SFP+_DIS_P21	OUT
H14	P18_Lane1_LED_B	OUT
H15	SFP+_MOD_ABS_P19	IN
H16	N/A	
H17	N/A	
H18	N/A	
J14	P35_Lane2_LED_B	OUT
J15	N/A	
J16	N/A	
J17	N/A	
J18	N/A	
K14	SFP+_DIS_P14	OUT
K15	SFP+_MOD_ABS_P15	IN
K16	SFP+_FLT_P14	IN
K17	N/A	

K18	P35_Lane2_LED_G	OUT
L13	SFP+_MOD_ABS_P18	IN
L14	SFP+_RXLOS_P18	IN
L15	SFP+_FLT_P16	IN
L16	SFP+_RXLOS_P15	IN
L17	P37_Lane0_LED_B	OUT
L18	P37_Lane0_LED_G	OUT
M12	SFP+_DIS_P22	OUT
M13	SFP+_RXLOS_P17	IN
M14	SFP+_FLT_P17	IN
M15	SFP+_MOD_ABS_P16	IN
M16	SFP+_DIS_P16	OUT
M17	P37_Lane0_LED_R	OUT
M18	P13_Lane0_LED_G	OUT
N13	SFP+_MOD_ABS_P13	IN
N14	SFP+_MOD_ABS_P24	IN
N15	SFP+_MOD_ABS_P11	IN
N16	SFP+_RXLOS_P16	IN
N17	P13_Lane0_LED_R	OUT
N18	P13_Lane0_LED_B	OUT
P14	SFP+_FLT_P15	IN
P15	SFP+_FLT_P11	IN
P16	P19_Lane2_LED_R	OUT
P17	P20_Lane3_LED_G	OUT
P18	P20_Lane3_LED_R	OUT
R15	SFP+_DIS_P11	OUT
R16	SFP+_RXLOS_P31	IN
R17	SFP+_DIS_P26	OUT
R18	SFP+_FLT_P26	IN
T16	I2C_0_SDA_CPLD2	IN/OUT
T17	SFP+_MOD_ABS_P27	IN
N11	SFP+_RXLOS_P13	IN
N12	SFP+_DIS_P19	OUT
N7	IP_LED_CLK3	IN
N8	IP_LED_DATA3	IN
P10	SFP+_DIS_P10	OUT
P11	SFP+_FLT_P10	IN

P12	SFP+_FLT_P19	IN
P13	SFP+_MOD_ABS_P14	IN
P6	SFP+_DIS_P24	OUT
P7	CPLD_RST	IN
P8	CPLD2_INT	OUT
P9	SFP+_RXLOS_P24	IN
R10	SFP+_RXLOS_P9	IN
R11	SFP+_RXLOS_P10	IN
R12	SFP+_DIS_P9	OUT
R13	SFP+_FLT_P9	IN
R14	N/A	
R5	SFP+_DIS_P5	OUT
R6	SFP+_FLT_P5	IN
R7	SFP+_MOD_ABS_P17	IN
R8	SFP+_DIS_P17	OUT
R9	SFP+_MOD_ABS_P9	IN
T10	N/A	
T11	N/A	
T12	N/A	
T13	N/A	
T14	N/A	
T15	N/A	
T4	SFP+_RXLOS_P12	IN
T5	SFP+_RXLOS_P6	IN
T6	SFP+_DIS_P6	OUT
T7	SFP+_MOD_ABS_P6	IN
T8	SFP+_RXLOS_P5	IN
T9	SFP+_DIS_P12	OUT
U1	P10_Lane1_LED_B	OUT
U10	P14_Lane1_LED_R	OUT
U11	P14_Lane1_LED_B	OUT
U12	SFP+_MOD_ABS_P10	IN
U13	I2C_0_SCL_CPLD2	IN
U14	SFP+_RXLOS_P14	IN
U15	SFP+_DIS_P15	OUT
U16	SFP+_RXLOS_P11	IN
U18	P16_Lane3_LED_G	OUT

U3	P9_Lane0_LED_B	OUT
U4	P9_Lane0_LED_G	OUT
U5	P9_Lane0_LED_R	OUT
U6	P11_Lane2_LED_G	OUT
U7	SFP+_FLT_P6	IN
U8	SFP+_MOD_ABS_P5	IN
U9	SFP+_FLT_P12	IN
V10	P14_Lane1_LED_G	OUT
V11	P15_Lane2_LED_B	OUT
V12	P15_Lane2_LED_G	OUT
V13	P15_Lane2_LED_R	OUT
V14	P16_Lane3_LED_B	OUT
V15	P16_Lane3_LED_R	OUT
V17	N/A	
V2	P10_Lane1_LED_G	OUT
V4	P10_Lane1_LED_R	OUT
V5	P11_Lane2_LED_B	OUT
V6	P11_Lane2_LED_R	OUT
V8	N/A	
V9	N/A	
N9	SFP+_FLT_P13	IN
N10	SFP+_DIS_P13	OUT
J6	CPLD2_25MHz	IN
K6	N/A	
K13	N/A	
J13	SFP+_FLT_P21	IN

5.12.3. CPLD3 pin-out list

Table 30 CPLD3 Pin-out List

Pin	Net name	IN/ OUT
T9	P54_Lane2_LED_R	OUT
R9	P54_Lane3_LED_B	OUT
R5	P54_Lane0_LED_G	OUT
T10	P53_Lane3_LED_B	OUT
K16	N/A	
R11	P55_Lane0_LED_G	OUT
T15	P56_Lane2_LED_B	OUT

T13	P55_Lane1_LED_G	OUT
M14	N/A	
F15	N/A	
E15	N/A	
G16	N/A	
R10	P56_Lane0_LED_G	OUT
C3	P39_Lane2_LED_G	OUT
T7	P53_Lane1_LED_B	OUT
L14	N/A	
K15	N/A	
T11	P56_Lane0_LED_B	OUT
K13	N/A	
L13	N/A	
N14	SFP_FX0_LED_G	OUT
F16	N/A	
E16	N/A	
G15	N/A	
D11	P45_Lane0_LED_R	OUT
C11	N/A	
C15	N/A	
D16	N/A	
A15	N/A	
M3	P51_Lane3_LED_R	OUT
N2	P51_Lane2_LED_R	OUT
E9	P56_Lane1_LED_G	OUT
C13	N/A	
B12	P49_Lane2_LED_G	OUT
A12	P50_Lane2_LED_B	OUT
B11	P49_Lane2_LED_B	OUT
C12	N/A	
D14	N/A	
F12	P48_Lane3_LED_R	OUT
C14	N/A	
D15	N/A	
B14	N/A	
M10	SFP_FX1_LED_R	OUT
G12	IP_LED_CLK4	IN

B13	N/A	
A10	P49_Lane1_LED_R	OUT
E12	P47_Lane2_LED_B	OUT
A11	P49_Lane2_LED_R	OUT
B9	P50_Lane1_LED_R	OUT
A9	P49_Lane1_LED_G	OUT
D4	P38_Lane1_LED_G	OUT
D10	P44_Lane3_LED_R	OUT
D13	N/A	
C10	P48_Lane3_LED_B	OUT
E5	IP_LED_CLK2	IN
E4	IP_LED_CLK0	IN
E7	IP_LED_CLK1	IN
A7	P50_Lane1_LED_G	OUT
F11	CPLD_RST	IN
F4	P54_Lane1_LED_B	OUT
B3	P34_Lane1_LED_G	OUT
B10	P49_Lane1_LED_B	OUT
D5	P34_Lane1_LED_B	OUT
D8	P45_Lane0_LED_G	OUT
E8	P48_Lane3_LED_G	OUT
D9	P44_Lane3_LED_B	OUT
C9	P45_Lane0_LED_B	OUT
E11	P47_Lane2_LED_R	OUT
E6	IP_LED_DATA4	IN
B8	P50_Lane1_LED_B	OUT
B1	P39_Lane2_LED_B	OUT
B7	P50_Lane0_LED_R	OUT
F13	N/A	
G14	N/A	
A8	P49_Lane0_LED_R	OUT
F5	IP_LED_DATA3	IN
H14	N/A	
G3	P51_Lane0_LED_B	OUT
M4	P54_Lane0_LED_B	OUT
L4	P52_Lane3_LED_B	OUT
H4	P52_Lane0_LED_R	OUT

K12	N/A	
J13	N/A	
N11	P55_Lane3_LED_B	OUT
H13	N/A	
C2	P42_Lane1_LED_G	OUT
D3	P38_Lane1_LED_R	OUT
G13	N/A	
F14	N/A	
H1	P50_Lane2_LED_R	OUT
T2	P51_Lane3_LED_G	OUT
N10	P55_Lane2_LED_G	OUT
H3	P52_Lane0_LED_B	OUT
L11	SFP_FX1_LED_B	OUT
E2	P49_Lane3_LED_B	OUT
N12	P56_Lane3_LED_R	OUT
T4	P53_Lane0_LED_G	OUT
L3	P52_Lane3_LED_G	OUT
T5	P53_Lane0_LED_R	OUT
L12	IP_LED_DATA0	IN
R14	P55_Lane2_LED_B	OUT
R13	P55_Lane1_LED_R	OUT
M13	N/A	
P12	P55_Lane3_LED_G	OUT
P13	SFP_FX0_LED_B	OUT
P11	P56_Lane2_LED_G	OUT
R16	P56_Lane2_LED_R	OUT
M11	SFP_FX1_LED_G	OUT
E10	CPLD3_INT	OUT
R3	P53_Lane1_LED_R	OUT
R4	P54_Lane1_LED_R	OUT
N13	SFP_FX0_LED_R	OUT
K14	N/A	
P14	MGMT_LINK_R	OUT
E13	N/A	
D12	P47_Lane2_LED_G	OUT
E14	N/A	
P2	P52_Lane3_LED_R	OUT

L15	N/A	
M12	MGMT_ACT	OUT
B16	N/A	
M16	N/A	
J14	N/A	
P9	P55_Lane0_LED_R	OUT
M7	PHY_LED2_CPLD	IN
M6	PHY_LED1_CPLD	IN
N6	P54_Lane3_LED_G	OUT
P7	P53_Lane3_LED_G	OUT
P5	P53_Lane2_LED_G	OUT
P15	P55_Lane3_LED_R	OUT
H16	N/A	
J16	N/A	
N15	P56_Lane3_LED_G	OUT
M15	N/A	
L16	N/A	
J12	N/A	
N9	P55_Lane1_LED_B	OUT
N16	P56_Lane3_LED_B	OUT
N7	P54_Lane3_LED_R	OUT
N8	P56_Lane0_LED_R	OUT
P8	P53_Lane3_LED_R	OUT
J15	N/A	
H15	N/A	
P10	P55_Lane2_LED_R	OUT
R8	P53_Lane2_LED_B	OUT
L5	P55_Lane0_LED_B	OUT
R12	P56_Lane1_LED_R	OUT
J4	P51_Lane2_LED_B	OUT
L2	P52_Lane1_LED_G	OUT
N1	P52_Lane2_LED_G	OUT
J2	P51_Lane0_LED_G	OUT
J1	P50_Lane3_LED_R	OUT
H2	P50_Lane3_LED_B	OUT
K3	P52_Lane2_LED_B	OUT
G1	P49_Lane3_LED_G	OUT

M2	P51_Lane2_LED_G	OUT
K5	P54_Lane0_LED_R	OUT
P4	P54_Lane2_LED_B	OUT
T12	P56_Lane1_LED_B	OUT
G4	IP_LED_CLK3	IN
N3	P53_Lane0_LED_B	OUT
T8	P54_Lane2_LED_G	OUT
K1	P52_Lane0_LED_G	OUT
K2	P51_Lane0_LED_R	OUT
R6	P53_Lane1_LED_G	OUT
K4	P52_Lane2_LED_R	OUT
M1	P51_Lane1_LED_R	OUT
R1	P51_Lane3_LED_B	OUT
F1	N/A	OUT
G2	P50_Lane3_LED_G	OUT
L1	P51_Lane1_LED_B	OUT
E3	IP_LED_DATA2	IN
C5	P34_Lane1_LED_R	OUT
C6	P41_Lane0_LED_R	OUT
A4	P33_Lane0_LED_B	OUT
A5	P50_Lane0_LED_B	OUT
R7	P54_Lane1_LED_G	OUT
D7	P42_Lane1_LED_B	OUT
B4	P33_Lane0_LED_R	OUT
A6	P49_Lane0_LED_B	OUT
F2	P49_Lane3_LED_R	OUT
F6	IP_LED_DATA1	IN
J3	P52_Lane1_LED_R	OUT
C4	P38_Lane1_LED_B	OUT
D1	P39_Lane2_LED_R	OUT
F3	P50_Lane2_LED_G	OUT
A2	P33_Lane0_LED_G	OUT
C7	P42_Lane1_LED_R	OUT
C8	P44_Lane3_LED_G	OUT
B6	P49_Lane0_LED_G	OUT
B5	P50_Lane0_LED_G	OUT
D6	P41_Lane0_LED_B	OUT

P6	P53_Lane2_LED_R	OUT
A13	N/A	
D2	P41_Lane0_LED_G	OUT
E1	P51_Lane1_LED_G	OUT
M9	I2C_0_SDA_CPLD3	IN/OUT
M8	I2C_0_SCL_CPLD3	IN
H12	N/A	
H5	CPLD_OSC_OUT_25MHz_R	IN
J5	P52_Lane1_LED_B	OUT

5.12.4. Fan CPLD pin-out list

Table 31 Fan board CPLD Pin-out List

Net name	pin number	Note
FAN_LED_G_5	M11	FAN5 LED
FAN_LED_R_6	N11	FAN6 LED
FAN_LED_R_5	P10	FAN5 LED
FAN6R_SENSOR	P12	FAN6
FAN5_PRES	R12	FAN5
FAN6_SENSOR	R13	FAN6
FAN6_PRES	R9	FAN6
CPLD_TDI_A	T10	
CPLD_TMS_A	T11	
CPLD_TDO_A	T12	
CPLD_TCK_A	T13	
CPU_UPGRADE_I2C_INT_L	T2	
BOARD_ID_1	T4	
BOARD_ID_2	T5	
VERSION_ID_1	T6	
VERSION_ID_2	T7	
VERSION_ID_3	T8	
FAN_LED_R_2	A10	FAN4 LED
GPIO_1	A11	
FAN_LED_R_3	A13	FAN3 LED
FAN3_SENSOR	A15	FAN3
FAN_IDLE	A2	

Net name	pin number	Note
FAN_SCL_2_R	A4	
FAN_SDA_2_R	A5	
FAN_INTERRUPT	A6	
FAN_MOS_CTRL	A7	
FAN_PWM_1	A8	FAN1
FAN_PWM_2	B13	FAN2
FAN_PWM_3	B16	FAN3
FAN_LED_R_1	B5	FAN1 LED
FAN1_DIR	B7	FAN1
FAN1R_SENSOR	B9	FAN1
FAN_LED_G_2	C10	FAN4 LED
FAN2R_SENSOR	C12	FAN2
FAN_LED_G_3	C13	FAN3 LED
FAN_LED_G_1	C7	FAN1 LED
FAN1_SENSOR	C8	FAN1
FAN2_DIR	D11	FAN2
EN_FAN6	D7	FAN6 Enable
EN_FAN5	D8	FAN5 Enable
EN_FAN4	D9	FAN4 Enable
EN_FAN3	E10	FAN3 Enable
EN_FAN2	E11	FAN2 Enable
EN_FAN1	E6	FAN1 Enable
25MHZ_OUT_R	H5	
JTAG_CPLD_TMS	N4	
JTAG_CPLD_TDI	L6	
JTAG_CPLD_TCK	P3	
JTAG_CPLD_TDO	M5	
FAN3_DIR	C14	FAN3
FAN3R_SENSOR	C15	FAN3
FAN2_SENSOR	E12	FAN2
FAN4_PRES	G15	FAN4
FAN_PWM_4	H13	FAN4
FAN4_DIR	H14	FAN4

Net name	pin number	Note
FAN4_SENSOR	J13	FAN4
FAN5_DIR	K13	FAN5
FAN4R_SENSOR	K14	FAN4
FAN_LED_G_6	L12	FAN6 LED
FAN5_SENSOR	L13	FAN5
FAN_LED_G_4	L16	FAN2 LED
FAN_PWM_6	M13	FAN6
FAN_PWM_5	M14	FAN5
FAN_LED_R_4	M16	FAN2 LED
FAN6_DIR	N13	FAN6
FAN5R_SENSOR	P14	FAN5
FAN2_PRES	C2	FAN2
FAN3_PRES	C3	FAN3
FAN1_PRES	D2	FAN1
FAN1_VENDORID_0	D3	FAN1
FAN1_VENDORID_1	E1	FAN1
FAN1_VENDORID_2	E2	FAN1
FAN2_VENDORID_0	E3	FAN2
FAN2_VENDORID_1	E4	FAN2
FAN2_VENDORID_2	E5	FAN2
FAN3_VENDORID_0	F1	FAN3
FAN3_VENDORID_1	F2	FAN3
FAN3_VENDORID_2	F3	FAN3
FAN4_VENDORID_0	F4	FAN4
FAN4_VENDORID_1	F5	FAN4
FAN4_VENDORID_2	F6	FAN4
FAN5_VENDORID_0	G1	FAN5
FAN5_VENDORID_1	G2	FAN5
FAN5_VENDORID_2	G3	FAN5
FAN6_VENDORID_0	G4	FAN6
FAN6_VENDORID_1	G6	FAN6
FAN6_VENDORID_2	H1	FAN6
FAN_SDA_1_R	M1	

Net name	pin number	Note
FAN_SCL_1	N1	

5.12.5. CPLD Field upgrade information

The system support CPLD field upgrade function for main CPLD and Fan CPLD.

5.12.5.1. JTAG connection

- Main board and Fan board

Main board CPLD have three CPLD devices; CPLD1, CPLD2 and CPLD3. Fan board has one CPLD device. The updater can update four CPLD devices in same time. CPU connects with CPLD's Jtag interface via CPU GPIO pin, and there has a JTAG chain in CPLD1, 2, 3 and Fan board CPLD.

5.12.5.2. Upgrade procedure

- Command for main board CPLD upgrade:
  - **"TFTP_server_IP" : It is the IP address of TFTP server**
  - **"file_name.updater" : It is the file name of new CPLD image updater**

ONIE: / # update_url tftp://**"TFTP_server_IP"/"file_name**.updater"

5.12.5.3. Operational mode

The real-time ISP feature present in the Max V family is used for upgrade CPLD code.

5.12.5.4. Time Required to Download New CPLD Image

It will take 20 sec for updating Main board CPLD code and 10 sec for updating Fan board CPLD code.

5.12.5.5. Power cycling requirements

The system needs a power cycle after finish CPLD code update. It will run original CPLD code before power cycle.

5.13. IDT 8V89307

5.13.1. Configurations of IDT 8V89307

Table 32 IDT 8V89307 Configurations

Pin Number	Pin Name	Function Description
J2	I2C_EN	0:SPI interface *1:I2C interface
E3	CS_B_ASEL0	6bit is fixed=>110011X ASEL0=0

		ADD[6:0]=1100110
C2 D2	DPLL1_MOD_SEL0 DPLL1_MOD_SEL1	DPLL1_MOD_SEL[0:1] 00:Manual normal 01:Manual holdover mode 10:Manual free run mode 11:Automatic normal mode

5.13.2. POR of IDT 8V89307

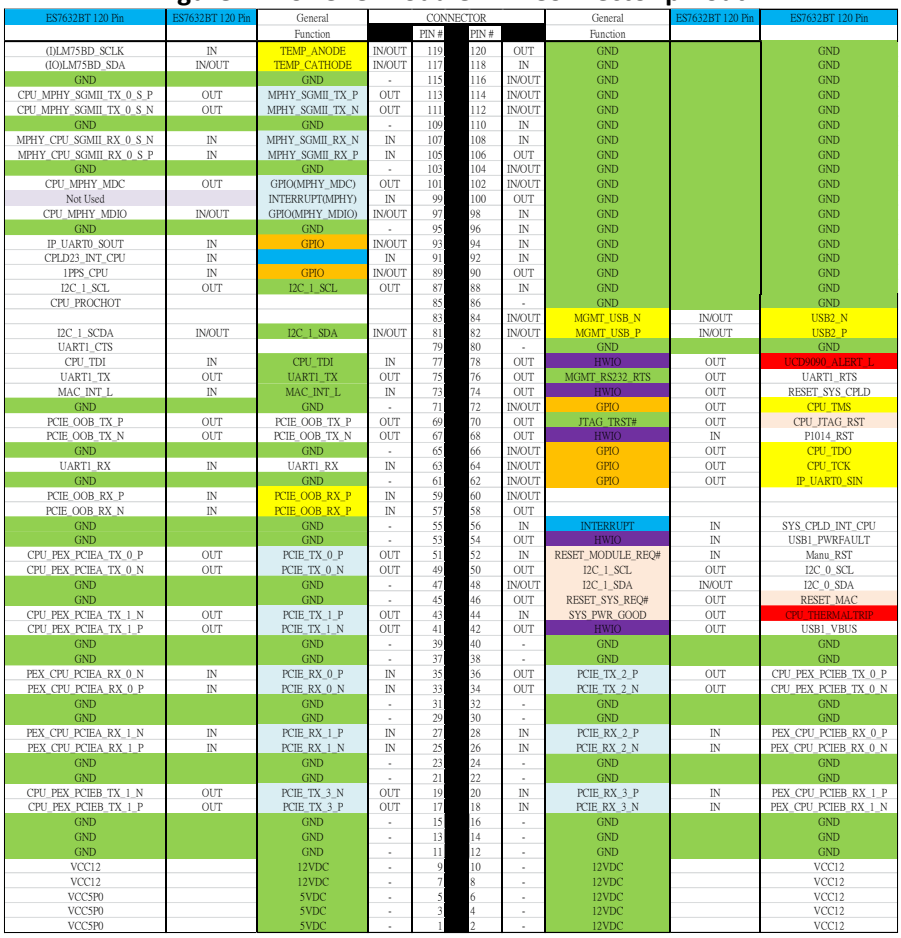
The detailed power-on reset (POR) flow is as follows:

1. 3.3V up and Ref clock up
2. Then 3.3V enable MPS1482 to generate 1.8V
3. All power are stable, POWR607 inform CPLD
4. CPLD receive the signal, CPLD assert Reset_N high

5.14. Connector

5.14.1. Connector for CPU module (CONN8)

Figure 47 For CPU module BTB Connector pinout



ES7632BT 120 Pin	ES7632BT 120 Pin	General Function	CONNECTOR PIN #		CONNECTOR PIN #		General Function	ES7632BT 120 Pin	ES7632BT 120 Pin
(I)LM75BD_SCLK	IN	TEMP_ANODE	IN/OUT	119	120	OUT	GND		GND
(IO)LM75BD_SDA	IN/OUT	TEMP_CATHODE	IN/OUT	117	118	IN	GND		GND
GND		GND	-	115	116	IN/OUT	GND		GND
CPU_MPHY_SGMII_TX_0_S_P	OUT	MPHY_SGMII_TX_P	OUT	113	114	IN/OUT	GND		GND
CPU_MPHY_SGMII_TX_0_S_N	OUT	MPHY_SGMII_TX_N	OUT	111	112	IN/OUT	GND		GND
GND		GND	-	109	110	IN	GND		GND
MPHY_CPU_SGMII_RX_0_S_N	IN	MPHY_SGMII_RX_N	IN	107	108	IN	GND		GND
MPHY_CPU_SGMII_RX_0_S_P	IN	MPHY_SGMII_RX_P	IN	105	106	OUT	GND		GND
GND		GND	-	103	104	IN/OUT	GND		GND
CPU_MPHY_MDC	OUT	GPIO(MPHY_MDC)	OUT	101	102	IN/OUT	GND		GND
Not Used		INTERRUPT(MPHY)	IN	99	100	OUT	GND		GND
CPU_MPHY_MDIO	IN/OUT	GPIO(MPHY_MDIO)	IN/OUT	97	98	IN	GND		GND
GND		GND	-	95	96	IN	GND		GND
IP_UART0_SOUT	IN	GPIO	IN/OUT	93	94	IN	GND		GND
CPLD23_INT_CPU	IN		IN	91	92	IN	GND		GND
1PPS_CPU	IN	GPIO	IN/OUT	89	90	OUT	GND		GND
I2C_1_SCL	OUT	I2C_1_SCL	OUT	87	88	IN	GND		GND
CPU_PROCHOT				85	86	-	GND		GND
				83	84	IN/OUT	MGMT_USB_N	IN/OUT	USB2_N
I2C_1_SCDA	IN/OUT	I2C_1_SDA	IN/OUT	81	82	IN/OUT	MGMT_USB_P	IN/OUT	USB2_P
UART1_CTS				79	80	-	GND		GND
CPU_TDI	IN	CPU_TDI	IN	77	78	OUT	HWIO	OUT	UCD9090_ALERT_L
UART1_TX	OUT	UART1_TX	OUT	75	76	OUT	MGMT_RS232_RTS	OUT	UART1_RTS
MAC_INT_L	IN	MAC_INT_L	IN	73	74	OUT	HWIO	OUT	RESET_SYS_CPLD
GND		GND	-	71	72	IN/OUT	GPIO	OUT	CPU_TMS
PCIE_OOB_TX_P	OUT	PCIE_OOB_TX_P	OUT	69	70	OUT	JTAG_TRST#	OUT	CPU_JTAG_RST
PCIE_OOB_TX_N	OUT	PCIE_OOB_TX_N	OUT	67	68	OUT	HWIO	IN	P1014_RST
GND		GND	-	65	66	IN/OUT	GPIO	OUT	CPU_TDO
UART1_RX	IN	UART1_RX	IN	63	64	IN/OUT	GPIO	OUT	CPU_TCK
GND		GND	-	61	62	IN/OUT	GPIO	OUT	IP_UART0_SIN
PCIE_OOB_RX_P	IN	PCIE_OOB_RX_P	IN	59	60	IN/OUT			
PCIE_OOB_RX_N	IN	PCIE_OOB_RX_P	IN	57	58	OUT			
GND		GND	-	55	56	IN	INTERRUPT	IN	SYS_CPLD_INT_CPU
GND		GND	-	53	54	OUT	HWIO	IN	USB1_PWRFAULT
CPU_PEX_PCIEA_TX_0_P	OUT	PCIE_TX_0_P	OUT	51	52	IN	RESET_MODULE_REQ#	IN	Manu_RST
CPU_PEX_PCIEA_TX_0_N	OUT	PCIE_TX_0_N	OUT	49	50	OUT	I2C_1_SCL	OUT	I2C_0_SCL
GND		GND	-	47	48	IN/OUT	I2C_1_SDA	IN/OUT	I2C_0_SDA
GND		GND	-	45	46	OUT	RESET_SYS_REQ#	OUT	RESET_MAC
CPU_PEX_PCIEA_TX_1_N	OUT	PCIE_TX_1_P	OUT	43	44	IN	SYS_PWR_GOOD	OUT	CPU_THERMALTRIP
CPU_PEX_PCIEA_TX_1_P	OUT	PCIE_TX_1_N	OUT	41	42	OUT	HWIO	OUT	USB1_VBUS
GND		GND	-	39	40	-	GND		GND
GND		GND	-	37	38	-	GND		GND
PEX_CPU_PCIEA_RX_0_N	IN	PCIE_RX_0_P	IN	35	36	OUT	PCIE_TX_2_P	OUT	CPU_PEX_PCIEB_TX_0_P
PEX_CPU_PCIEA_RX_0_P	IN	PCIE_RX_0_N	IN	33	34	OUT	PCIE_TX_2_N	OUT	CPU_PEX_PCIEB_TX_0_N
GND		GND	-	31	32	-	GND		GND
GND		GND	-	29	30	-	GND		GND
PEX_CPU_PCIEA_RX_1_N	IN	PCIE_RX_1_P	IN	27	28	IN	PCIE_RX_2_P	IN	PEX_CPU_PCIEB_RX_0_P
PEX_CPU_PCIEA_RX_1_P	IN	PCIE_RX_1_N	IN	25	26	IN	PCIE_RX_2_N	IN	PEX_CPU_PCIEB_RX_0_N
GND		GND	-	23	24	-	GND		GND
GND		GND	-	21	22	-	GND		GND
CPU_PEX_PCIEB_TX_1_N	OUT	PCIE_TX_3_N	OUT	19	20	IN	PCIE_RX_3_P	IN	PEX_CPU_PCIEB_RX_1_P
CPU_PEX_PCIEB_TX_1_P	OUT	PCIE_TX_3_P	OUT	17	18	IN	PCIE_RX_3_N	IN	PEX_CPU_PCIEB_RX_1_N
GND		GND	-	15	16	-	GND		GND
GND		GND	-	13	14	-	GND		GND
GND		GND	-	11	12	-	GND		GND
VCC12		12VDC	-	9	10	-	12VDC		VCC12
VCC12		12VDC	-	7	8	-	12VDC		VCC12
VCC5P0		5VDC	-	5	6	-	12VDC		VCC12
VCC5P0		5VDC	-	3	4	-	12VDC		VCC12
VCC5P0		5VDC	-	1	2	-	12VDC		VCC12

5.14.2. Connector for Fan board (CONN2)

Table 33 For Fan board BTB Connector pinout

Name	Type	Net Name	Description
1	Power	GND	12V/3.3V return
2	Power	GND	12V/3.3V return
3	Power	FAN_IN_3V3	3.3V Power
4	Power	FAN_IN_3V3	3.3V Power
5	Power	FAN_IN_3V3	3.3V Power

6	Power	FAN_IN_3V3	3.3V Power
7	Power	FAN_IN_12V	12V Power
8	Power	FAN_IN_12V	12V Power
9	Power	FAN_IN_12V	12V Power
10	Power	FAN_IN_12V	12V Power
11	Power	FAN_IN_12V	12V Power
12	Power	FAN_IN_12V	12V Power
13	Power	GND	12V/3.3V return
14	Power	GND	12V/3.3V return
15	OUT	Fan_idle	Enable/disable the Fan board's I2C master
16	IN	Fan_interrupt	Fan board send interrupt
17	Power	GND	12V/3.3V return
18	Power	GND	12V/3.3V return
19	IN	FAN_SCL_2	For Fan CPLD access switch board's thermal sensor
20	INOUT	FAN_SDA_1	For CPLD to access Fan CPLD status
21	INOUT	FAN_SDA_2	For Fan CPLD access switch board's thermal sensor
22	OUT	FAN_SCL_1	For CPLD to access Fan CPLD status
23	Power	GND	12V/3.3V return
24	Power	GND	12V/3.3V return
25	IN	CPLD_TMS	JTAG_TMS
26	OUT	CPLD_TDO	JTAG_TDO
27	IN	CPLD_TCK	JTAG_TCK
28	IN	CPLD_TDI	JTAG_TDI
29	Power	GND	12V/3.3V return
30	Power	GND	12V/3.3V return

5.14.3. Download connector for IR3595 (CONN1)

Table 34 For IR3595 download Connector pinout

Name	Type	Net Name	Description
1	Power	GND	Download cable GND link
2	Power	GND	Download cable GND link
3	INOUT	IR3595B_SMB_DIO_R	For burn IR3595(U23) firmware code
4	INOUT	IR3595A_SMB_DIO_R	For burn IR3595(U3) firmware code
5	OUT	IR3595B_SMB_CLK_R	For access IR3595(U23) status
6	OUT	IR3595A_SMB_CLK_R	For access IR3595(U3) status
7	IN	VEN_VCC5P0	VCC5P0 Enable signal
8	Power	GND	Download cable GND link

9	Power	GND	Download cable GND link
10	Power	GND	Download cable GND link

5.14.4. Download connector for POWR1014A (CONN3)

Table 35 For POWR1014A download Connector pinout

Name	Type	Net Name	Description
1	Power	Vstb_3V3	Standby 3.3V Power
2	IN	P1014_TDO	Output access to Download Cable
3	OUT	P1014_TDI	Input access to POWR1014A (U14)
4	NA	NA	NA
5	NA	NA	NA
6	OUT	P1014_TMS	For access POWR1014A (U14) TMS status
7	Power	GND	Standby 3.3V return
8	OUT	P1014_TCK	For access POWR1014A (U14) TCK status

5.14.5. Download connector for CPLD (U40,U47,U48) (CONN6)

Table 36 For CPLD download Connector pinout

Name	Type	Net Name	Description
1	IN	JTAG_TCK_R	For access Download Cable TCK status
2	Power	GND	Standby 3.3V return
3	IN	JTAG_TDO	Output access to Download Cable
4	Power	Vstb_3V3	Standby 3.3V Power
5	IN	JTAG_TMS_R	For access Download Cable TMS status
6	NA	NA	NA
7	NA	NA	NA
8	NA	NA	NA
9	OUT	JTAG_TDI	Input access to CPLD
10	Power	GND	Download cable GND link

5.15. PSU

The system supports 4 kinds of power module.

- AC power (Air direction : Front to back; red color panel)
- AC power (Air direction : Back to front; blue color panel)
- DC Power (Air direction : Front to back; red color panel)
- DC input Power (Air direction : Front to back; blue color panel)

Those are for difference application; the fan direction is front to back or back to front, the AC/DC Power or DC/DC power.

The AC/DC and DC/DC power are only different between power input; the output voltage SPEC is the

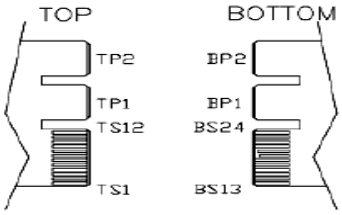
same. The AC/DC power is 90~240Vac input, and DC/DC power is 36~72Vdc input. The power supply can support load sharing function.

5.15.1. Pinout

The power module output pin define is as below.

Figure 48 PSU Pinout

3.3. **Pin assianment for DC output gold fingers**



PIN NO.	CONDITION	PIN NO.	CONDITION
TS1	PDB_FAULT	BS13	+12VS+
TS2	PRESENT	BS14	+12VRS-
TS3	A0	BS15	12LS
TS4	PDB_ALERT	BS16	SMB_ALERT
TS5	AC-OK	BS17	SDA
TS6	Reserved	BS18	SCL
TS7	Reserved	BS19	PS-KILL
TS8	Reserved	BS20	PS_ON
TS9	Reserved	BS21	PW_OK
TS10	A2	BS22	A1
TS11	+5VSB	BS23	+5VSB
TS12	+5VSB	BS24	+5VSB
TP1	GND	BP1	+12V
TP2	GND	BP2	+12V
TOP		BOTTOM	

Figure 3: signal descriptions

5.15.2. Dimension

Nominal Dimensions

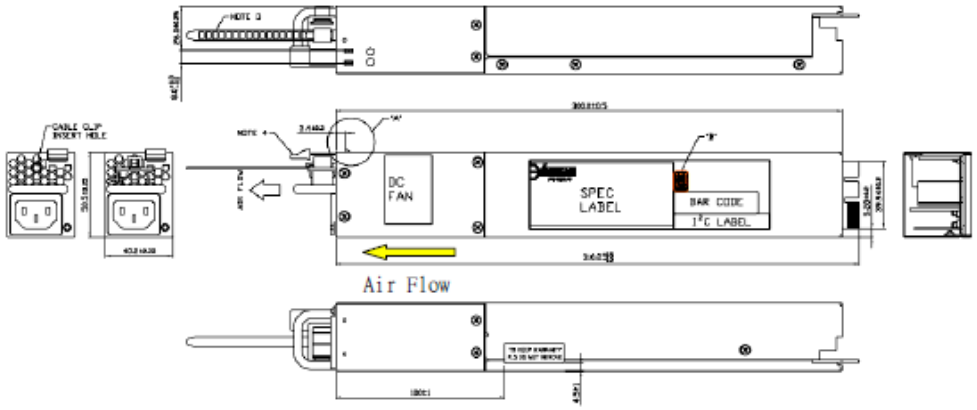
Height: 40mm (fits in 1U rack in vertical installation);

Width: 50.5mm

Depth: 310.2mm

Figure 49 PSU Dimension

The casing dimension is W 50.5 mm x L 310.2 mm x H 40 mm(including gold finger)



3.

Figure 2: Outline drawing

3.

5.15.3. Efficiency

The Efficiency should meet at least 80Plus Platinum rating, specified in the below table. The efficiency test condition should be 230VAC and with external fan power source or deduction of the power consumed by the fan at specified loading, according to 80Plus efficiency measurement specifications.

Figure 50 PSU Efficiency

(80Plus Platinum) test at 230VAC with external fan instead of self fan module.

Input	10% load	20% load	50%load	100%load
230VAC	*	90%	94%	91%
115VAC	*	*	*	*

5.15.4. Power Supply Management Controller (PSMC)

The PSMC device in the power supply shall derive its power of the +5V or +3.3V on the system side of the Oring device and shall be grounded to return. It shall be compatible with SMBus specification 2.0 and PMBusTM Power System Management Protocol Specification Part I and Part II in Revision 1.1 or later. It shall be located at the address set by the A0 and A1 pins. Refer to the specification posted on www.ssiforum.org and www.pmbus.org website for details of the power supply monitoring interface requirements and refer to followed section of supported features. The below table reflect the power module addresses complying with the position in the power system.

Figure 51 PSU PSMC Addressing

PDB position and power module address	PM1/B0h	PM2/B2h	PM3/B4h	PM4/B6h
Pin A0	0	1	0	1
Pin A1	0	0	1	1

5.15.5. Power Supply Field Replacement Unit (FRU)

The power supply shall support electronic access of FRU information over an I2C bus. Five pins at the power supply connector are allocated for this. They are named SCL, SDA, A1, A0 and Write protect. SCL is serial clock. SDA is serial data. These two bidirectional signals from the basic communication lines over the I2C bus. A0and A1 are input address lines to the power supply. The backplane defines the state of these lines such that the address to the power supply is unique within the system. The resulting I2C address shall be per table below. The Write protection pin is to ensure that data will not accidentally overwritten.
The device used for this shall be powered from a 3.3V bias voltage derived from the 5VSB output . No pull-up resistors shall be on SCL or SDA inside the power supply.

Figure 52 PSU EEPROM Addressing

A1	A0	Address
Low	Low	0xA0
Low	High	0xA2
High	Low	0xA4
High	High	0xA6

5.15.6. PSMC Sensors

Sensors shall be available to the PSMC for monitoring purpose. All Sensors shall continue to provide real time data as long as the PSMC device is powered. This means in standby and operation mode, while in standby the main output(s) of the power supply shall read zero Amps and Volts.

Table 37 PSU PSMC Sensor list

Sensor	Description
Vinput	Input Voltage
Iinput	Input Current
Pinput	Input Power
Voutput_main	Output Voltage main output
Ioutput_main	Output Current main output
Poutput_main	Output Power main output
Voutput_aux	Output Voltage auxiliary output
Ioutput_aux	Output Current auxiliary output
Poutput_aux	Output Power auxiliary output
Tcomp(TBD)	Component Temperature
Tenv	Environmental Temperature
RPMFan	Fan Speed reading
PDBfail	PDB fail protection

5.15.7. LEDs of Power Supply units

The power supply has Green/ Red led to show the power supply status.

Figure 53 PSU LEDs of Power Supply units

The LED TYPE: YCG317-EGW(R+G) or equal.

Power supply status	Power supply LED color
No AC power to all PSU	OFF
Only +5V standby output on (AC OK)	1Hz Blinking Green
Power supply DC output ON and OK	Green
Power supply fail	Red
Fan fail	1Hz Blinking Red
Power supply warning	0.5Hz Blinking Red/Green *

NOTE: * Blinking frequency: (Red and Green on 0.5 Sec and off 0.5 Sec separately and sequentially in two seconds)

5.16. Power Consumption

The total estimated power budget described is ~602W on the 48 x 25G、8 x 100G switchboard with CPU system.

All calculating data are based on the maximum power dissipation in the spec of components. Combining the real measurement of simulated projects, the total power is less than this estimation by 1/4 ~ 1/3.

Figure 54 Power Consumption Table

Power Consumption Estimation Table / CURRENT (max) per device (A)																
Voltage(V) / Device	12	5	3.3	2.5	0.6	1.8	1.7	1.5	1.3	1.2	1.05	ROV 0.8	ROV 0.8	Quantity	Unility(%)	Total(W)
BDXDE			0.487			26	0.35	0.162	0.5	3	11.283			1		65.34225
BCM56873			0.3			0.5				1.8		194.5	18.85	1		174.73
BCM54616S			0.083							0.2				1		0.5139
DDR4				0.5	0.75					2.176				2		8.6224
SPI Flash			0.05											4		0.66
PS2251-50		0.153												1		0.765
NAND Flash		0.5												1		2.5
CPLD			0.5											4		6.6
SFP28 (SR)			0.6											48		95.04
QSFP28 (SR4)			1.5											8		39.6
SFP+			0.5											2		3.3
USB		0.5												1		2.5
FAN	1.8													6		129.6
M.2 SSD 32G			0.487											1		1.6071
BCM5720			0.359											1		1.1847
MISC.			0.2											1		0.66
BMC Module		0.1	0.8											1		3.14
LEDs(for 25G, 100G & system)			0.02											84		5.544
Power moniter			0.1											1		0.33
Total Current(mA)	10.8	1.253	48.496	1	1.5	26.5	0.35	0.162	0.5	9.352	11.283	194.5	18.85			542.2394
Voltage Toleration(%)	5%		5%							5%		3%	3%			
Efficiency(%)																602.4882

6. PCB

There include PCB information of stack-up, dimension and placement.

6.1. Stack-up

The Switch board PCB material is the ultra-low loss material for High speed signal. The PCB has 14 layers and power plane has 2oz for high current application.

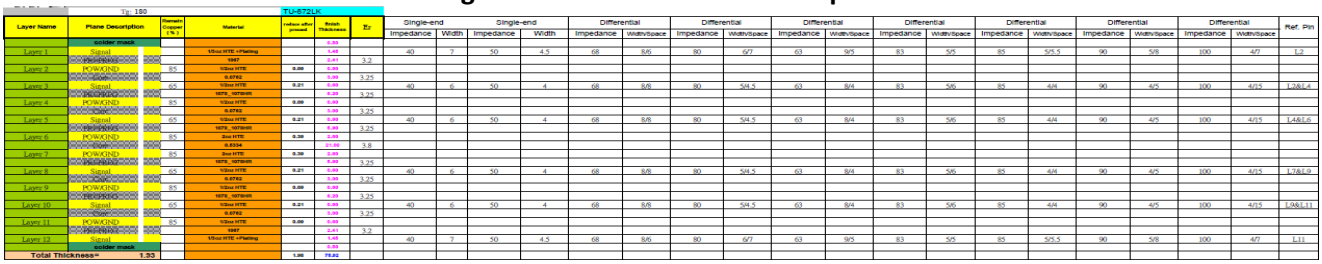
Figure 55 Switch board PCB Stackup

Accton Tech 14 Layer Stack up Proposal

			Customer Requirement								HCS Proposal (04/08/2014)																		
				SE 50 ohms	DIFF 90ohms		DIFF 92ohms		DIFF 100ohms									For Reference		SE 50 ohms	DIFF 90ohms		DIFF 92ohms		DIFF 100ohms	
Layer #	A/W Code	Type	Cu Thickness (mil)	Linewidth (mils)	Linewidth (mils)	Airgap (mils)	Linewidth (mils)	Airgap (mils)	Linewidth (mils)	Airgap (mils)	Estimated Thickness (um)	Cu Weight (oz)	Copper Foil type	roughness S-side/M-side(um)	Estimated Thickness (Mils)	Estimated Layer Cu Ratio (%)	Construction	Dk @ 1 GHz	Df @ 1 GHz	Dk @ 10 GHz	Df @ 10 GHz	Line width (mils)	Line width (mils)	Air-gap (mils)	Line width (mils)	Air-gap (mils)	Line width (mils)	Air-gap (mils)
		Soldermask	1								25				1.0														
1	TOP	0.5oz Cu Foil+	1.7	8.75	8	7.5	7	6.5	6.5	8	48		MW-G	0.25/4.5	1.9	20%						8.5	7.2	4.8	7.1	4.9	6.2	5.8
		Prepreg									107				4.2		3313HR	3.75	0.0030	3.72	0.0046								
2	GND	1.0 oz Cu	1.3	REFERENCE LAYER							32	1.0	MLS-G	5/3	1.3	80%						REFERENCE LAYER							
	Core 1	CORE									102				4.0		3313	3.83	0.0031	3.81	0.0047								
3	S	0.5 oz Cu	0.6	4.5	5.5	9.5	5	8.5	4.5	8.5	16	0.5	MLS-G	3/3	0.6	20%						6.6	7.0	6.0	6.8	6.2	5.7	6.3
		Prepreg									326				12.8		3313HR*3	3.75	0.0030	3.72	0.0046								
4	GND	1.0 oz Cu	1.3	REFERENCE LAYER							32	1.0	MLS-G	5/3	1.3	80%						REFERENCE LAYER							
	Core 2	CORE									102				4.0		3313	3.83	0.0031	3.81	0.0047								
5	S	0.5 oz Cu	0.6	4.5	5.5	9.5	5	8.5	4.5	8.5	16	0.5	MLS-G	3/3	0.6	20%						6.6	7.0	6.0	6.8	6.2	5.7	6.3
		Prepreg									326				12.8		3313HR*3	3.75	0.0030	3.72	0.0046								
6	GND	1.0 oz Cu	1.3	REFERENCE LAYER							32	1.0	MLS-G	5/3	1.3	80%						REFERENCE LAYER							
	Core 3	CORE									127				5.0		1 x 2116	3.85	0.0031	3.82	0.0047								
7	V	2.0 oz Cu	2.6	REFERENCE LAYER							66	2.0	MLS-G	8.5/3	2.6	80%						6.50	--	--	--	--	4.73	8.27
		Prepreg									317				12.5		3313HR*3	3.75	0.0030	3.72	0.0046								
8	V	2.0 oz Cu	2.6	REFERENCE LAYER							66	2.0	MLS-G	8.5/3	2.6	80%						6.50	--	--	--	--	4.73	8.27
	Core 5	CORE									127				5.0		1 x 2116	3.85	0.0031	3.82	0.0047								
9	GND	1.0 oz Cu	1.3	REFERENCE LAYER							32	1.0	MLS-G	5/3	1.3	80%						REFERENCE LAYER							
		Prepreg									326				12.8		3313HR*3	3.75	0.0030	3.72	0.0046								
10	S	0.5 oz Cu	0.6	4.5	5.5	9.5	5	8.5	4.5	8.5	16	0.5	MLS-G	3/3	0.6	20%						6.6	7.0	6.0	6.8	6.2	5.7	6.3
	Core 6	CORE									102				4.0		3313	3.83	0.0031	3.81	0.0047								
11	GND	1.0 oz Cu	1.3	REFERENCE LAYER							32	1.0	MLS-G	5/3	1.3	80%						REFERENCE LAYER							
		Prepreg									326				12.8		3313HR*3	3.75	0.0030	3.72	0.0046								
12	S	0.5 oz Cu	0.6	4.5	5.5	9.5	5	8.5	4.5	8.5	16	0.5	MLS-G	3/3	0.6	20%						6.6	7.0	6.0	6.8	6.2	5.7	6.3
	Core 7	CORE									102				4.0		3313	3.83	0.0031	3.81	0.0047								
13	GND	1.0 oz Cu	1.3	REFERENCE LAYER							32	1.0	MLS-G	5/3	1.3	80%						REFERENCE LAYER							
		Prepreg									107				4.2		3313HR	3.75	0.0030	3.72	0.0046								
14	BOT	Cu Foil+platin	1.7	8.75	8	7.5	7	6.5	6.5	8	48		MW-G	0.25/4.5	1.9	20%						8.5	7.2	4.8	7.1	4.9	6.2	5.8
		Soldermask	1								25				1.0														
Requested thickness			3.0mm								3.03	mm			119.2	mils (Soldermask to soldermask over copper)													

The CPU board PCB material is the low loss material for High speed signal. The PCB has 12 layers and power plane has 2oz for current application.

Figure 56 CPU board PCB Stackup



Layer Name	Plane Description	Remain Copper (%)	Material	Yellow after pressed	Finish Thickness	Er	Single-end Impedance	Single-end Width	Single-end Impedance	Single-end Width	Differential Impedance	Differential Width/Space	Differential Impedance	Differential Width/Space	Differential Impedance	Differential Width/Space	Differential Impedance	Differential Width/Space	Differential Impedance	Differential Width/Space	Differential Impedance	Differential Width/Space	Ref. Pin
	solder mask				0.02																		
Layer 1	Signal		1/0oz HTE +Plating		0.48		40	7	50	4.5	68	8/6	80	6/7	63	9/5	83	5/5	85	5/5.5	90	5/8	100	4/7	L2
	POWGND		1oz	0.06	0.43	3.2																			
Layer 2	POWGND	85	0.0762		0.30																				
	Signal	65	1/0oz HTE	0.21	0.50	3.25	40	6	50	4	68	8/8	80	5/4.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	L2&L4
Layer 3	POWGND		1070_1070GR		0.30																				
	POWGND	85	0.0762	0.06	0.30	3.25																			
Layer 4	Signal	65	1/0oz HTE	0.21	0.50	3.25	40	6	50	4	68	8/8	80	5/4.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	L4&L6
Layer 5	POWGND		1070_1070GR		0.30																				
	POWGND	85	2oz HTE	0.36	0.80	3.8																			
	POWGND		0.0334		21.00																				
Layer 6	POWGND	85	2oz HTE	0.36	0.80	3.25																			
	Signal	65	1/0oz HTE	0.21	0.50	3.25	40	6	50	4	68	8/8	80	5/4.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	L7&L9
Layer 7	POWGND		0.0762		0.30																				
	POWGND	85	1/0oz HTE	0.06	0.30	3.25																			
Layer 8	Signal	65	1070_1070GR		0.30		40	6	50	4	68	8/8	80	5/4.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	L8&L10
Layer 9	POWGND		0.0762		0.30																				
	POWGND	85	1/0oz HTE	0.06	0.30	3.25																			
Layer 10	Signal	65	1070_1070GR		0.30		40	6	50	4	68	8/8	80	5/4.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	L9&L11
	POWGND		0.0762		0.30																				
Layer 11	POWGND	85	1/0oz HTE	0.06	0.30	3.25																			
	POWGND		1oz		0.41	3.2																			
Layer 12	Signal		1/0oz HTE +Plating		0.48		40	7	50	4.5	68	8/6	80	6/7	63	9/5	83	5/5	85	5/5.5	90	5/8	100	4/7	L11
	solder mask				0.02																				
Total Thickness=	1.93			1.00	79.02																				

The Fan PCB is 4 layers

6.2. Dimension

The Switch PCB dimension is 418.7 x 249 mm.

Figure 57 Switch board PCB Dimension

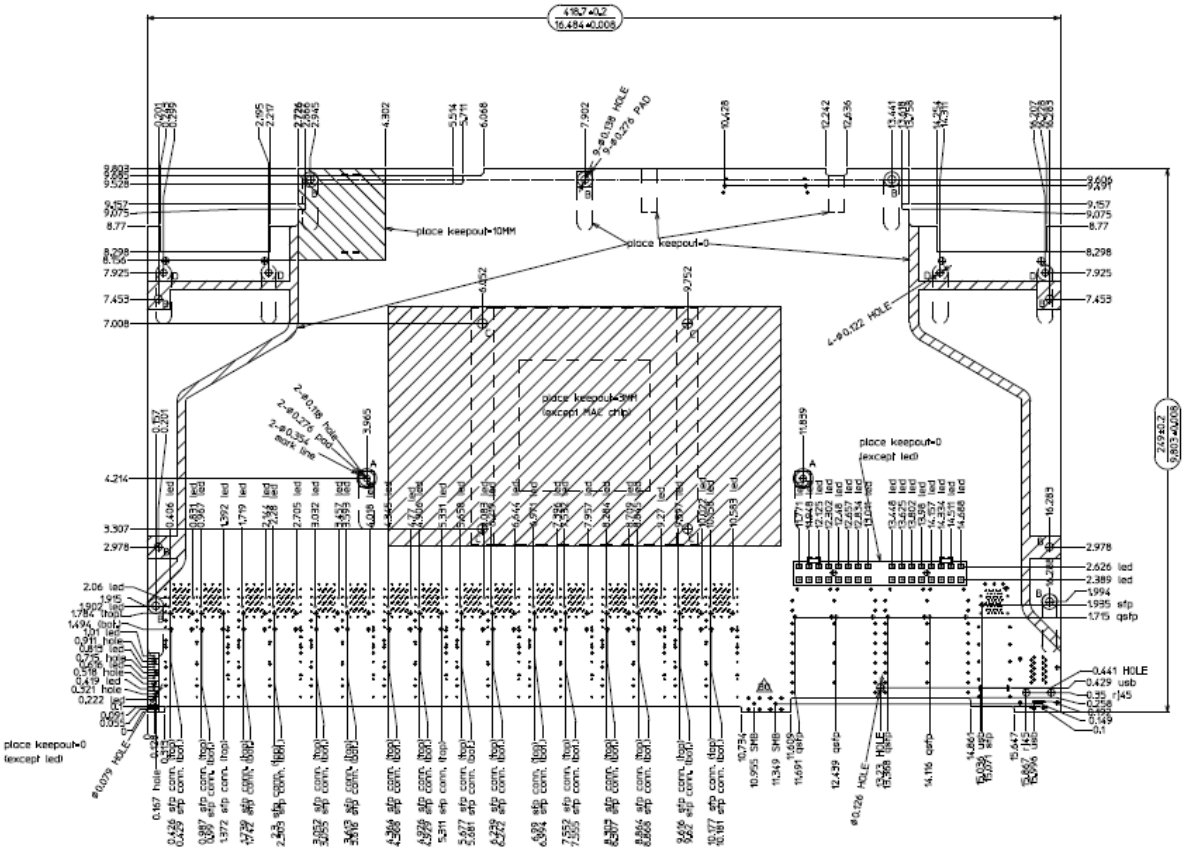
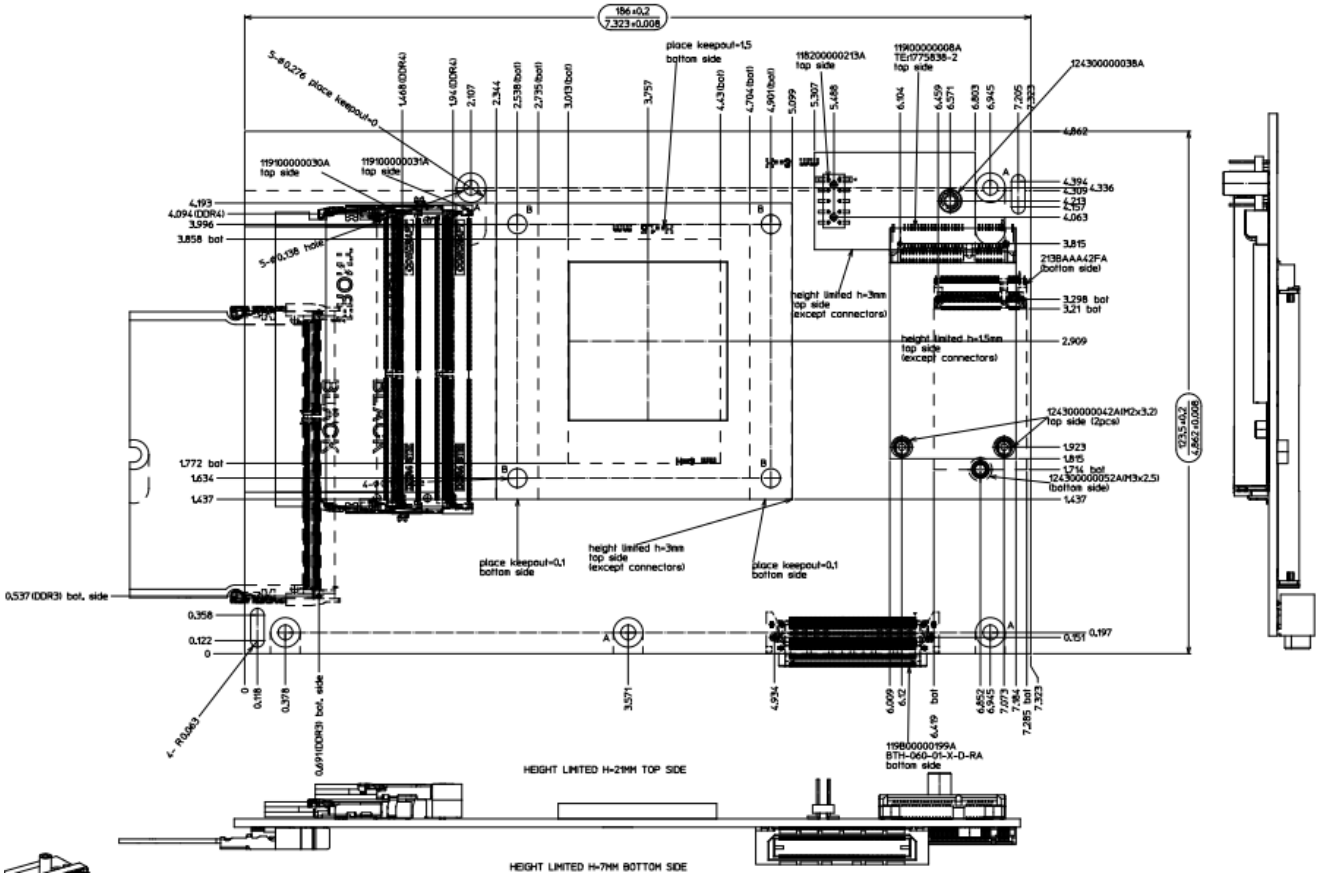
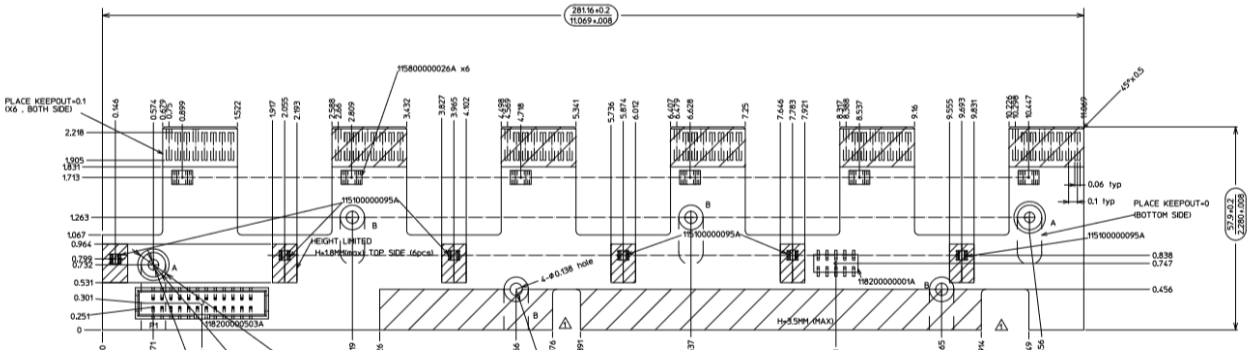


Figure 58 CPU board PCB Dimension



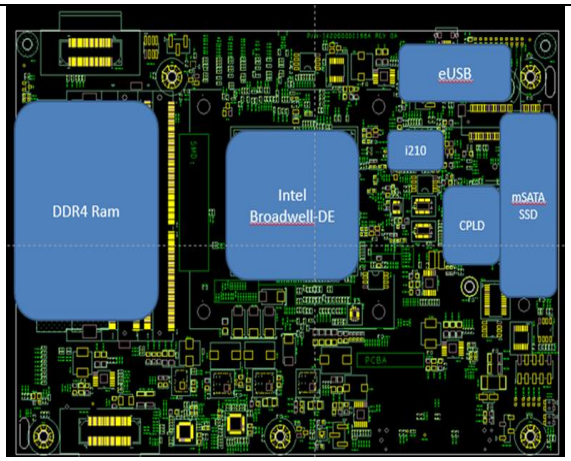
Fan PCB Dimensions



6.3. Placement

Figure 59 CPU board - PCB Placement

Top



Bottom

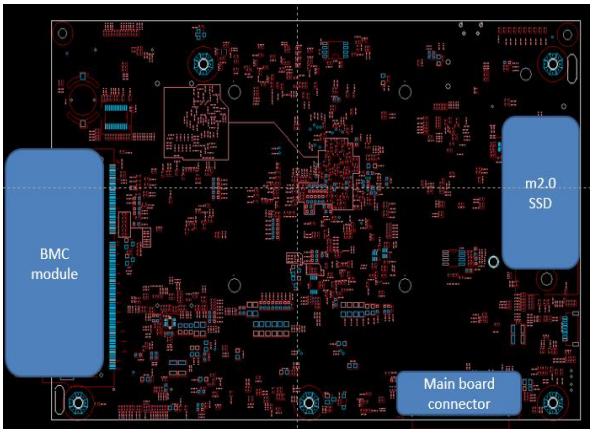
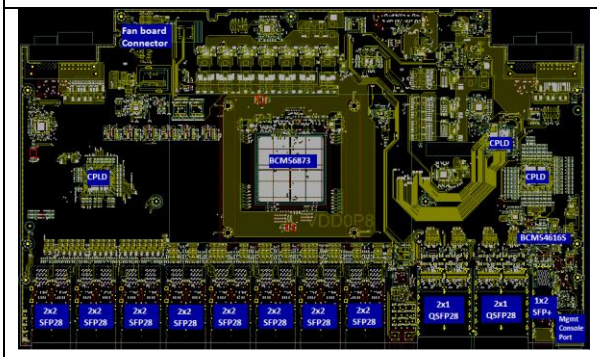
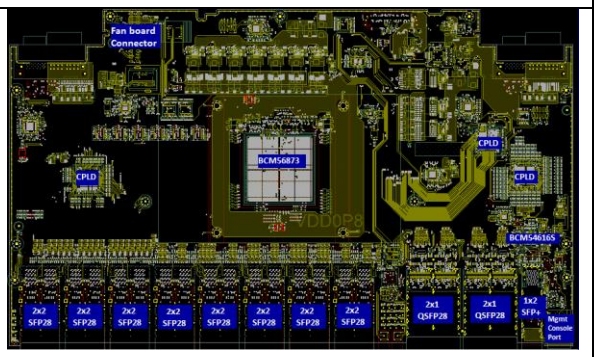


Figure 60 Switch board - PCB Placement

Top	Bottom
	

7. Mechanical

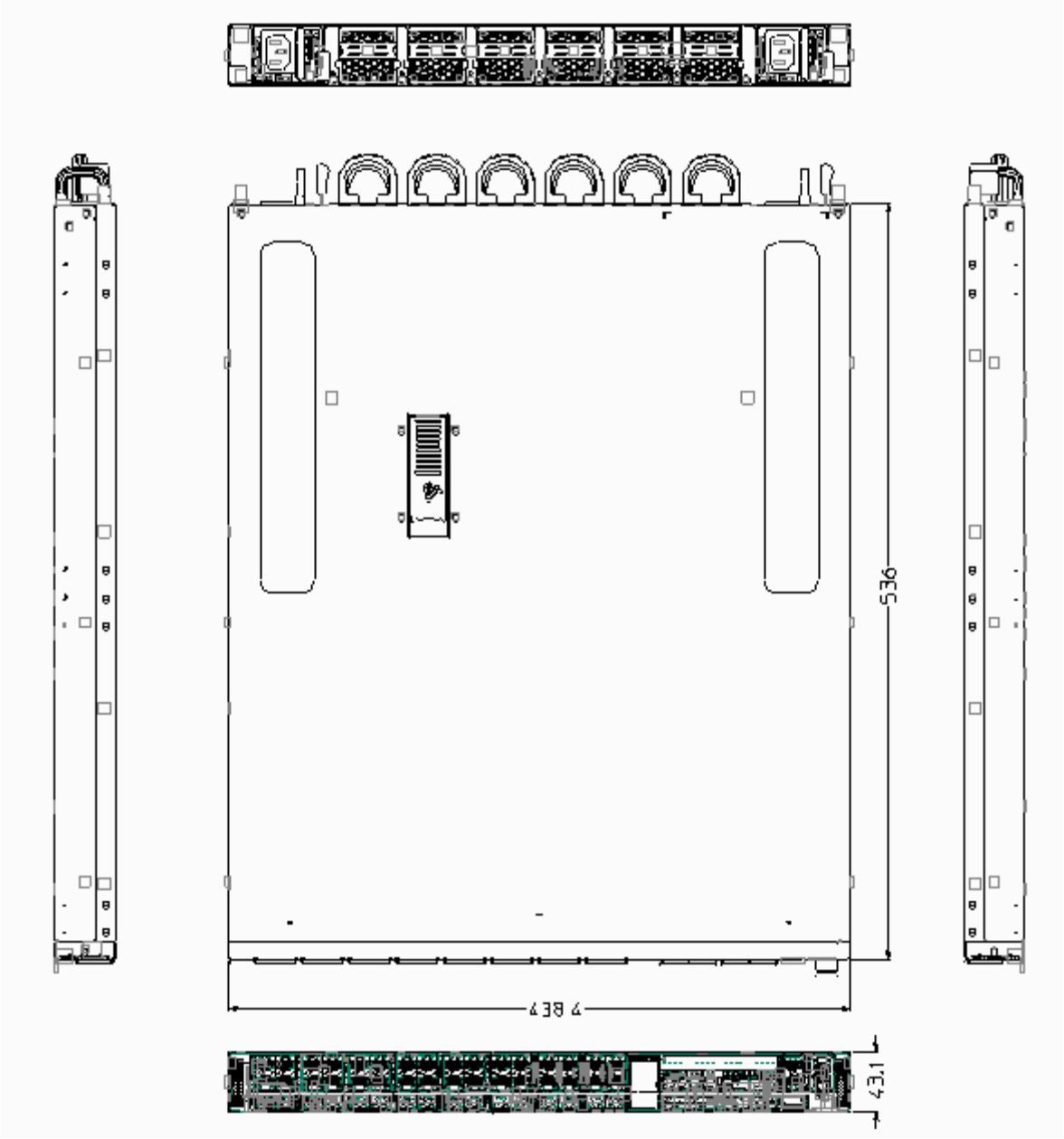
7.1. Dimension

Height: 43.25mm(maximum)

Width: 438.4mm

Depth: 536mm

Figure 61 Mechanical Dimension



7.2. Placement

Figure 62 Mechanical Placement (Top)

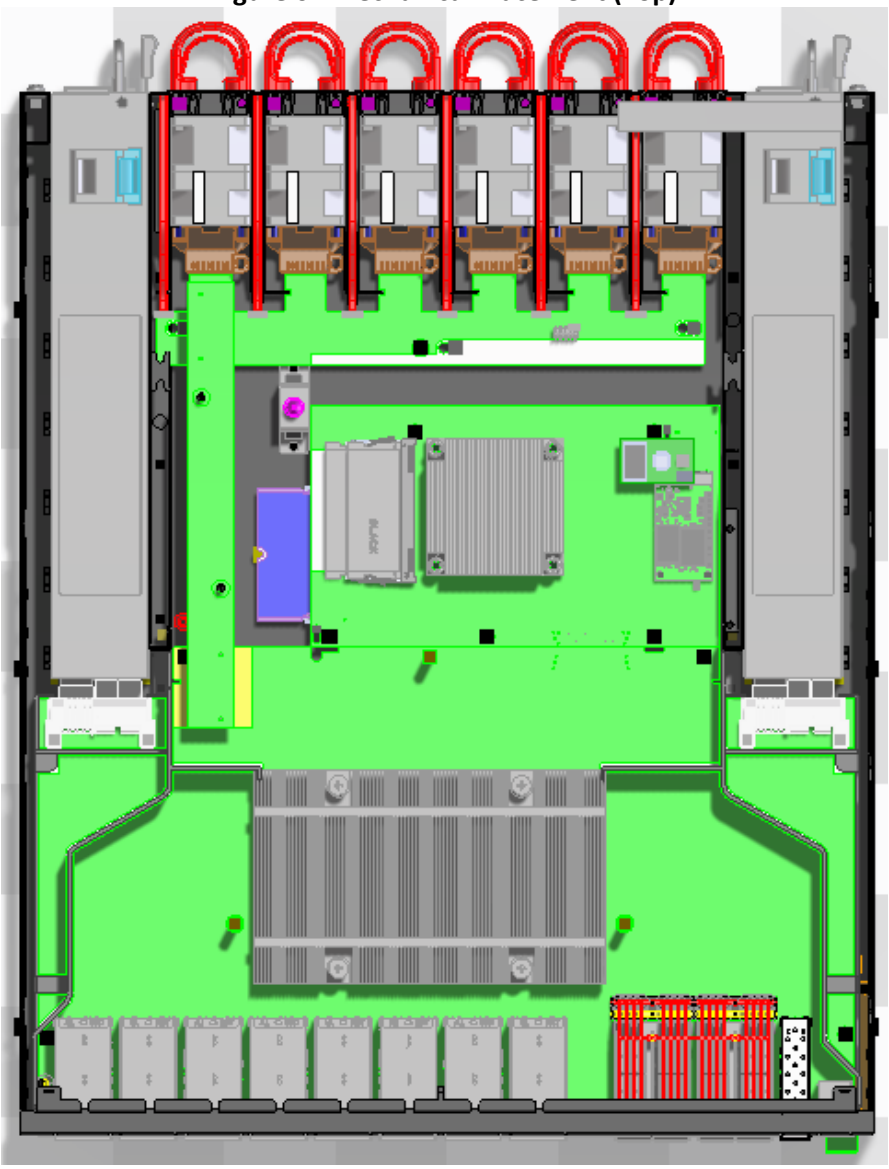
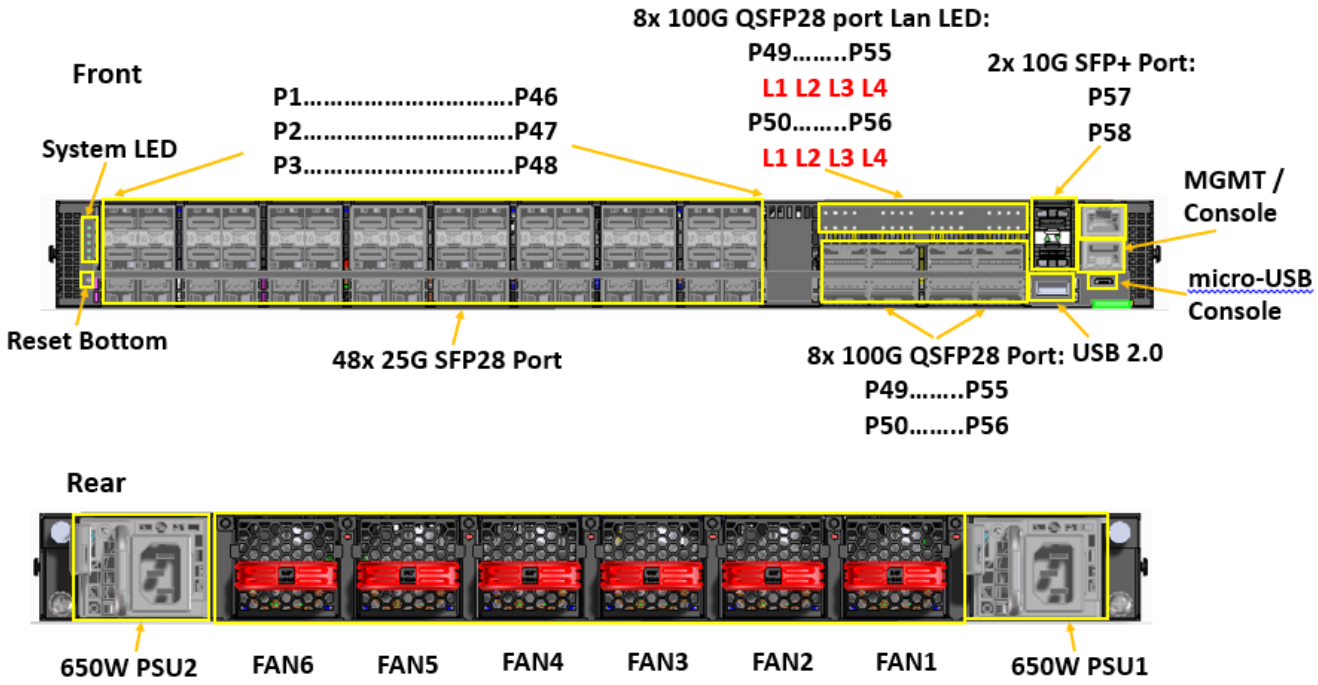


Figure 63 System Front/Rear Placement



7.3. Cooling Method

7.3.1. Fan module

The Fan board has a CPLD to do the fan controller function. The CPLD on the Fan board can control the Fan's PWM signal for adjust Fan speed and count the Fan's Tach signal for Fan speed reporting. CPU can read the thermal sensor to get thermal information, and then adjust Fan speed to reduce system's thermal. The Fan's CPLD had included I2C thermal watchdog to avoid system shutdown. If the register count to zero, the Fan speed will be set to high speed.

The CPLD information is "CPLD 5M1270ZF256C5N 3.3V FBGA256 LT/LF ALTERA"

- Front to Back Fan module with red color handle
- Back to Front Fan module with blue color handle

Table 38 Fan Module Speed

	F2B	B2F
Main source	19500 R.P.M 22500 R.P.M	22500 R.P.M 19500 R.P.M
Second source	22100 R.P.M 21400 R.P.M	21400 R.P.M 22100 R.P.M

Figure 64 Fan Tray Design Concept

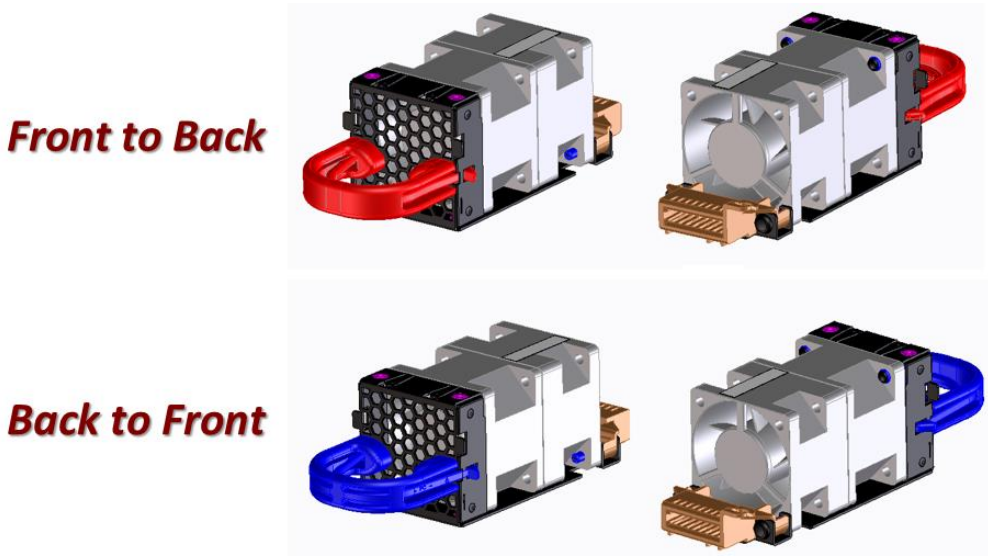


Figure 65 Fan Speed information

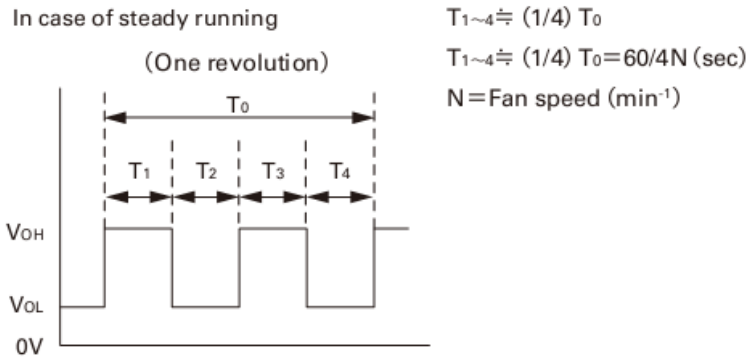
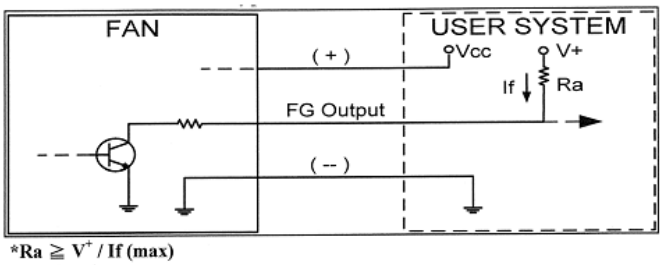
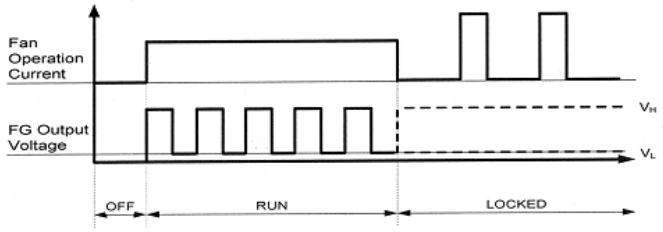


Figure 66 Fan failed information



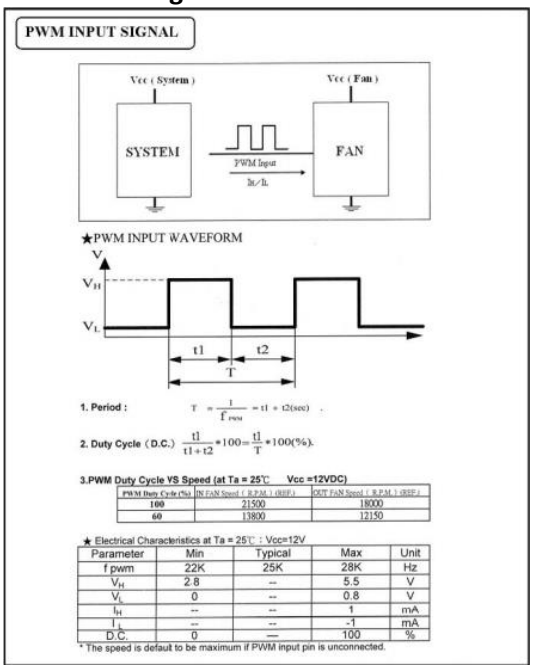
*Ra ≧ V+ / If (max)



★Electrical Characteristics ：(at Ta = 25℃, V_{CC}=12V)

Parameter	Ratings			Unit
	min	typ.	max	
FG Supply Voltage(V+)	3	--	13.2	Voltage
FG Output Current (If)	--	--	5	mA
FG Output (VL)	0	--	0.5	Voltage
FG Output (VH)	--	V+	--	Voltage

Figure 67 Fan PWM



The system only can provide 3.3V PWM signal. The min of Vh of fan need be low than 3.3V.

Software Support

The AS7326-56X supports a base software package composed of the following components:

BIOS support

The AS7326-56X Supports AMI AptioV BIOS version A01 or greater with the x86 CPU module

ONIE

See https://github.com/opencomputeproject/onie/tree/master/machine/accton for the latest supported version

Open Network Linux

See http://opennetlinux.org/ for latest supported version

8. Specifications and Standards

8.1. Safety

- UL (CAN/CSA 22.2 No 60950-1 & UL60950-1)
- CB (IEC/EN60950-1)
- CCC (GB4943.1-2011)
- BSMI (CNS14336-1)

8.2. Electromagnetic Compatibility

- CE Mark
  - EN55032 Class A
  - EN55024 (Immunity) for Information Technology Equipment
  - EN 61000-3-3
  - E N 61000-3-2
- FCC Title 47, Part 15, Subpart B Class A
- VCCI Class A
- CNS 13438 (BSMI) → by Request
- CCC (GB9254-2008) → by Request

8.3. Environmental

- Low-Temperature Exposure and Thermal Shock (packaged) : NEBS GR63-CORE ISSUE 4 , Section 4.1.1.1
- High Relative Humidity Exposure (Packaged) : NEBS GR63-CORE ISSUE 4 , Section 4.1.1.2
- High-Temperature Exposure and Thermal Shock (Packaged) : NEBS GR63-CORE ISSUE 4 , Section 4.1.1.3
- Operating Temperature and Relative Humidity : NEBS GR63-CORE ISSUE 4 , Section 4.1.2
- Altitude : NEBS GR63-CORE ISSUE 4 , Section 4.1.3
- Handling Drop Tests -Packaged Equipment : NEBS GR63-CORE ISSUE 4 , Section 4.3.1.1
- Unpackaged Equipment -Drop Tests (All Equipment) : NEBS GR63-CORE ISSUE 4 , Section 4.3.2
- Earthquake (10U Rack) : NEBS GR63-CORE ISSUE 4 , Section 4.4.1 (Zone4)
- Office Vibration Test Procedure; 90 minutes/axis (Stand & 42U Rack) : NEBS GR63-CORE ISSUE 4 , section 4.4.4
- Transportation Vibration-Packaged Equipment : NEBS GR63-CORE ISSUE 4 , section 4.4.5
- Acoustic noise : NEBS GR63-CORE ISSUE 4 , section 4.6
- Bump : IEC60068-2-29- packaged
- Shock : ETSI EN 300 019-2-3 -Operational Tests, Class T3.2 op

8.4. ROHS (6/6) Requirement

Restriction of Hazardous Substances (6/6):
Compliance with Environmental procedure 020499-00, primarily focused on Restriction of Hazardous Substances (ROHS Directive 2002/95/EC) and Waste Electrical and Electronic Equipment (WEEE Directive 2002/96/EC).

8.5. WEEE Standards

The switches complied with the following WEEE standards:
Waste Electrical and Electronic Equipment (WEEE Directive 2002/96/EC)

8.6. IEEE Standards

- IEEE 802.3ba 40G/25GBASE
- IEEE 802.3bm next generation 40G/25G Optical Ethernet
- IEEE P802.bj 100 Gb/s & FEC support

8.7. Internet Standards

- SFF-8431 SFP+ 10 Gb/s and Low Speed Electrical Interface
- SFF-8436 QSFP+ 10 Gb/s 4X Pluggable Transceiver
- SFF-8635 QSFP+ 10 Gb/s 4X Pluggable Transceiver Solution
- SFF-8665 QSFP+ 28 Gb/s 4X Pluggable Transceiver Solution