EDGECORE Networks Corporation

Edgecore AS9700-32X

Switch Specification

Revision 1.2

OPEN

Compute Project

Revision History

Revision	Date	Author	Description
1.0	3/13/2018	Jeff Catlin	Initial Release
1.1	3/24/2018	Jeff Catlin	Minor clean up
1.2	9/19/2018	Jeff Catlin	SKU Model number update

Contents

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	AS9700-32X
CPU	Intel Broadwell-DE, 4 Core
FLASH	SPI FLASH 128MB x 2
RAM	DDR4 8GB x2 SO-DIMM (expandable up to 32GB, w/I ECC
SSD	M.2 SSD 100GB x 1, mSATA SSD 100GB x 1 (option) (Support from 32GB to 256GB)
MAC	Broadcom BCM56980 (Tomahawk III)
Ethernet Port	400G QSFP56-DD port x 32 10G SFP+ port x 2 (Auxiliary port)
EMP PHY	Broadcom BCM54616S
Management Port	RJ45 port x 1
Console	RJ45 type RS232 x 1
USB	Type-A USB 2.0 port x 1
CPLD	Controlled by CPU I2C, field upgradeable
TPM Module	ST33ZP24AR28PVSP
Port LED (QSFP56-DD)	Four LED per port
Port LED (SFP+)	One bi-color LEDs per port
Push Button	One push button for reset at front panel
PTP Clock	1PPS and 10MHz SMB connector output
PCB	Switch mainboard, 413/5mm x 269mmx4.0mm, 24 Layers CPU board, 210mm x 123.5mmx2.0mm, 12 Layers Fan board, 281 x 57.9mmx2.36mm, 4 Layers
Mechanical Dimension	17.25" x 21.1" x 1U
PSU	Redundant/hot swappable 1300W AC/DC PSU
System Cooling	6 fan-tray modules with 40mm x40mm x 56mm 12V fans, hot-swappable

	AS9700-32X
System Air Flow	AFO/AFI(Note.)

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Scope

This document outlines the technical specifications for the Edgecore AS9700-32X Open Switch Platform submitted to the Open Compute Foundation.

Overview

This document describes the technical specifications of the AS9700-32X Leaf/Spine switch designed by Edgecore Networks Corporation. The AS9700-32X is a cost optimized switch design focused on Leaf/Spine deployments which support 400/100G. The AS9700-32X switch supports thirty-two QSFP-DD ports that each can operate at 10/25/40/50/100/200/400G modes of operation (different per port configurations supported based upon speed selected).

The AS9700-32X is a PHY-Less design with the QSFP28-DD connections directly attaching to the Serdes interfaces of the Broadcom 56980 switching silicon providing the lowest cost, latency, and power. The AS9700-32X supports traditional features found in Top of Rack / Leaf / Spine switches such as:

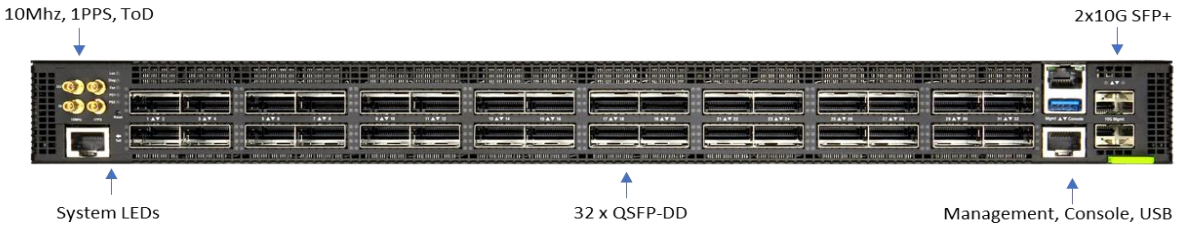
- Redundant field replaceable power supply and fan units
- Support for “Front to Back” or “Back to Front” air flow direction
- The AS9700-32X supports various Open Source CPU modules offered by Edgecore Networks which include the following:
    - Atom based C2538 based CPU module made publicly available through the OCP accepted AS7712-32X design

http://files.opencompute.org/oc/public.php?service=files&t=3d2271fd0e40a66725a747030487d571

    - Xeon based D-1518 based CPU module made publicly available through the OCP accepted AS7800-64X design and referenced in this specification

http://files.opencompute.org/oc/public.php?service=files&t=d2b4bfed8dfc024a1f2ece0db57118ee

The AS9700-32X is a 1RU design that supports standard 19” rack deployments as well as standard 21” Open Rack deployments with the ORSA-1RU.



1. Introduction

AS9700-32X is 1U high and 536mm deep, with Broadcom Tomahawk III chipset. The physical layer will consist of 32 port 400G QSFP56-DD ports and 2 port SFP+ 10G ports. The switch has a nominal operating temperature range from 0 to +45 degree C.

The following are key features of AS9700-32X:

- Redundant and hot-swappable 1300W PSU (1+1)
- Redundant and hot swappable fans (5+1)
- 32 port QSFP56-DD 400G ports
- 2 port SFP+ 10G ports management port
- 1 x RJ45 10/100/1G GE management port
- CPU Intel
  - Broadwell-DE x86 4~8 cores 2.2GHz CPU
  - Denverton 4 cores 2.4GHz
- 1 x Type-A USB port
- 1 x RJ45 console port
- 1588 and Sync-E
- System LED & Reset button

1.1. Reference Documents

Broadcom **BCM56980** Data Sheet
Intel **BDXDE** Data Sheet
Intel Denverton Datasheet
IDT**82P33731** WANPLL Data Sheet

1.2. Acronyms and Terminology

POR Power On Configuration
PSUPower Supply Unit

2. Hardware Architecture

2.1. Overview

AS9700-32X provides 32 x 400G QSFP56-DD and 2 x 10G SFP+ network ports. It also supports one 1G RJ-45 port, RJ-45 Console port, and USB port.

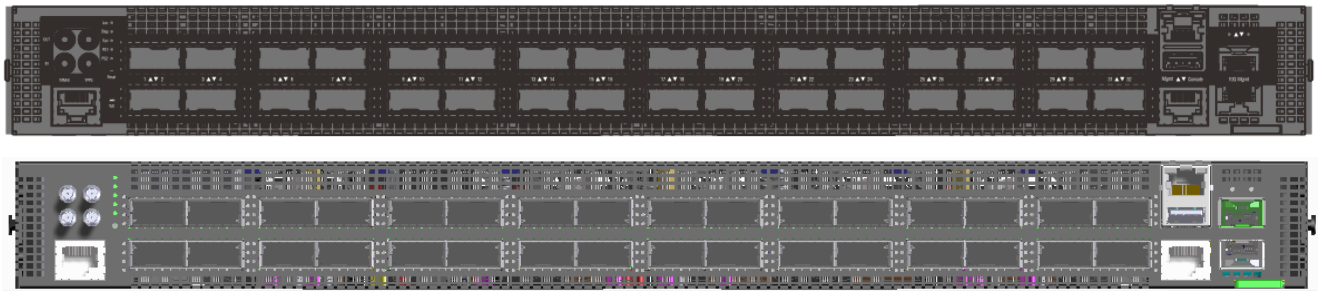


Figure 2-1 AS9716-32X Front Panel

Figure 2-2 AS9716-32X Rear Panel

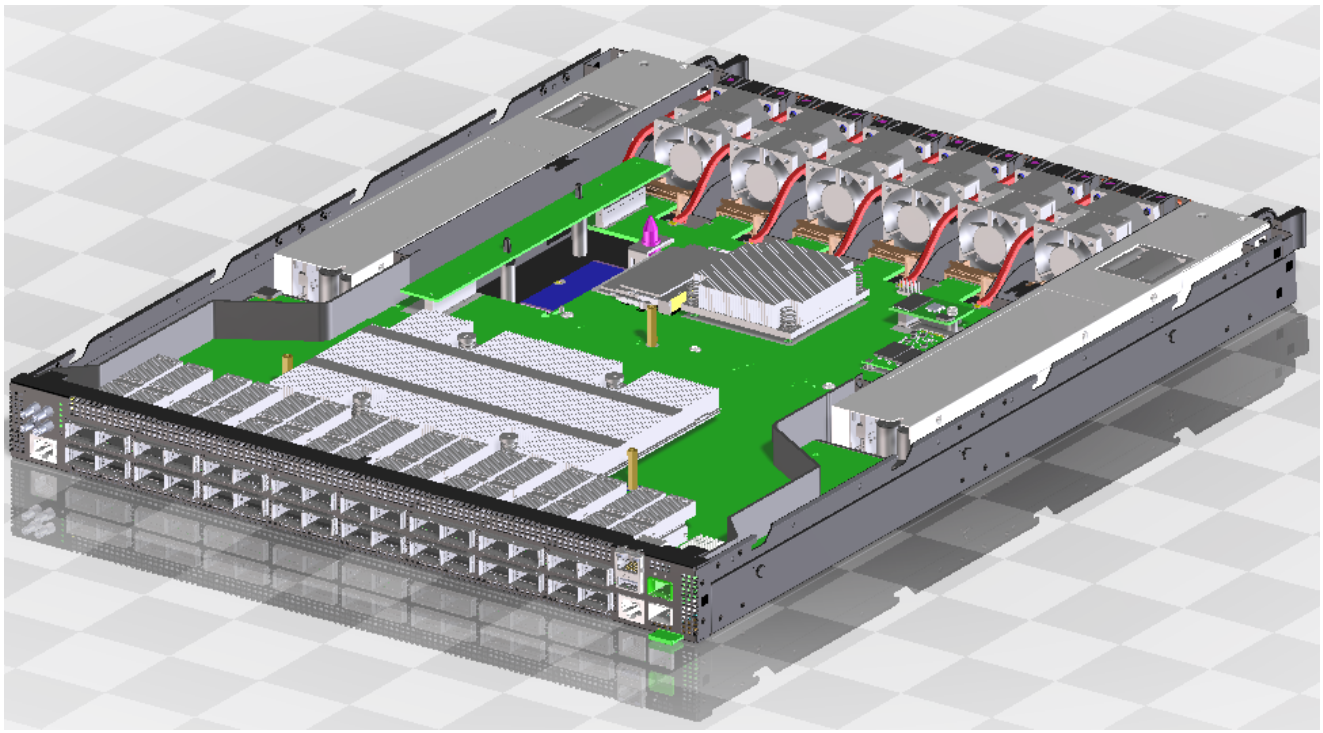


Figure 2-3 AS9716-32X placement

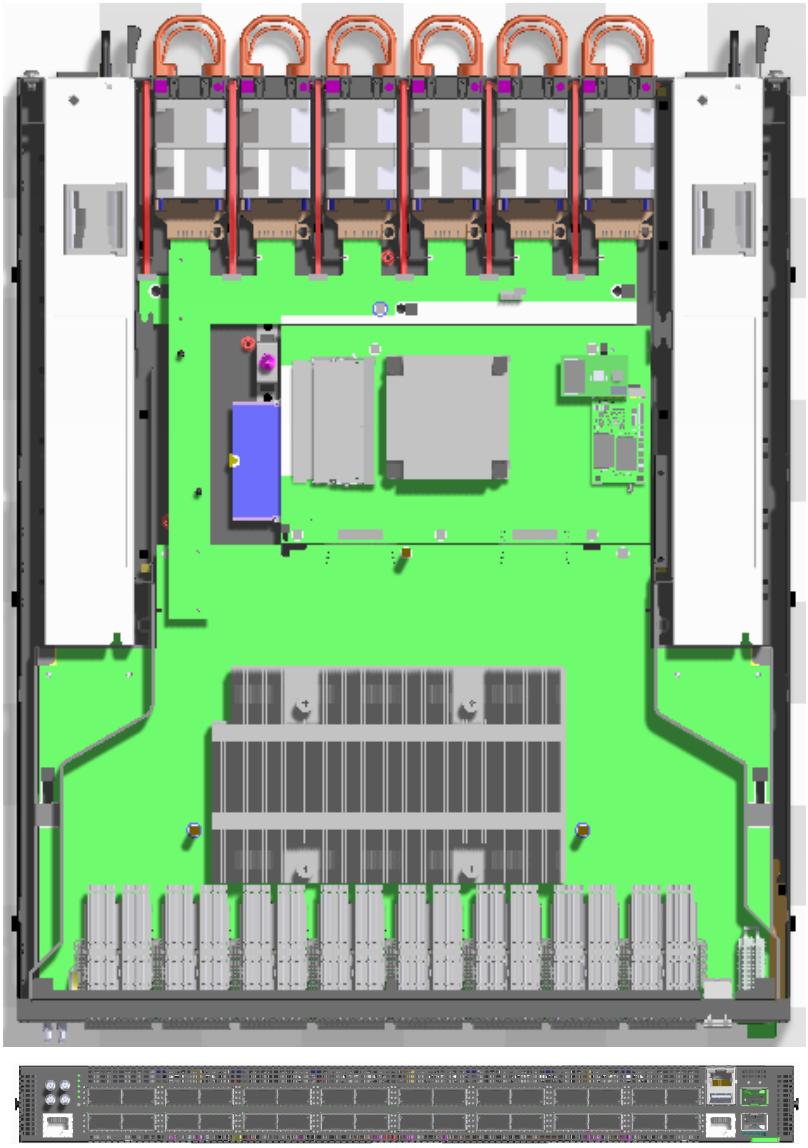


Figure 2-4 AS9716-32X top view

Figure 2-5 AS9716-32X Cover

	AS9700-32X
CPU	Intel Broadwell-DE, 4 Core
FLASH	SPI FLASH 128MB x 2
RAM	DDR4 8GB x2 SO-DIMM (expandable up to 32GB, w/I ECC
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Port LED (SFP+)	One bi-color LEDs per port
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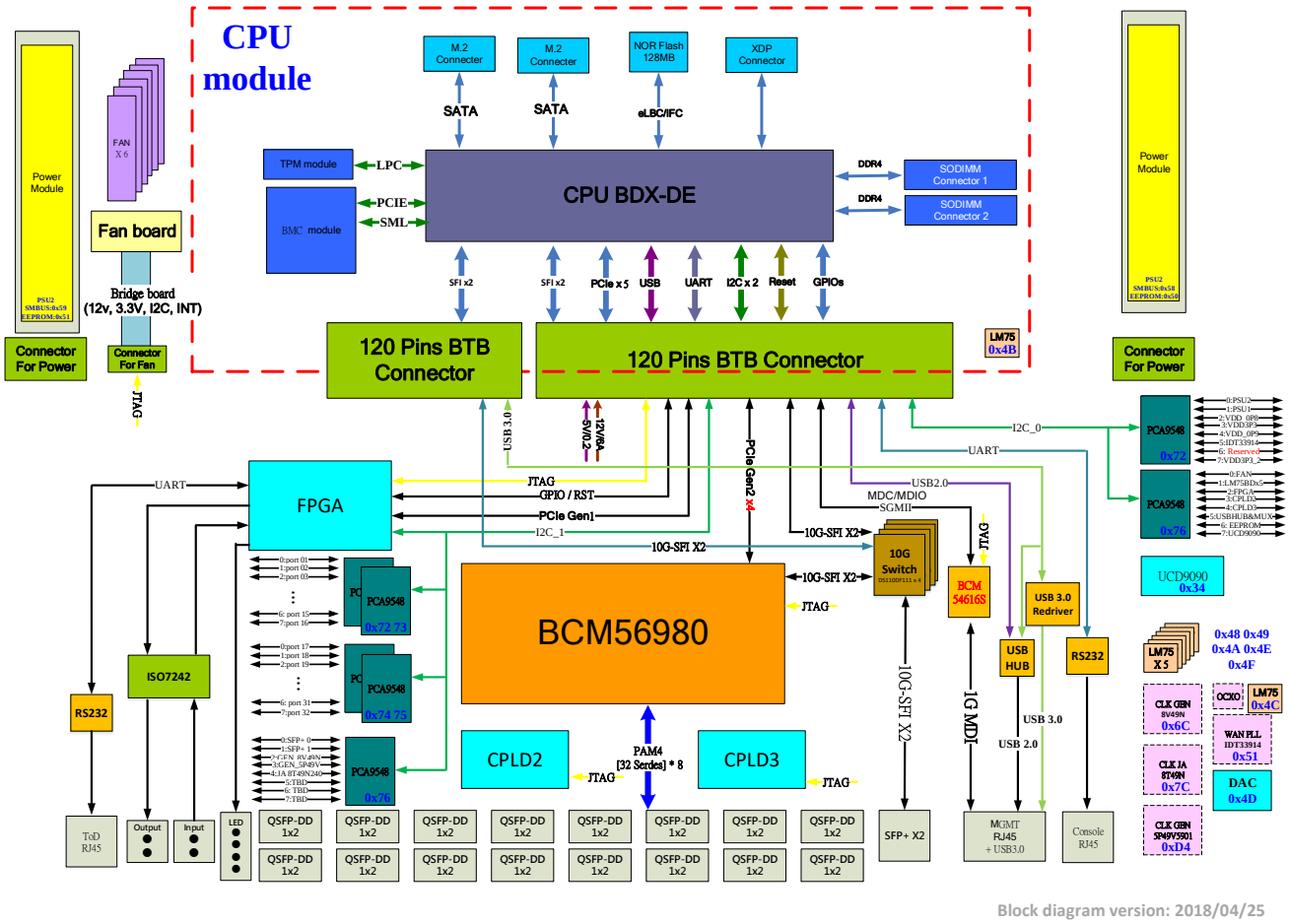
PTP Clock	1PPS and 10MHz SMB connector output
PCB	Switch mainboard, 413/5mm x 269mmx4.0mm, 24 Layers CPU board, 210mm x 123.5mmx2.0mm, 12 Layers Fan board, 281 x 57.9mmx2.36mm, 4 Layers
Mechanical Dimension	17.25” x 21.1” x 1U
PSU	Redundant/hot swappable 1300W AC/DC PSU
System Cooling	6 fan-tray modules with 40mm x40mm x 56mm 12V fans, hot-swappable
System Air Flow	AFO/AFI(Note.)

Table 2-1 System Overview

2.2. Block Diagram

AS9700-32X provides 32 x 400G QSFP56-DD and 2 x 10G SFP+ ports on the board. It supports one 1G RJ-45 port for management and control. The switch controller is BCM56980. A BlackHawkCore with max. 12.8TB/s switch controller. BCM56980 is connected to CPU module via PCIe Gen2.0 x 4. The host system includes two banks of 8GB DDR4 SO-DIMM, two 16MB SPI Flash, Watchdog timer, Thermal detector, SYNC Ethernet and other glue logic.

The Base unit uses 12VDC and 5VDC from the Hot swappable Power module.



Block diagram version: 2018/04/25

Figure 2-6 System Block Diagram

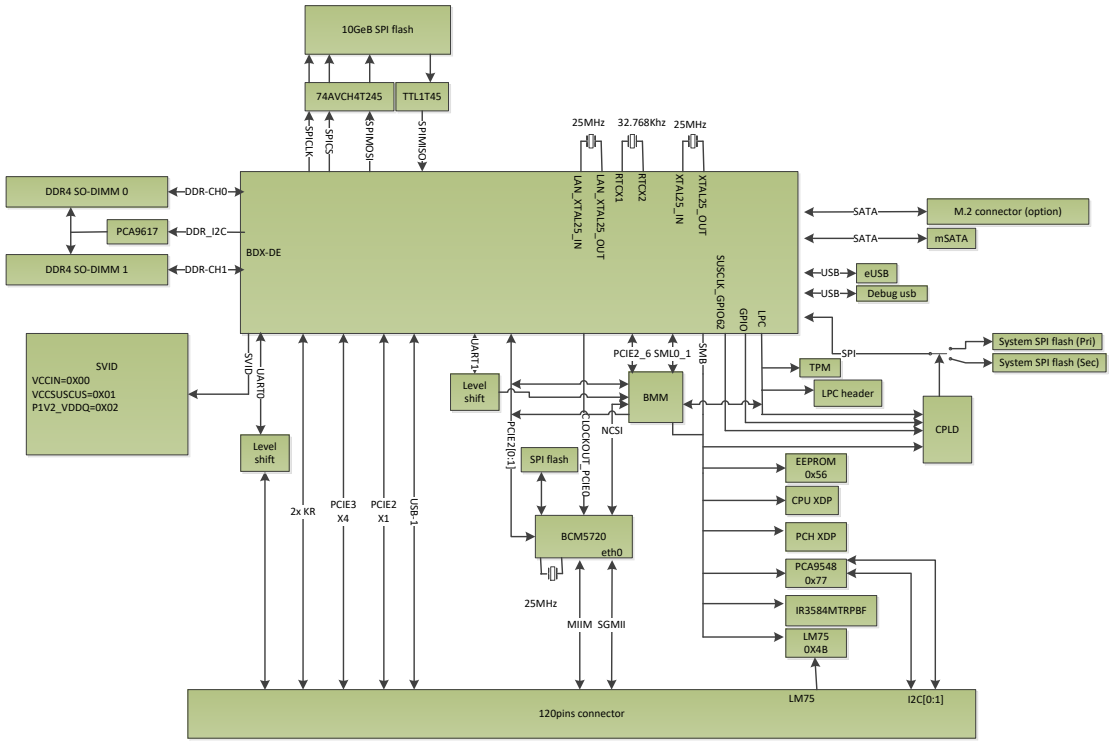


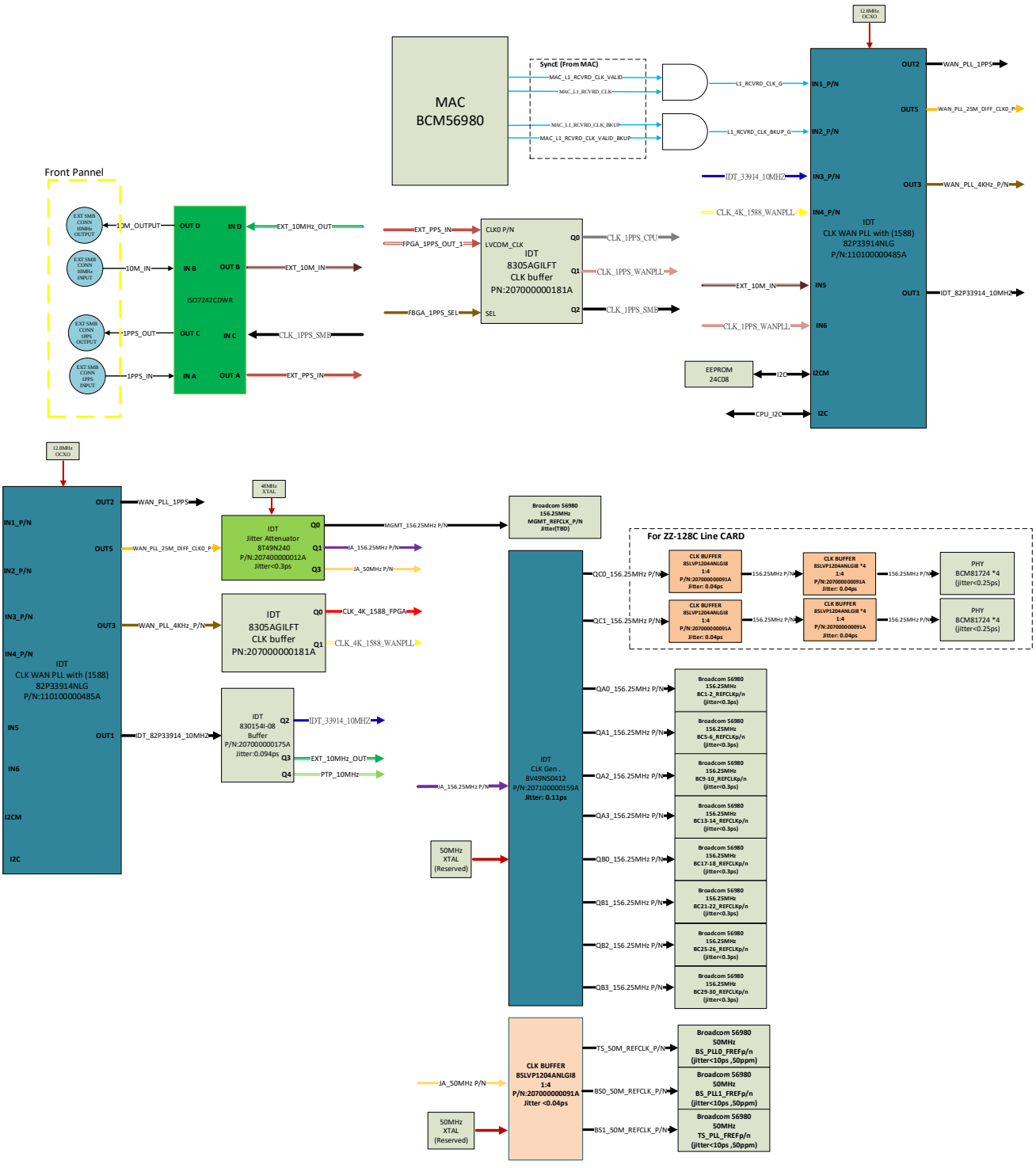
Figure 2-7 CPU Board Block Diagram

2.2.1. Clock Tree

The unit supports has a Synchronous logic consisted of Network Interface Synchronizer chip, Jitter attenuators and clock buffers. The key component is a Network Interface Synchronizer chip.

The Network Interface Synchronizer chip selects a reference clock from one of two valid clock sources generating a Stratum 3 compliant reference clock for the Broadcom Tomahawk III chip. This clock is also used as a transmit reference clock for all external interface ports. This logic consists of a IDT 82P33914 Network Interface Synchronizer chip and Oven controlled crystal oscillator. This synchronizer chip when properly configured will produce 25MHz and 156.25MHz clock which frequency locked to a selected port recovered clock.

The IDT 82P33914 can provides physical layer and packet based synchronous clocks for IEEE 1588 /PTP Telecom Profile applications, which configured through an I2C interface, it reports major state information via a number of status and control signals. CPU will extract time stamp information in packets come from MAC, then it sends time information to 82P33914 to generate SYNC clock, and to FPGA to transform these information to BroadSync format. MAC can get time information via BroadSync interface and do synchronization.


MAC
BCM56980
SyncE (From MAC)
MAC_L1_RCVRD_CLK_VALID
MAC_L1_RCVRD_CLK
MAC_L1_RCVRD_CLK_BKUP
MAC_L1_RCVRD_CLK_VALID_BKUP
L1_RCVRD_CLK_G
L1_RCVRD_CLK_BKUP_G
12.8MHz OCXO
IDT_33914_10MHZ
CLK_4K_1588_WANPLL
EXT_10M_IN
CLK_1PPS_WANPLL
CPU_I2C
EEPROM
24C08
IDT
CLK WAN PLL with (1588)
82P33914NLG
P/N:110100000485A
OUT2
WAN_PLL_1PPS
OUT5
WAN_PLL_25M_DIFF_CLK0_P
OUT3
WAN_PLL_4KHz_P/N
OUT1
IDT_82P33914_10MHz
Front Pannel
EXT SMB CONN 10MHz OUTPUT
10M_OUTPUT
EXT SMB CONN 10MHz INPUT
10M_IN
EXT SMB CONN 1PPS OUTPUT
1PPS_OUT
EXT SMB CONN 1PPS INPUT
1PPS_IN
ISO7242CDWR
OUT D
IN D
OUT B
IN B
OUT C
IN C
OUT A
IN A
EXT_10MHz_OUT
EXT_10M_IN
CLK_1PPS_SMB
EXT_PPS_IN
EXT_PPS_IN
FPGA_1PPS_OUT_1
FBGA_1PPS_SEL
CLK0 P/N
LVCOM_CLK
SEL
IDT
8305AGILFT
CLK buffer
PN:207000000181A
Q0
Q1
Q2
CLK_1PPS_CPU
CLK_1PPS_WANPLL
CLK_1PPS_SMB
12.8MHz OCXO
IDT
CLK WAN PLL with (1588)
82P33914NLG
P/N:110100000485A
WAN_PLL_1PPS
WAN_PLL_25M_DIFF_CLK0_P
WAN_PLL_4KHz_P/N
IDT_82P33914_10MHz
40MHz XTAL
IDT
Jitter Attenuator
8T49N240
P/N:207400000012A
Jitter<0.3ps
MGMT_156.25MHz P/N
JA_156.25MHz P/N
JA_50MHz P/N
IDT
8305AGILFT
CLK buffer
PN:207000000181A
CLK_4K_1588_FPGA
CLK_4K_1588_WANPLL
IDT
830154I-08
Buffer
P/N:207000000175A
Jitter:0.094ps
IDT_33914_10MHZ
EXT_10MHz_OUT
PTP_10MHz
Broadcom 56980
156.25MHz
MGMT_REFCLK_P/N
Jitter(TBD)
For ZZ-128C Line CARD
CLK BUFFER
8SLVP1204ANLGI8
1:4
P/N:207000000091A
Jitter: 0.04ps
156.25MHz P/N
PHY
BCM81724 *4
(jitter<0.25ps)
IDT
CLK Gen .
8V49NS0412
P/N:207100000159A
Jitter: 0.11ps
JA_156.25MHz P/N
50MHz
XTAL
(Reserved)
QC0_156.25MHz P/N
QC1_156.25MHz P/N
QA0_156.25MHz P/N
QA1_156.25MHz P/N
QA2_156.25MHz P/N
QA3_156.25MHz P/N
QB0_156.25MHz P/N
QB1_156.25MHz P/N
QB2_156.25MHz P/N
QB3_156.25MHz P/N
Broadcom 56980
156.25MHz
BC1-2_REFCLKp/n
(jitter<0.3ps)
BC5-6_REFCLKp/n
BC9-10_REFCLKp/n
BC13-14_REFCLKp/n
BC17-18_REFCLKp/n
BC21-22_REFCLKp/n
BC25-26_REFCLKp/n
BC29-30_REFCLKp/n
CLK BUFFER
8SLVP1204ANLGI8
1:4
P/N:207000000091A
Jitter <0.04ps
JA_50MHz P/N
50MHz
XTAL
(Reserved)
TS_50M_REFCLK_P/N
BS0_50M_REFCLK_P/N
BS1_50M_REFCLK_P/N
Broadcom 56980
50MHz
BS_PLL0_FREFp/n
(jitter<10ps ,50ppm)
BS_PLL1_FREFp/n
TS_PLL_FREFp/n

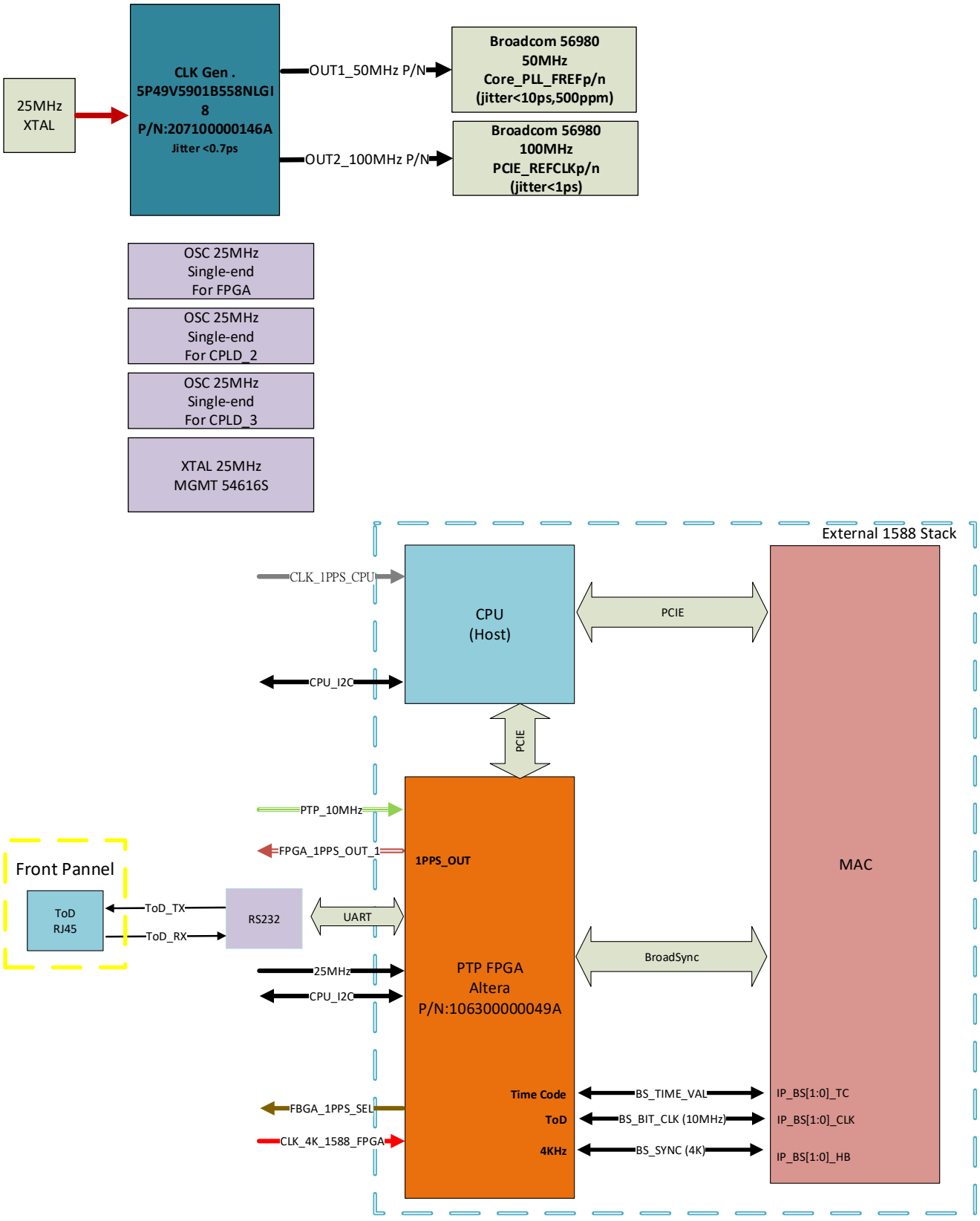


Figure 2-8 Switch board clock Tree

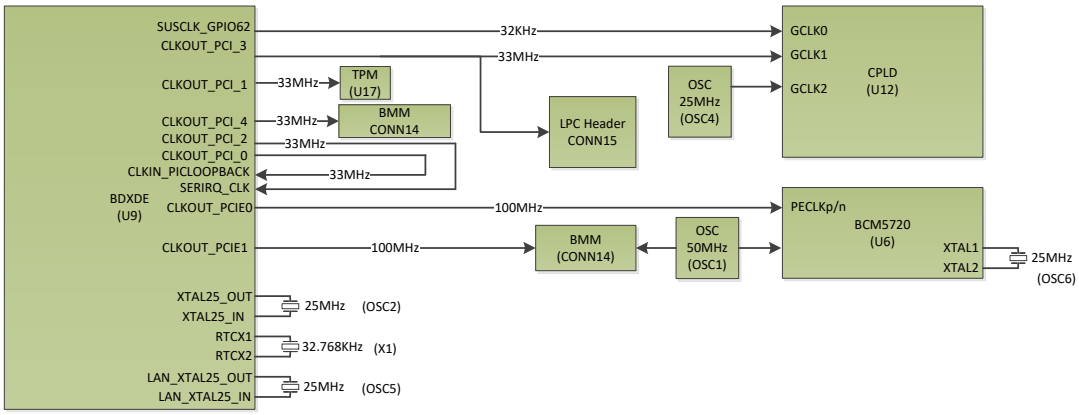


Figure 2-9 CPU board clock Tree

2.2.2. Power Tree

2.2.2.1. CPU board power tree

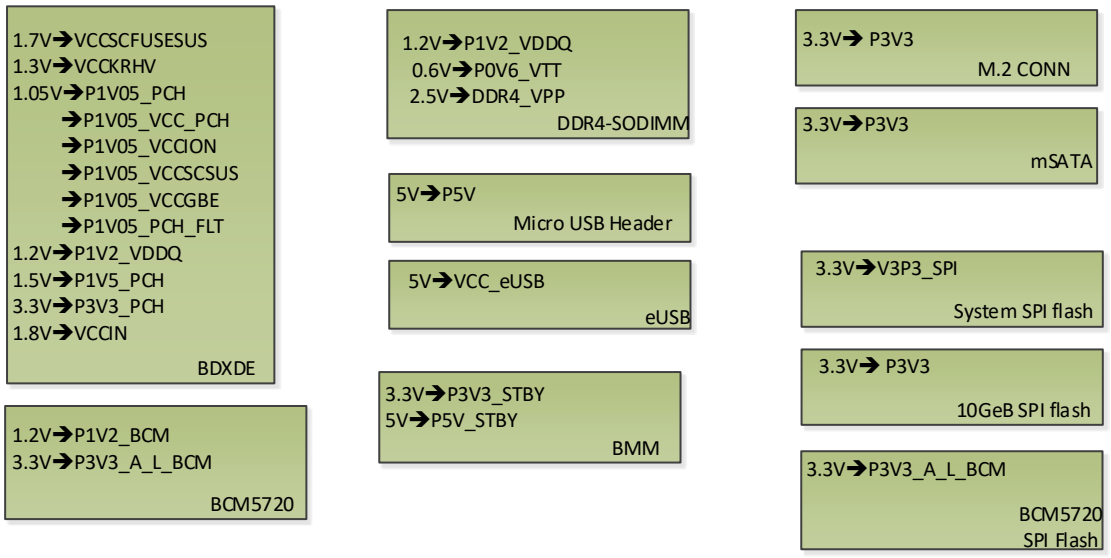
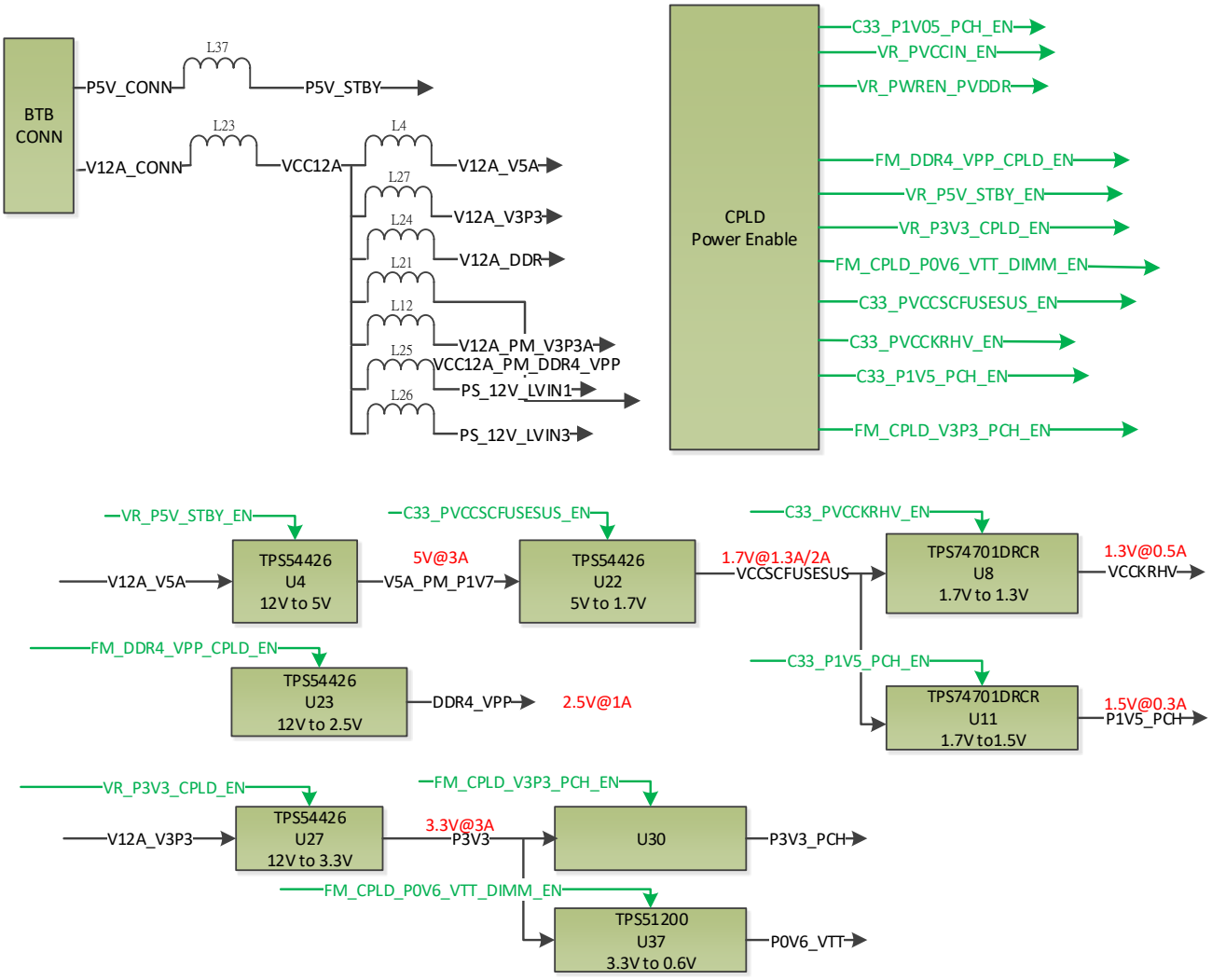


Figure 2-10 CPU Power rail


BTB CONN
P5V_CONN
L37
P5V_STBY
V12A_CONN
L23
VCC12A
L4
V12A_V5A
L27
V12A_V3P3
L24
V12A_DDR
L21
L12
V12A_PM_V3P3A
L25
VCC12A_PM_DDR4_VPP
PS_12V_LVIN1
L26
PS_12V_LVIN3
CPLD Power Enable
C33_P1V05_PCH_EN
VR_PVCCIN_EN
VR_PWREN_PVDDR
FM_DDR4_VPP_CPLD_EN
VR_P5V_STBY_EN
VR_P3V3_CPLD_EN
FM_CPLD_P0V6_VTT_DIMM_EN
C33_PVCCSCFUSESUS_EN
C33_PVCCKRHV_EN
C33_P1V5_PCH_EN
FM_CPLD_V3P3_PCH_EN
VR_P5V_STBY_EN
V12A_V5A
TPS54426 U4 12V to 5V
5V@3A
V5A_PM_P1V7
C33_PVCCSCFUSESUS_EN
TPS54426 U22 5V to 1.7V
1.7V@1.3A/2A
VCCSCFUSESUS
C33_PVCCKRHV_EN
TPS74701DRCR U8 1.7V to 1.3V
1.3V@0.5A
VCCKRHV
FM_DDR4_VPP_CPLD_EN
TPS54426 U23 12V to 2.5V
DDR4_VPP
2.5V@1A
C33_P1V5_PCH_EN
TPS74701DRCR U11 1.7V to1.5V
1.5V@0.3A
P1V5_PCH
VR_P3V3_CPLD_EN
V12A_V3P3
TPS54426 U27 12V to 3.3V
3.3V@3A
P3V3
FM_CPLD_V3P3_PCH_EN
U30
P3V3_PCH
FM_CPLD_P0V6_VTT_DIMM_EN
TPS51200 U37 3.3V to 0.6V
P0V6_VTT

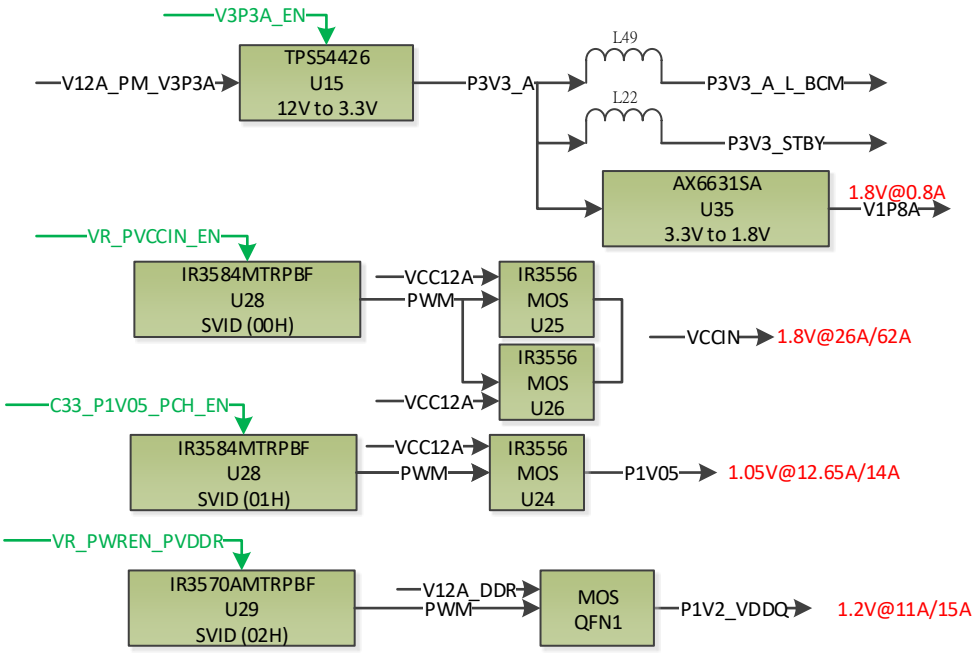


Figure 2-11 CPU Power tree and power solution

2.2.2.2. Switch board power tree

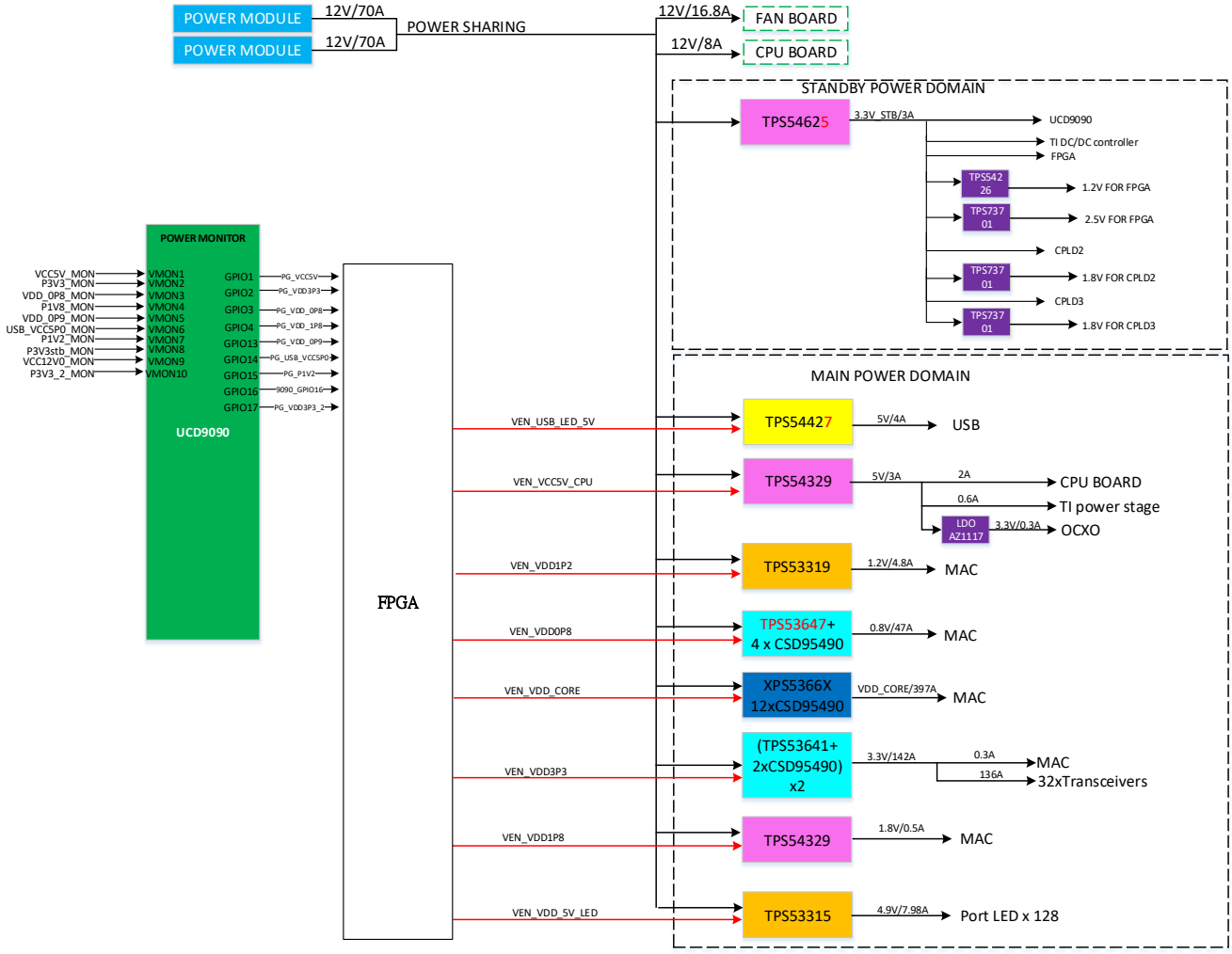


Figure 2-12 Switch board Power Tree

2.2.3. Reset Tree

The reset system will follow as below.

1. The CPU board and switch board will be power on. And the reset monitor IC will check DC power voltage if reach the threshold.
2. The monitor IC will send Power_RST signal to CPLD if all power is OK.
3. CPLD pass the MANU_RST signal to CPU board, and hold the all reset signals of switch board's device
4. CPU get the switch board's MANU_RST signal from switch board's CPLD, it means switch is ready to boot up. CPU board will check itself status and pull up Reset_SYS_CPLD signal to switch's CPLD to boot up switch board.
5. When switch's CPLD get the Reset_SYS_CPLD signal, switch's CPLD will pass to all device on switch to boot up device.
6. When the system running, the switch's CPLD has different register for every device's rest signal. CPU can reset switch's device separately via switch's CPLD register.

If CPU wants to reset itself without main board system, CPU can set "1" in "reset_lock" register of main board's CPLD1 (0x0B).Main board CPLD1 will block "reset_sys_cpld" signal to CPLD1, and main board CPLD1 will send "reset_lock" signal to CPU to indicate the "reset_lock" register status.

The default value of “reset_lock” register is “0”.

The following is about the reset tree topology.

Figure 2-13 Reset Tree

2.2.4. I2C Tree

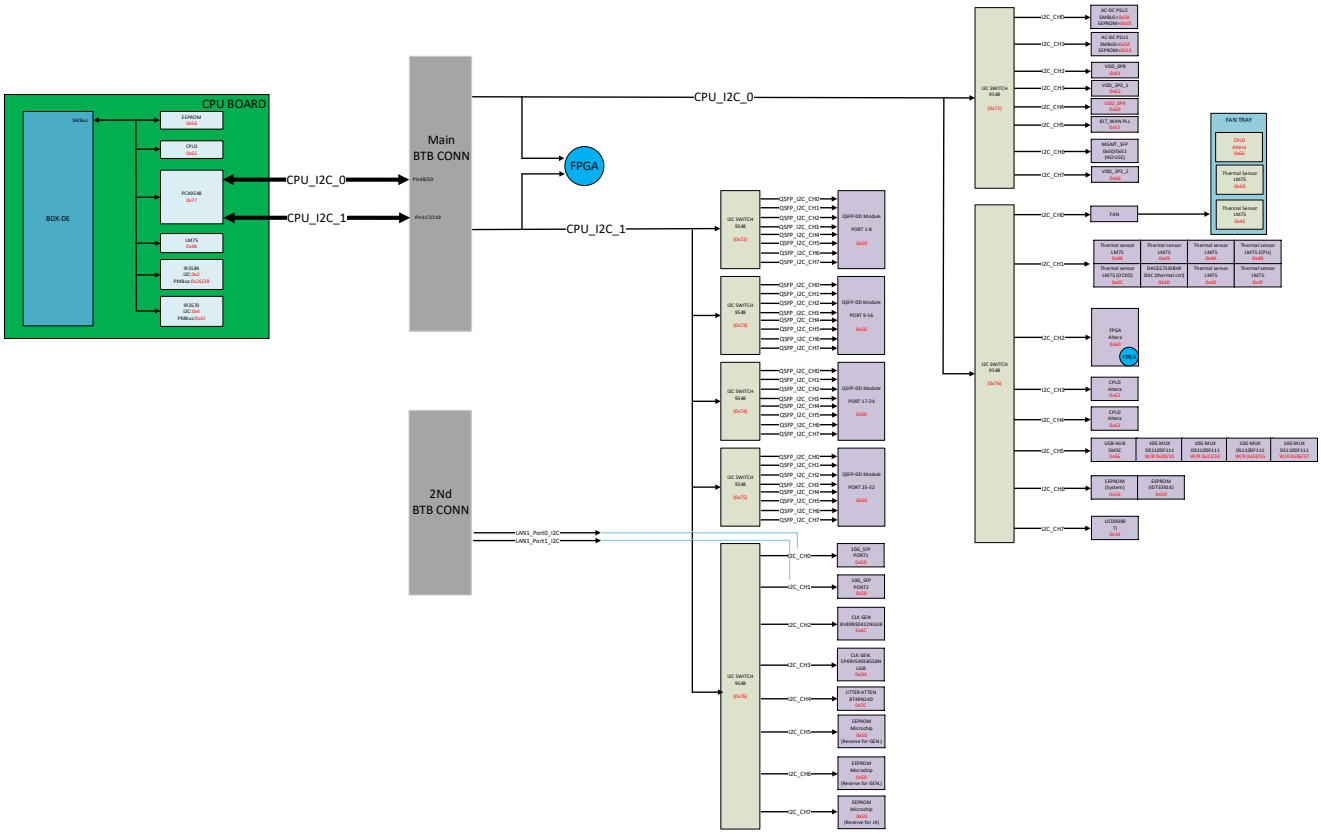


Figure 2-14 I2C Tree

2.3. LED Indicator

The system has 5 status LEDs, 32 400G port LEDs and 2 SFP+ LEDs. The 5 status LEDs are for PWR1. PWR2. Fan, Diag and LOG.

The 5 system LED is on left side.

The port numbering scheme on the front panel is starting from 1 to 34. Even on top, odd on bottom, left to right.

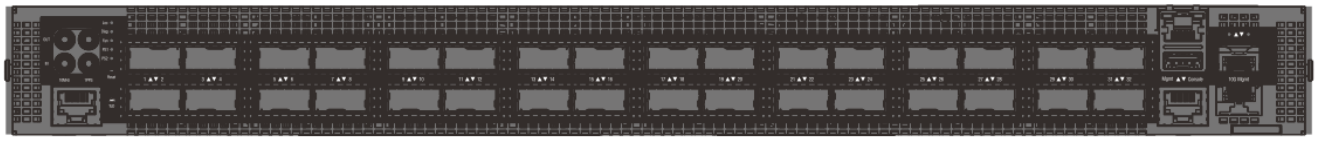


Figure 2-15 Front panel

2.3.1. System LED

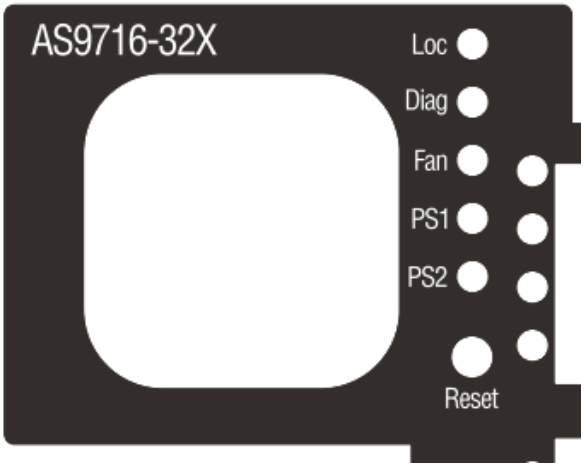


Figure 2-16 System LED

LED	Color	Mode
LOC	Amber Flashing	Flashing by remote management command. Assists the technician in finding the right device for service in the rack.
	OFF	Not a particular switch that technician need to find
Diag	Green	System self-diagnostic test successfully completed.
	Amber	System self-diagnostic test has detected a fault. (Fan, thermal or any interface fault.)
	Blinking Green	System boot in progress
FANs	Green	System FAN operating normally.
	Amber	Fan tray present buy system FAN is fault.
	OFF	System OFF
Power Supply 1	Green	This power is operating normally.
	Amber	PWR present but not power on or this power is fault.
	Off	Power supply not present.
Power Supply 2	Green	This power is operating normally.
	Amber	PWR present but not power on or this power is fault.

LED	Color	Mode
	Off	Power supply not present.

Table 2-2 System LED Definition

2.3.2. Port LED

AS9716-32X use 4 LED for port LED. First LED is tri-color LED and the other three LED is single Color LED (Green) for fan out usage.

There are 32 RGB LED for 32 400G port, one port with 1 RGB LED. 1 RGB LED indicates one port status. The QSFP56-DD port can run in 400G and 200G speed.

Table 2-3 Port LED Definition

LED		Condtion	Status
QSFP-DD Port LED (400G Mode)		On/Flashing **Blue**	QSFP-DD port has a valid link at 400G. Flashing indicates activity.
		Off	There is no link on the port.
QSFP-DD Port LED (200G Mode)		On/Flashing **White**	QSFP-DD port has a valid link at 200G. Flashing indicates activity.
		Off	There is no link on the port.
QSFP-DD Port LED (100G Mode)		On/Flashing **Green**	QSFP-DD port has a valid link at 100G via break out cable. Flashing indicates activity.
		Off	There is no link on the port.
QSFP-DD Port LED (50G Mode)		On/Flashing **Green**	QSFP-DD port has a valid link at 50 G via break out cable. Flashing indicates activity.
		Off	There is no link on the port.
10G management Port SFP+ Port LED		On/Flashing Green	SFP+ port has a valid link at 10G Flashing indicates activity.
		On/Flashing Amber	SFP+ port has a valid link at 1G. Flashing indicates activity.
		Off	There is no link on the port.
1G management port RJ45 LED	Link	On	Port has a valid link
		Off	There is no link on the port
	Activity	Flashing	Flashing indicates activity
		Off	There is no link on the port

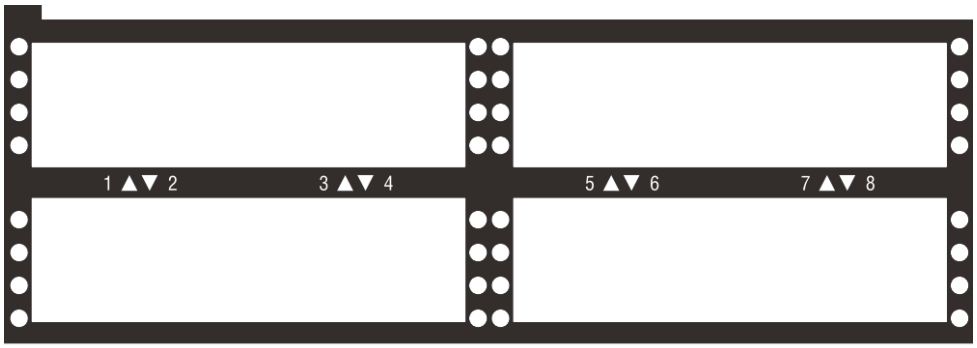


Figure 2-17 Port LED indication

The CPLD drives the LED signals by de-coding the LED stream from MAC.
Note: The LEDs flash to indicate activity.

2.3.3. Management Port LED- 1G and 10G

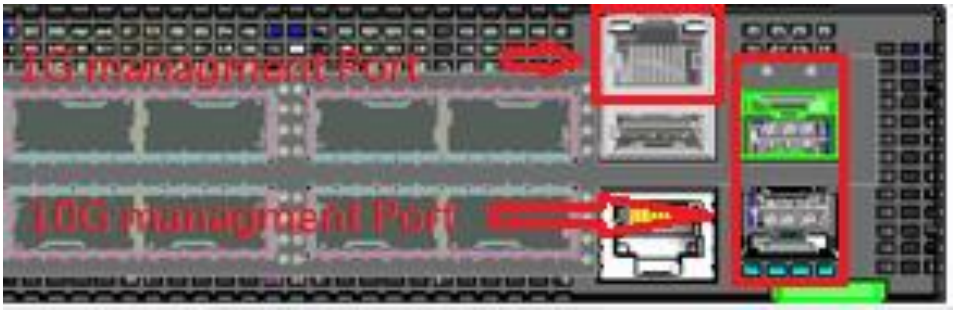


Figure 2-18 Management Port LED

Table 2-4 Management Port LED Definition

LED		Condtion	Status
10G management Port SFP+ Port LED		On/Flashing Green	SFP+ port has a valid link at 10G Flashing indicates activity.
		On/Flashing Amber	SFP+ port has a valid link at 1G. Flashing indicates activity.
		Off	There is no link on the port.
1G management port RJ45 LED	Link	On	Port has a valid link
		Off	There is no link on the port
	Activity	Flashing	Flashing indicates activity
		Off	There is no link on the port

2.4. Reset Button

There is a reset button on the front panel to reboot the system.

Reset button

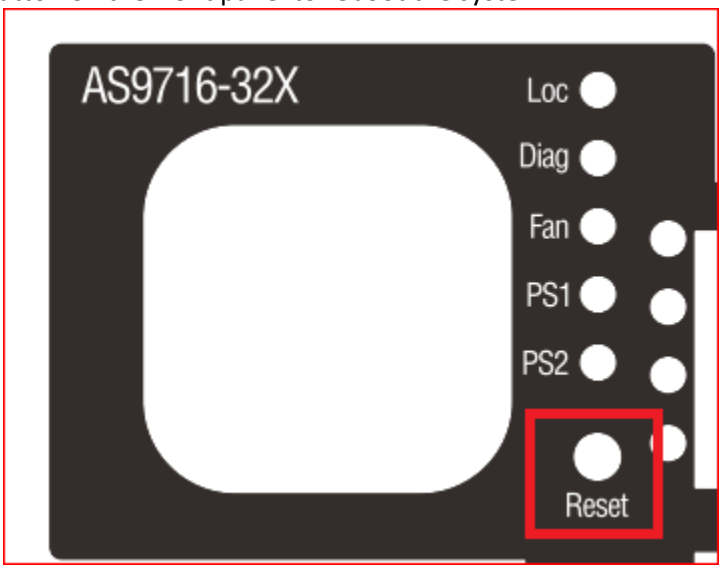


Figure 2-19 Front panel reset button

3. CPU Sub-system (Broadwell-DE)

3.1. Configurations of CPU

- 2 DDR4 channels, 1DPC with DDR4 2133 ECC SODIMM.
- Memory speed: DDR4 2133, up to 2400.
- PCI Express Lanes :
  - 24Gen3, 1x16 and 1x8, 6 controllers x4 granularity (Uncore)
  - 8 Gen2, 2x4, 8controlles x 1 granularity (Integrated PCH logic)
- Integrated 10GbE Controller contains two independent 10GbE MACs that support an XGMII interface link to the either KX4 or KR PHY device interfaces.
  - KX4 PHY supports
    - XAUI for XGMII extension
    - 10GBASE-KX4 for gigabit backplane applications.
    - 2500BASE-KX for gigabit backplane applications.
    - 1000BASE-KX for gigabit backplane applications.
  - KR PHY supports
    - 10GBASE-KR for gigabit backplane application
    - 1000BASE-KX for gigabit backplane application.
    - 10GBASE SFP+ through a XFI compatible interface
    - 10GBASE-T through a XFI compatible interface
- Integrated PCH logic
  - PCI Express Base specification, revision 2.0 support for up to eight ports with transfers up to 5GT/s
  - ACPI power management logic support revision 4.0a
  - Enhanced DMA controller, interrupt controller, and timer function.
  - Integrated Serial ATA host controllers with independent DMA operation on up to six ports.

- xHCI USB controller provides support for up to 4 USB ports, of which four can be configured as SuperSpeed USB 3.0 ports.
- One legacy EHCI USB controller provides a USB debug port.
- Integrated 10/100/1000 Gigabit Ethernet MAC witch system defense.
- System Management Bus (SMBus) specification, version 2.0 with additional support for I2C devices
- Supports intel Virtualization Technology for Directed I/O (Intel VT-d)
- Supports intel Trusted Execution Technology (Intel TXT)
- Integrated clock controller
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Serial Peripheral Interface (SPI) support
- JTAG Boundary scan support.

3.1.1. Reset Flow of CPU

The cores and uncore supports the following reset types. Note PWRGOOD_CPU is driven by the PCH.

Cold reset is the first time when the platform asserts PWRGOOD_CPU and asserts RESET_CPU_N to the uncore. The platform has to wait for the Base Clock (BCLK) and the power to be stable before asserting PWRGOOD_CPU. This results in reset of all the states in the processor, including the sticky state that is preserved on the other resets. PLLs come up, I/O (DMI2,uncore PCI Express, and DDR) links undergo initialization and calibration. Components in fixed and variable power planes are brought up. Ring, router, SAD, and various lookup tables in the core/Cbo are initialized. Once the uncore initialization has completed, then the power is enabled to the cores and cores are brought out of reset. BIOS is fetched from the PCH.

Warm reset is typically a platform wide event and is indicated by assertion and deassertion of the RESET_CPU_N signal on the socket while PWRGOOD_CPU remains asserted. This reset preserves the error log state and machine check bank states for use by platform debug. The warm reset preserves the error log state and machine check bank states for use by platform for post error event analysis. To maintain the DDR memory attached to the processor self refresh and sticky registers remain valid through out a warm reset, the "Reset_warn" message must complete by the processor. The "Reset_warn" is a message that gets issued from the PCH to all sockets prior to warm reset. BIOS will need to program the FlexRatioMSR/CSR in each socket and invoke the Warm Reset to the platform.

The reset flow is divided into the following 5 phases.

- Phase 0: Expectations from the platform (before assertion of PWRGOOD_CPU)
  - Initially PWRGOOD_CPU signal is deasserted and RESET_CPU_N is asserted to the socket. PWRGOOD_CPU cannot deassert until RESET_CPU_N is asserted.
  - PWRGOOD_CPU must be asserted no sooner than 2 ms after the IVR Vccin supply has fully ramped-up.
  - Vccioin may be brought up before Vccin for IVR is brought up if not at the same time. Vccioin is intended to source the PECI IO.
  - The PWRGOOD_CPU and RESET_CPU_N signals have "clean" edges.
  - The reference clock (BCLK) is stable.
  - All external power rails have ramped as follows: Vccin, Vccioin, VCCD are up and stable at their nominal values
  - Assert PWRGOOD_CPU (RESET_CPU_N still asserted) only after 2 msec of Vccin,

Vccioin and VCCD at tolerance.

- After the power rails are up and stable for 2 msec and reference clocks are stable, platform asserts PWRGOOD_CPU and continues to assert RESET_CPU_N signal to the socket.
- PWRGOOD_CPU remains asserted as long as Vccin, Vccioin and VCCD remain stable.
- No power sequencing between Vccin and VCCD is required.

- Phase 1: PCU bring-up
  - Phase 1a: Activity Leading to PCU Start-up
    - Assertion of PWRGOOD_CPU (the trigger to move from the end Phase 0 to thestart of Phase 1a).
    - Processor starts a timer (using BCLK) for determinism interval.
    - The PECI and SVID interfaces are held in reset until IVR asserts its power good signal.
    - The PCU PLL is enabled.
  - Phase 1b: Pcode Controlled Preparing for Broad uncore Bring-Up
    - Starting at the sub-phase, all steps should be synchronous.
    - PCU micro controller comes out of reset to start reset pcode execution. This is the planned "re-entry" point for Warm Reset processing.
    - Early reset pcode determines that it is at the start of Phase 1b.
    - Pcode brings the rest of the PCU hardware out of reset.
    - Pcode determines the boot config.
    - Pcode issues SVID command to ramp Vccin to 1.8V for cold reset.
    - Pcode reads and compares Vccin MBVR ICCMAX limit (reg 21h) vs its own supported ICCMAX limit:
      - If VR's ICCMAX ≥ supported ICCMAX then bootup continues.
      - If VR's ICCMAX < supported ICCMAX then bootup halts and system shuts down. MSR 411h IA32_MC4_STATUS logs Error code 0x1e - MCA_VR_ICC_MAX_LESS_THAN_FUSED_ICC_MAX in field MSEC_FW.
    - Pcode sequences uncore non-boot IVRs to ramp up.
    - Pcode signals uncore power good to IIO, IMC.
    - Delivery of the uncore power good signals defines the transition from the end of phase 1b to the beginning of phase 1c.
  - Phase 1c: PLL locking and IO Calibration
    - Pcode initiates thermal sensors.
    - Pcode locks PLLs in the following order: IIO, and IMC.
    - Pcode instructs the ring PLLs to start locking.
    - RESET_CPU_N signal is deasserted.
    - De-assertion of RESET_CPU_N signal will bring PCU out of reset and signifies the transition from the end of Phase 1c to the beginning of Phase 2.
- Phase 2: Uncore initialization and core bring up
  - The starting assumptions are:
    - All IVRs except core IVRs have ramped-up and are stable.
    - All PLLs except core PLLs have locked.
    - Phase 2 is entered as a result of de-assertion of external pin RESET_CPU_N.
    - Boot mode related straps have been sampled and are available.
    - Some IO link calibration have started and may or may not have completed by the start of this phase.

- In this phase
  - PCU comes out of reset again and again determines the reset type.
  - Reset is deasserted to the ring units (HA, Cbo, IIO).
  - Reset is de-asserted to System Agents (IMC, IIO).
  - Pcode initializes the ring stops
  - Pcode performs boot mode processing based on straps. Set the advertised firmware, IO, and Intel TXT agent bits appropriately.
  - Pcode services DMI2 handshake protocol. If DMI2 links are used in DMI2 mode, pcode checks if the links have trained to L0. If it's the legacy socket, and if DMI2 links does not reach L0 within 3-4 ms, pcode executes error flow.
  - Pcode determines number of cores, slices and st/mt-threading for the core. In this step pcode also takes into account number of BIOS-disabled cores. Pcode determines whether BIST should be executed. BIST is executed if BIST Strap is set or requested.
  - Pcode programs the logical ids and switches from physical to logical mode.
  - LLC reset and configuration.
  - If it's not service processor boot mode, pcode waits for links to get to parameter exchange.
  - Pcode releases links to get to Normal operation (i.e. L0)
  - Pcode sets core Cstate to C1

- Phase 3: Reset execution (from core reset to fetch boot vector)
  - The starting assumptions are:
    - Before this phase starts, following information is provided to the core: APIC-ID, whether it's the BSP, SMT enable/disable, reset type (cold, warm, C6 exit).
    - Uncore necessary to the get to the BIOS and Intel TXT Address space is fully initialized.
  - In this phase:
    - Initialize core's internal structures, arrays, microarchitectural and architectural state.
    - Execute MLC BIST if BIST enabled.
    - Initialize uncore.
    - Read LLC BIST results from the uncore and report it in the EAX register.
    - Report LLC and MLC BIST results.
    - The core and thread selected as package BSP fetches BIOS or goes to “Wait-for-SIPI” state
    - The end assumption is there is at least one thread that was designated as package BSP.
- Phase 4: BIOS execution

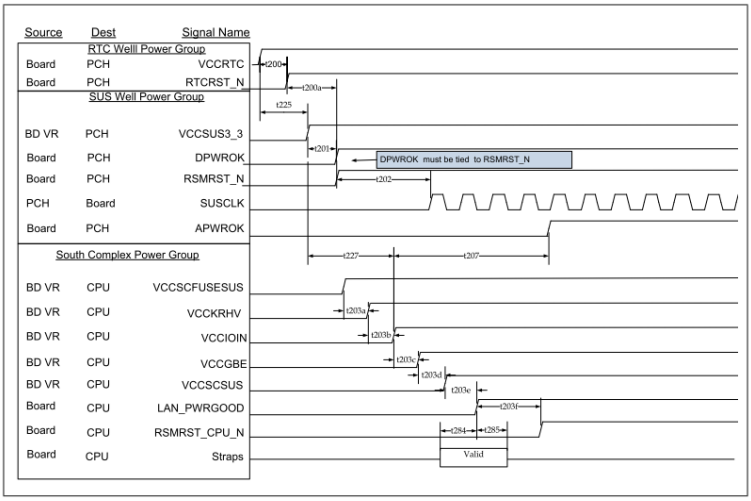


Figure 3-1 Power Sequencing Diagram G3 with RTC loss to S5

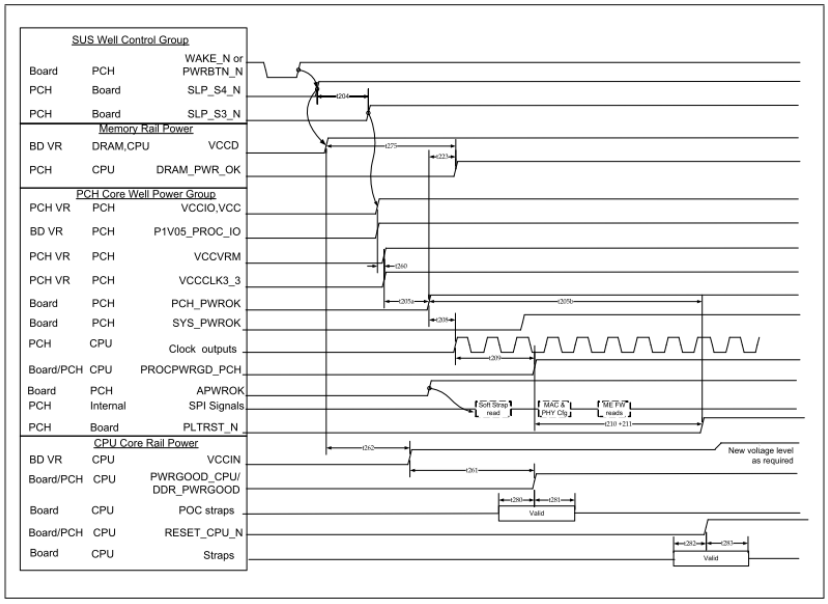


Figure 3-2 Power Sequencing Diagram S5 to S0

3.1.2. PCH Strap Pin Definition

Table 3- 1 PCH Strap definitions

Strap pin	description	value
SATA1GP/ GPIO19	This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used	1

	in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 Reserved 1 1 SPI (default) 0 0 LPC	
GPIO51	This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.	1
SATA3GP /GPIO37	0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).	0
MFG_MODE_STRAP	0 = Enable security measures defined in the Flash Descriptor. 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.	0
INTVRMEN	0 = DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source (should be connected to an external VRM). It should not pull the strap low. 1 = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left as No Connect.	1
GPIO62 / SUSCLK	0 = Disable PLL On-Die voltage regulator. 1 = Enable PLL On-Die voltage regulator.	1
DSWODVREN	0 = Disable Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This mode is only supported for testing environments. 1 = Enable DSW 3.3 V-to-1.05 V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards.	1
SPKR	0 = Disable “No Reboot” mode. 1 = Enable “No Reboot” mode (integrated PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.	
SATA2GP/GPIO36	0 = SoC RX is terminated to VSS. Grangeville platform only supports SoC Rx terminated to VSS. 1 = SoC RX is terminated to VCC/2.	0
GPIO33	0 = SoC TX is terminated to VSS. Grangeville	0

	platform only supports SoC Tx terminated to VSS 1 = SoC TX is terminated to VCC/2.	
GPIO53	0 = SoC is in AC-coupling mode. Grangeville platform only supports AC-coupling mode. 1 = SoC is in DC-coupling mode.	0
GPIO55	0 = Enable “Top Swap” mode. This inverts an address on access to SPI and firmware hub, so the processor believes its fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64 KB blocks in the FWH or the appropriate address lines (A16, A17, A18, A19, or A20) as selected in Top-Swap Block size soft strap (handled through FITc. 1 = Disable “Top Swap” mode.	1
GPIO8	This pin must not be driven low until after rising edge of RSMRST_N.	1
GPIO44	This pin must not be driven low until after rising edge of RSMRST_N.	1
GPIO46	This pin must not be driven low until after rising edge of RSMRST_N.	1
BIST_ENABLE	Build-in Self Test (BIST) enable strap: 0 = BIST Disable 1 = BIST Enable	0
BMCINIT	Integrated Service Processor Boot Mode Selection: 0 = Integrated Service Processor Boot Mode Disabled. 1 = Integrated Service Processor Boot Mode Enable	1
TXT_PLTEN	0 = The platform is not Intel TXT enabled. 1 = Default. The platform is Intel TXT enabled.	0
TXT_AGENT	0 = Default. The SoC is not the Intel TXT Agent. 1 = The SoC is the Intel TXT Agent.	0
SAFE_MODE_BOOT	0 = Safe Mode Boot Disabled 1 = Safe Mode Boot Enabled	1
DEBUG_EN_N	0 = Debug Mode 1 = Normal Mode	XDP_PRESENT_N
DDR3_4_STRAP	Select between DDR4 and DDR3 0 = DDR3, it requires <1K ohm pull down in order to out drive the internal pull up. 1= DDR4 (Default)	1
PECI0 ; PECI1 ; PECI2	In micro-server design space, there will be multiple sockets that share a PECI bus. However these sockets are effectively independent agents. The PECI IDs are used as	000

	straps to identify which socket is which in order for PECI bus to work.	
LAN_MDIO_DIR_CTL_0; LAN_MDIO_DIR_CTL_1	00 = Both LAN ports are disabled. Note: In this mode manageability is not functional and must not be enabled in NVM control word 1. 01 = Port 1 is disabled. Port 0 is enabled. 10 = Reserved 11 = Both Port 0 and 1 are enabled. Recommend 5.1K ohm pull up to VCCIOIN or 5.1K ohm pull down to GND.	11
RSVD12_AJ67	This pin should have a 5.1K ohm pull down to GND.	0
RSVD11_AG67	This pin should have a 5.1K ohm pull down to GND.	0
RSVD10_AN78	This pin should have a 5.1K ohm pull down to GND.	0
RSVD09_AC64	This pin should have a 5.1K ohm pull down to GND.	0
SERIRQ_DIR	Recommend 5.1k ohm pull up to VCCIOIN.	1
UART_TXD[0]	Recommend 5.1k ohm pull down to GND.	0
UART_TXD[1]	Controls the security attributes on the NVM - for pre-production usage only. 0 = Disable NVM Security (Default) 1 = Security Enabled Recommend 5.1K ohm pull down to GND.	0
LAN_NCSI_RXD0	Recommend 5.1K ohm pull up to VCCIOIN.	1
LAN_NCSI_RXD1	Enable/Disable manageability traffic: 0 = LAN available in S5 for WoL (Default) 1 = LAN not available in S5. Manageability is disabled. Recommend 5.1K ohm pull down to GND.	0
LAN_NCSI_ARB_OUT	Selects SVID VR Operating Mode 1 - VCCSCSUS, P1V05_PCH, VCCGBE, VCCIOIN are combined into one SVID controlled supply. 0 - Separate SVID controllers (default).	1
RSVD84	49.9Ω 1% to GND	0
RSVD93	1k - 5.1kΩ to GND	0
RSVD94	1k - 5.1kΩ to GND	0
RSVD00	1k - 5.1kΩ to VCC3_3	1
RSVD18	1k - 5.1kΩ to GND	0
RSVD16	1k - 5.1kΩ to GND	0
RSVD17	1k - 5.1kΩ to GND	0
RSVD21	1k - 5.1kΩ to GND	0
NCTF/TP	1k - 5.1kΩ to VCC3_3	1

3.2. Memory Mapping

Broadwell-DE SoC contains registers that are located in the processor I/O space and memory space and sets of PCI configuration registers that are located in PCI configuration space. This chapter describes Broadwell-DE SoC I/O and memory maps at the register-set level. Register access is also described.

Table 3- 2 PCI devices and functions

Bus:Device:Function	Function Description
Bus0:Device31:Function0	LPC controller
Bus0:Device31:Function2	SATA controller #1
Bus0:Device31:Function3	SMBus controller
Bus0:Device31:Function5	SATA controller#2
Bus0:Device31:Function6	Thermal subsystem
Bus0:Device29:Function0	USB EHCI controller#1
Bus0:Device28:Function0	PCI-e port1
Bus0:Device28:Function1	PCI-e port2
Bus0:Device28:Function2	PCI-e port3
Bus0:Device28:Function3	PCI-e port4
Bus0:Device28:Function4	PCI-e port5
Bus0:Device28:Function5	PCI-e port6
Bus0:Device28:Function6	PCI-e port7
Bus0:Device28:Function7	PCI-e port8
Bus0:Device25:Function0	Gigabit Ethernet controller
Bus0:Device22:Function0	Intel management engine interface#1
Bus0:Device22:Function1	Intel management engine interface#2
Bus0:Device22:Function2	IDE-R
Bus0:Device22:Function3	KT
Bus0:Device20:Function0	xHCI controller

Table 3- 3 Fixed I/O ranges decoded by Broadwell-DE

I/O Address	Read Target	Write Target	Internal Unit
00h-08h	DMA controller	DMA controller	DMA
09h-0Eh	reserved	DMA controller	DMA
0Fh	DMA controller	DMA controller	DMA
10h-18h	DMA controller	DMA controller	DMA
19h-1Eh	reserved	DMA controller	DMA
1Fh	DMA controller	DMA controller	DMA
20h-21h	Interrupt controller	Interrupt controller	interrupt
24h-25h	Interrupt controller	Interrupt controller	interrupt
28h-29h	Interrupt controller	Interrupt controller	interrupt
2Ch-2Dh	Interrupt controller	Interrupt controller	interrupt
2Eh-2Fh	LPC SIO	LPC SIO	Forwarded to LPC
30h-31h	Interrupt controller	Interrupt controller	interrupt
34h-35h	Interrupt controller	Interrupt controller	interrupt
38h-39h	Interrupt controller	Interrupt controller	interrupt
3Ch-3Dh	Interrupt controller	Interrupt controller	interrupt
40h-42h	Timer/Counter	Timer/Counter	PIT

43h	reserved	Timer/Counter	PIT
4Eh-4Fh	LPC SIO	LPC SIO	Forwarded to LPC
50h-52h	Timer/Counter	Timer/Counter	PIT
53h	reserved	Timer/Counter	PIT
60h	microcontroller	microcontroller	Forwarded to LPC
61h	NMI controller	NMI controller	Processor I/F
62h	microcontroller	microcontroller	Forwarded to LPC
64h	microcontroller	microcontroller	Forwarded to LPC
66h	microcontroller	microcontroller	Forwarded to LPC
70h	reserved	NMI and RTC controller	RTC
71h	RTC controller	RTC controller	RTC
72h	RTC controller	NMI and RTC controller	RTC
73h	RTC controller	RTC controller	RTC
74h	RTC controller	NMI and RTC controller	RTC
75h	RTC controller	RTC controller	RTC
76h	RTC controller	NMI and RTC controller	RTC
77h	RTC controller	RTC controller	RTC
80h	DMA controller, LPC, PCI or PCIe	DMA controller, LPC, PCI or PCIe	DMA
81h-83h	DMA controller	DMA controller	DMA
84h-86h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
87h	DMA controller	DMA controller	DMA
88h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
89h-8Bh	DMA controller	DMA controller	DMA
8Ch-8Eh	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
8Fh	DMA controller	DMA controller	DMA
90h-91h	DMA controller	DMA controller	DMA
92h	Reset generator	Reset generator	Processor I/F
93h-9Fh	DMA controller	DMA controller	DMA
A0h-A1h	Interrupt controller	Interrupt controller	interrupt
A4h-A5h	Interrupt controller	Interrupt controller	interrupt
A8h-A9h	Interrupt controller	Interrupt controller	interrupt
ACh-ADh	Interrupt controller	Interrupt controller	interrupt
B0h-B1h	Interrupt controller	Interrupt controller	interrupt
B2h-B3h	Power management	Power management	Power management
B4h-B5h	Interrupt controller	Interrupt controller	interrupt
B8h-B9h	Interrupt controller	Interrupt controller	interrupt
BCh-BDh	Interrupt controller	Interrupt controller	interrupt
C0h-D1h	DMA controller	DMA controller	DMA
D2h-DDh	reserved	DMA controller	DMA
DEh-DFh	DMA controller	DMA controller	DMA
F0h	Ferr#/interrupt controller	Ferr#/interrupt controller	Processor I/F
170h-177h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
1F0h-1F7h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
200h-207h	Gameport low	Gameport low	Forwarded to LPC
208h-20Fh	Gameport high	Gameport high	Forwarded to LPC
376h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
3F6h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA

4D0h-4D1h	Interrupt controller	Interrupt controller	interrupt
CF9h	Reset generator	Reset generator	Processor I/F

3.3. FLASH

There are four SPI flashs, 2 x 128Mb for BIOS, 1 x 32Mb for 10GBE controller +and 1 x 16Mb for BCM5720.

U1, U31, the two 128Mb flash are for system boot BIOS, one is primary another one is backup.

There are two ways that can update the BIOS flash, one is via dediprog (CONN3), the other is via BMC module. If user want to update bios from BMC, the “BDX_SPI_MUX_SEL” would be pull low from high.

U16, 32Mb flash is for 10G controller setup that need level shift because of that SPI interface voltage level of BDXDE LAN is 1.05volt different SPI flash voltage level.

U39, the 16Mb flash is for BCM5720 MAC setup.

The system boot flash SPI clock rate is 20MHz via the SPI memory mapped configuration register SSFC[18:16] = “000” setting and the CPU GbE LAN SPI flash clock rate is 20MHz via the GBE LAN memory mapped configuration register SSFC[18:16] = “000” setting.

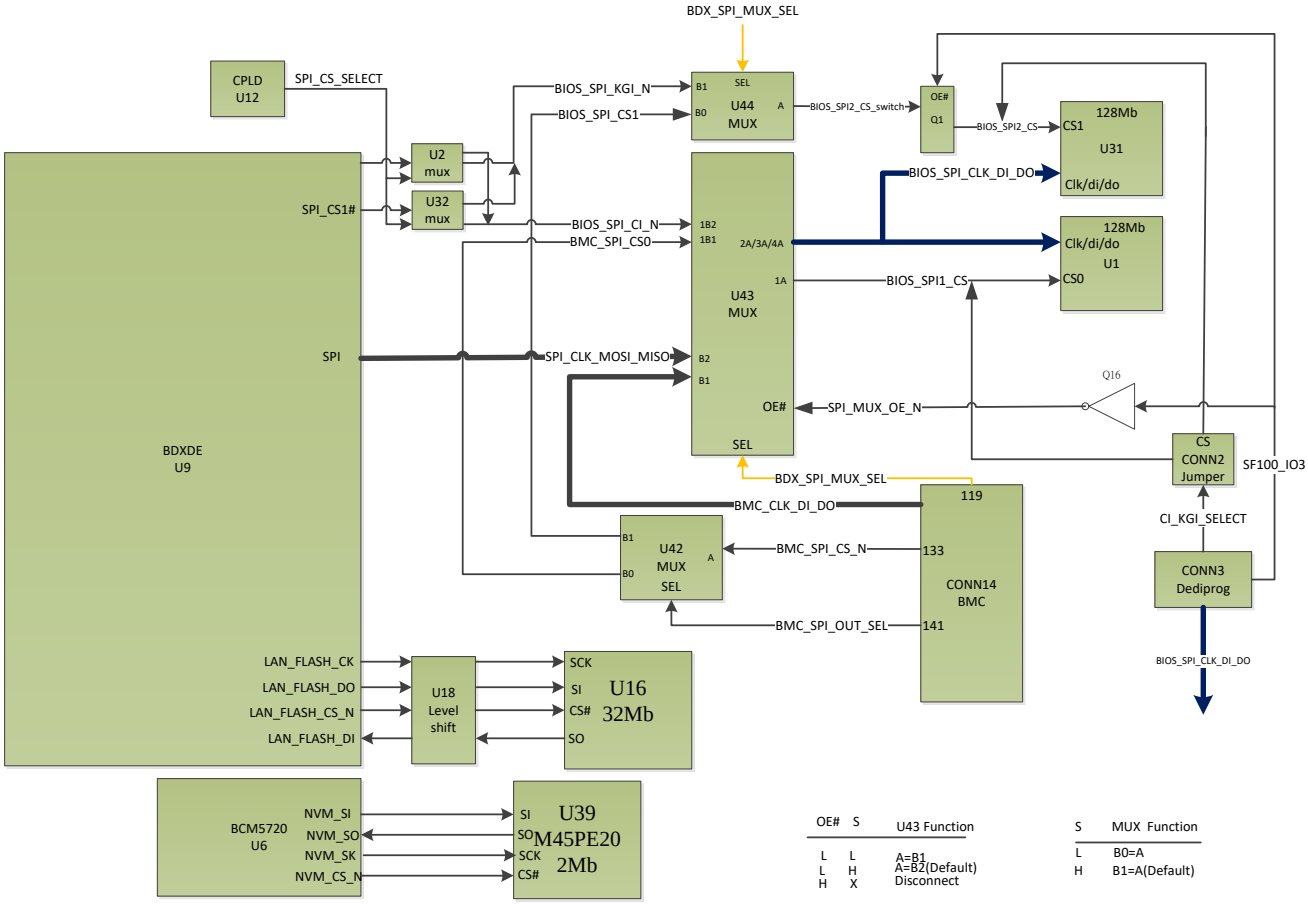


Figure 3-3 FLASH Connection

3.3.1. Bios Flash Upgrade

There are two methods to upgrade the system bios flash:

a. Using SF100 DEDIPROG programmer

b. Using BMC module

3.3.1.1. Using SF100/SF600 DEDIPROG programmer

1. Preparing the SF100 / SF600

BIOS SPI Flash Update

- Tools Required:
  - Host Windows* PC with USB port
  - DediProg* SF600 SPI Flash Programmer
  - SF600 cable Adapter with an 8-pin header
  - USB cable
    - http://www.dediprog.com/
- Required Software:
  - Download and install the software corresponding to th DediProg* SF600 SPI Flash Programmer tool onto the Windows* PC
    - http://www.dediprog.com/

2. Select flash

U1: Current BIOS Image (CI)

U31: Known Good BIOS Image (KGI)

3. Connect the SF100/SF600 connect on CONN3

4. For CI flash, put jumper on CONN2 = 1-2

5. For KGI flash, put jumper on CONN2 = 2-3

3.3.2. 10GBE firmware flash upgrade

The U16 10GBE flash could be upgrade by SW

3.3.3. BCM5720 firmware flash upgrade

The U39 BCM5720 flash could be upgrade by SW.

3.4. DDR4

The Intel Broadwell-DE CPU family can support memory DDR3 and DDR4 that need via strap pin DDR3_4_STRAP to configure which one be supported.

Currently the board supports two DDR4 SODIMM modules with ECC, so the DDR3_4_STRAP should be pull to high.

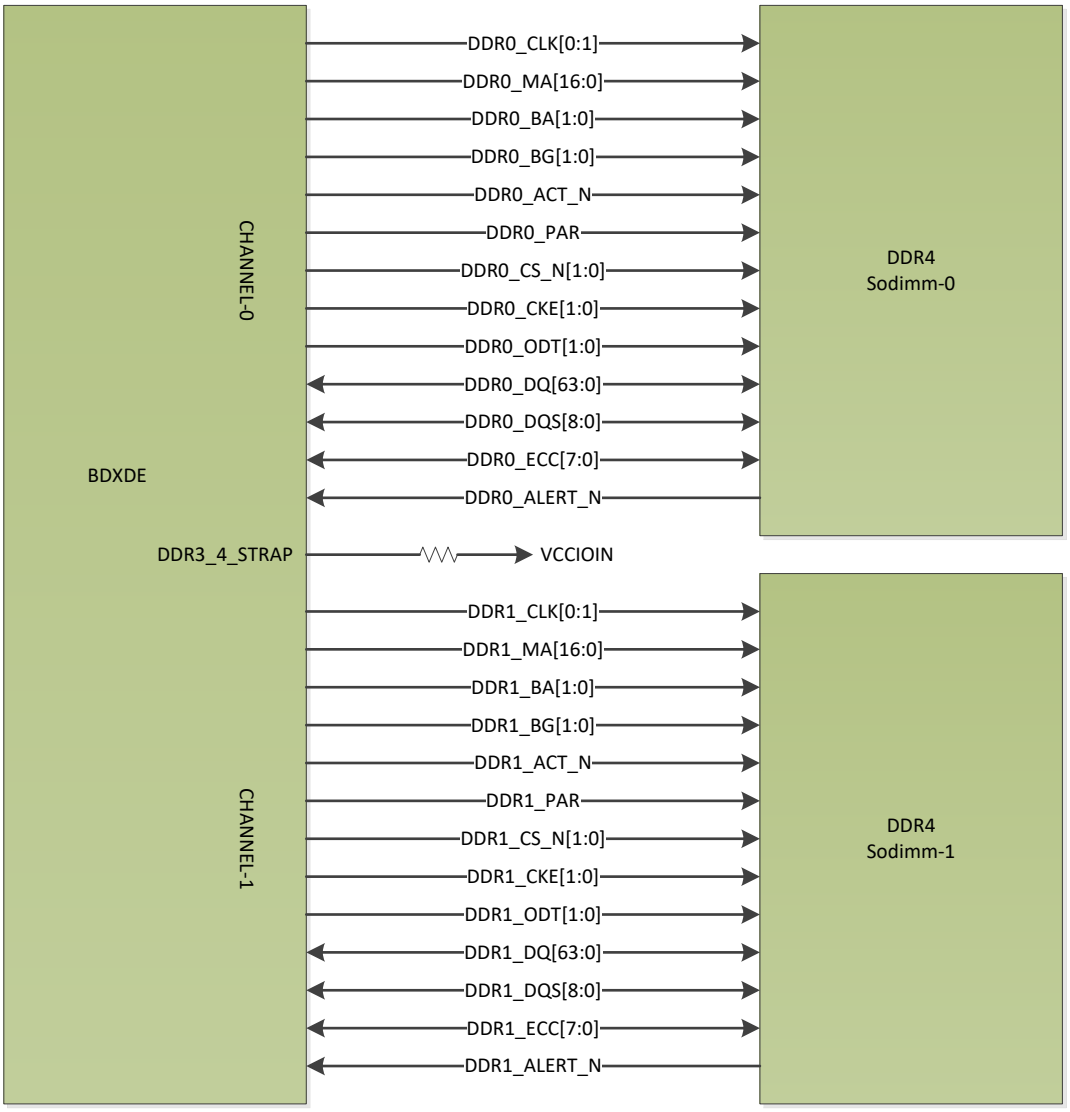


Figure 3-4 RAM Connection

3.5. PCIe

The CPU board has to provide the x4 PCIE Gen3 and x1 PCIE Gen2 to main board. The x4 PCIE GEN3 is used to connect the BCM56960 for control path, the PCIE GEN2 x1 is sued to communicate the OOB.

There are other PCIE GEN2 that connect to on board MAC BCM5720 and BMC module.

The PCIE interface connected to BCM5720 is PCIE GEN2 x2.

The PCIE interface connected to BMC module is PCIE GEN2 x1, which is used to active the graphic inside the BMC chip to achieve the vKVM and vMedia function through IPMI when the BMC chip uses AST2400.

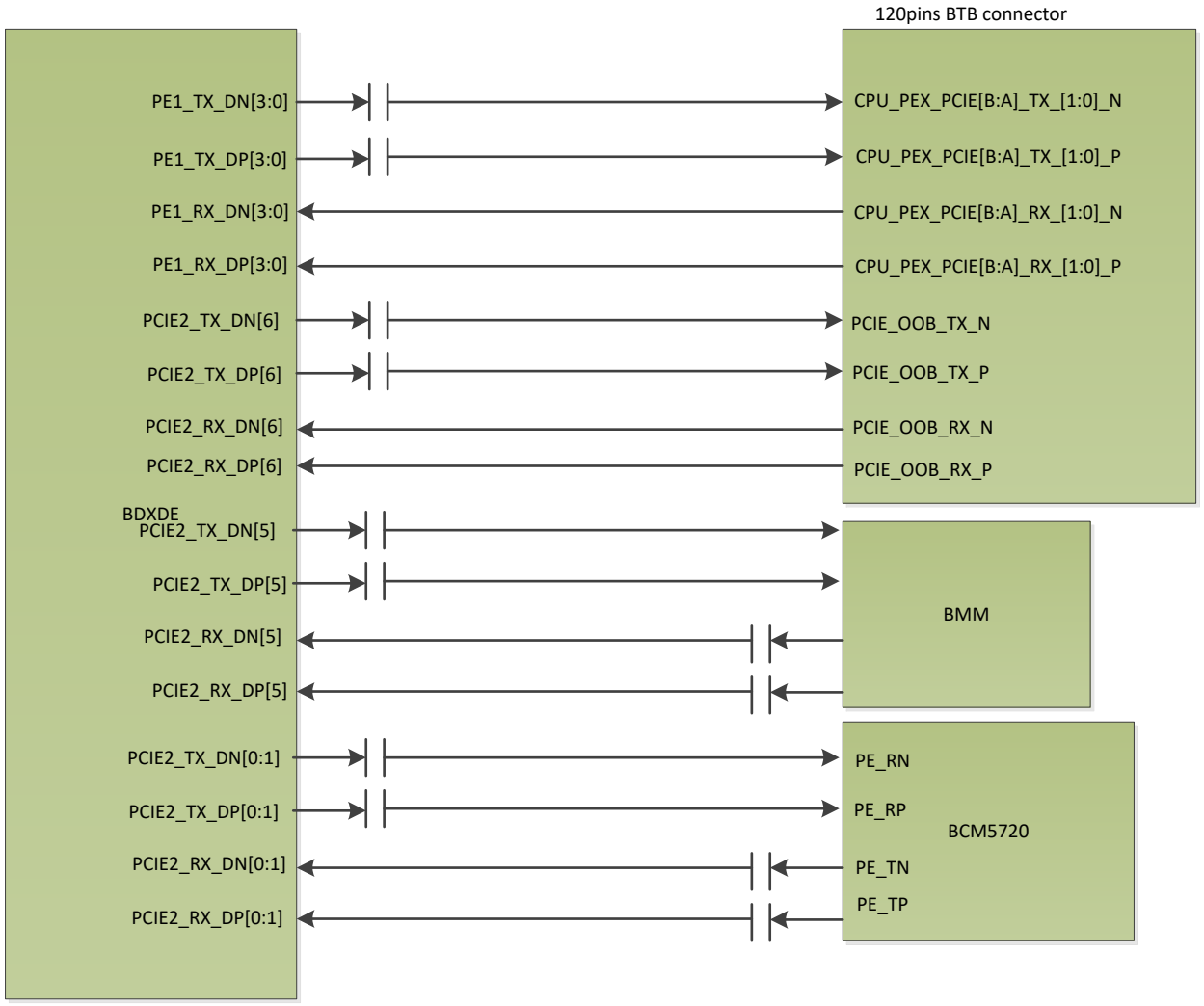


Figure 3-5 PCIe Topology

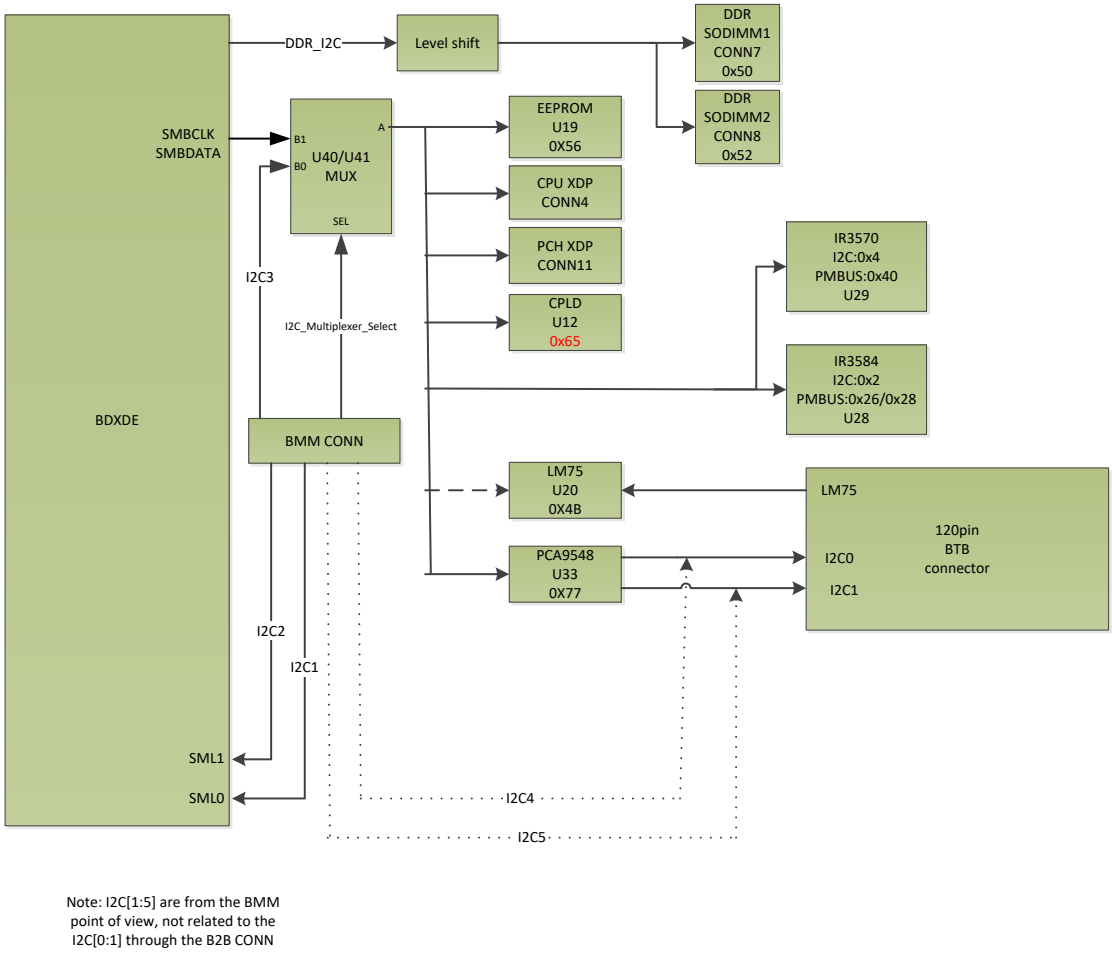
3.6. SMbus/I2C

The SMbus from Broadwell-DE can access the CPU board and main board device via SMBUS0.

The U40/U41 multiplexers are used to prevent multi-master issues on the SMBUS.

The BMC module could use the SMBUS when the I2C_multiplexer_select pin is driven from high to low.

In order to prevent the hang-up issue which occurred when the CPU is accessing the SMBUS and BMC module want to take the bus master (I2C_multiplexer_select would be driven low), if the BMC module is installed, BMC would be the master for all SMBUS, CPU would ask BMC for SMBUS information via LPC by IPMI.



Note: I2C[1:5] are from the BMM point of view, not related to the I2C[0:1] through the B2B CONN

Figure 3-6 CPU Board SMBUS Connection

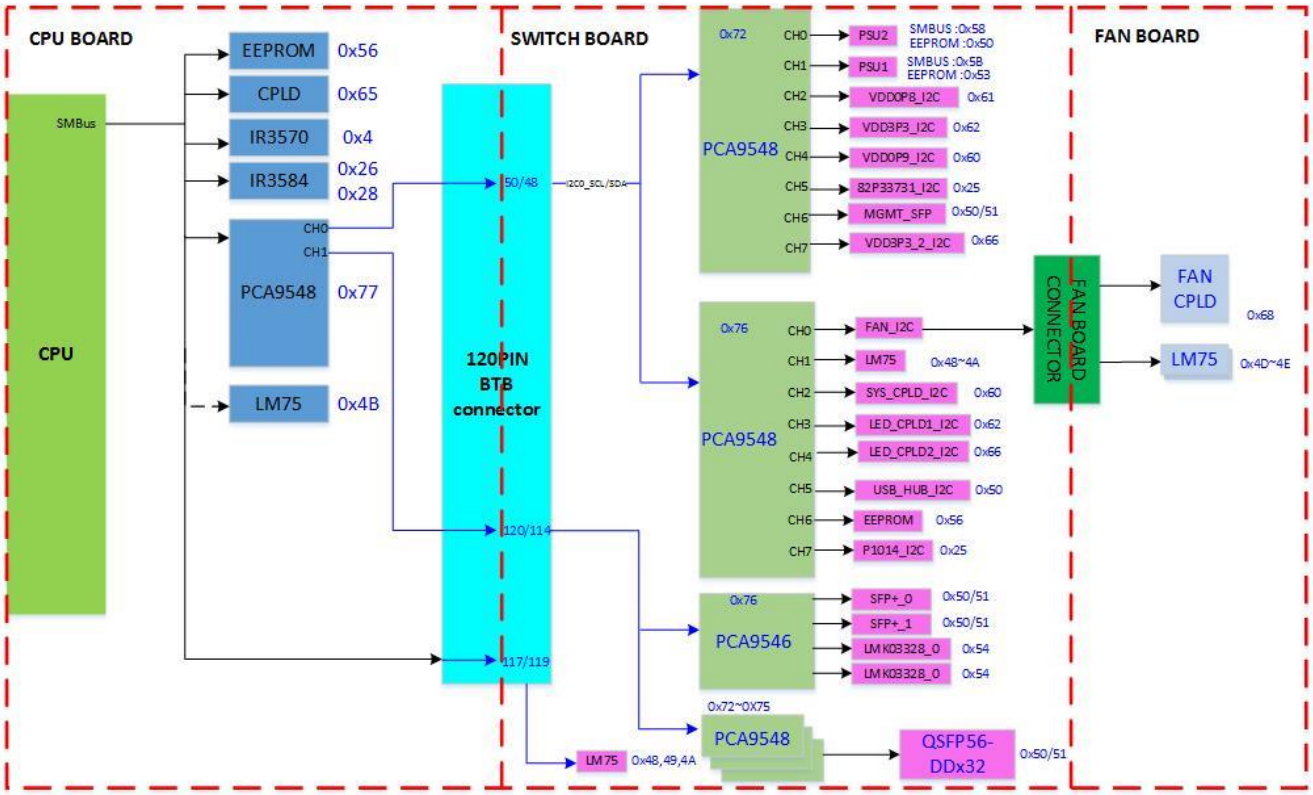


Figure 3-7 Main Board SMBUS Connection

3.7. UART

There is a RJ-45 type console port in front panel connected to CPU UART_1 interface. The interface supports asynchronous mode with default eight data bits, one stop bit, and no parity. The unit will operate at any one of the following baud rates, 9600, 19200, 38400, 57600 and 115200 bps.

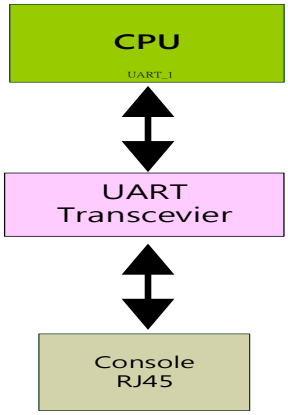


Figure 3-8 UART Connection

Table 3- 4 RJ-45 Type Console Pin Definition

Pin number	Pin name	Pin number	Pin name
1	RTS	2	
3	TXD	4	GND
5	GND	6	RXD
7		8	CTS

3.8. USB

There are four USB 2.0 interfaces in the project.

The USB-0 via the 120pins BTB connector to switch board is for chassis USB connector.

The USB-1 is for debug function.

The USB-2 connects to eUSB module for OS access.

The USB-3 is connected to BMC module for vMEDIA function.

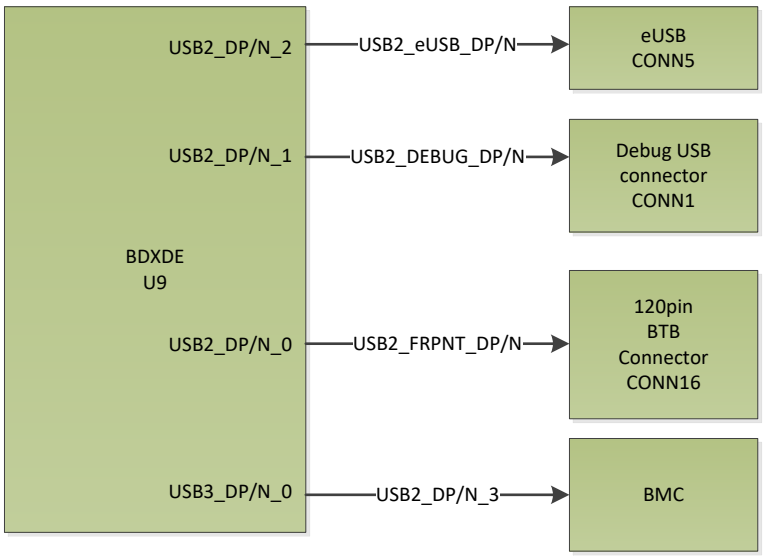


Figure 3-9 USB Connection

3.9. SATA

The CPU board supports 2 SATA SSD devices via SATA 3.0 interface.
SATA 3.0 CH0 support mSATA SSD module.
SATA 3.0 CH1 support m.2 SSD module.
The following table shows the mSATA and m.2 SSD module dimension and size.

Table 3- 5 SATA SSD Module Table

Type	Dimension	Capacity
mSATA SSD	50.8mm x 29.85mm x 4.0mm	16GB~512GB (option)
M.2 SSD	42.0mm × 22.0mm × 3.5mm	32GB~256GB (default)
	80.0mm x 22.0mm	32GB~512GB (option)

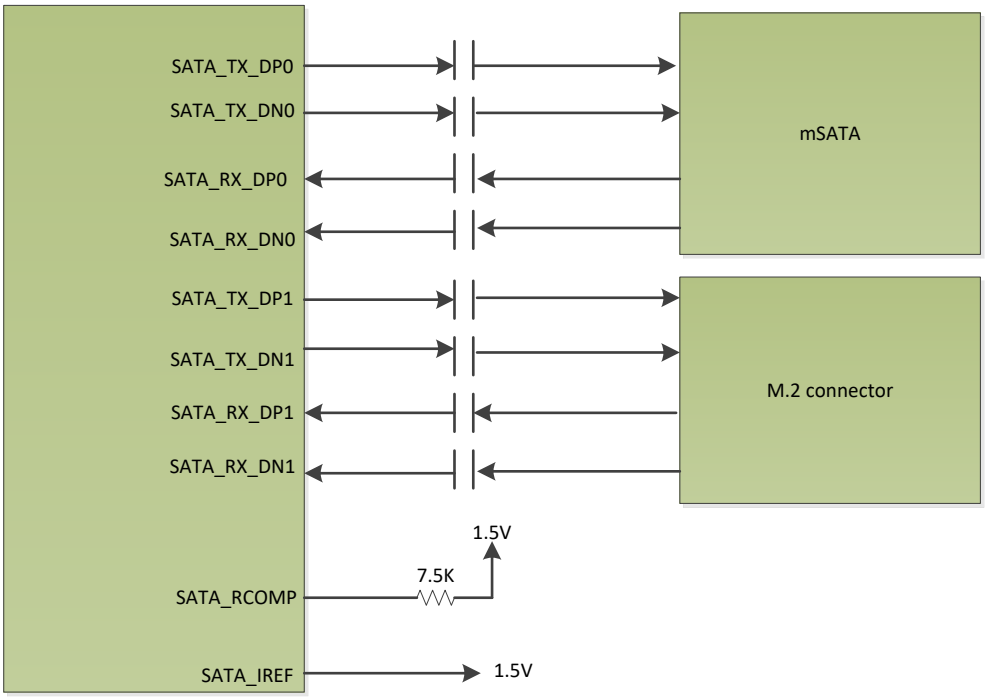


Figure 3-10 SATA Connection

3.10. GPIO

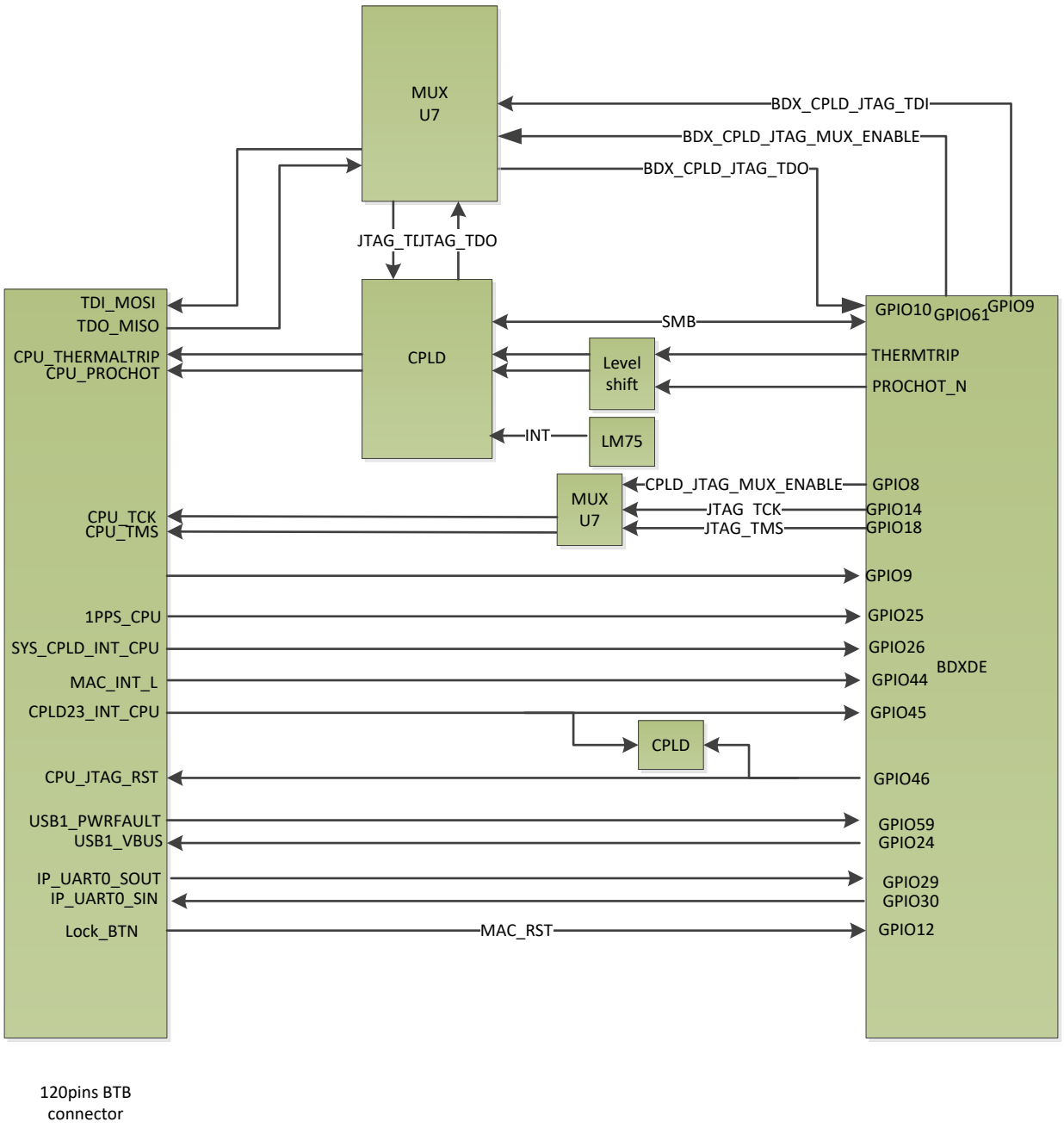


Figure 3-11 GPIO Connection

The following table is the GPIO function description of BDXDE CPU.

Table 3- 6 GPIO table

Pin name	GPIO_USE_SEL	GPIO_IO_SEL	function

	1: GPIO	1: input	
	0: Native	0: output	
GPIO0	0	X	BMBUSY#
GPIO1	1	0	Watch dog event clear indicator
GPIO2	0	X	NC
GPIO3	0	X	NC
GPIO4	1	1	CPU to PCH Throttle event interrupt
GPIO5	0	X	NC
GPIO6	1	0	JTAG enable, enable JTAG multiplexer to update CPLD code from CPU. 1: enable the JTAG multiplexer 0: disable the JTAG multiplexer
GPIO7	0	X	NC
GPIO8	1	0	JTAG Multiplexer select, which select the JTAG signals from CPU would go to CPLD or main board 1: to CPLD (default) 0: to Main board
GPIO9	1	0	XDP_NOA5_PCH/ BDX_CPLD_JTAG_TDI When configure to be BDX_CPLD_JTAG_TDI, which is CPU JTAG output
GPIO10	1	1	XDP_NOA6_PCH/ BDX_CPLD_JTAG_TDO When this pin configure to BDX_CPLD_JTAG_TDO , which is CPU JTAG input
GPIO11	0	X	SMBALERT#
GPIO12	1	0	Reset MAC, to do the sleep function.
GPIO14	1	0	XDP_NOA7_PCH/ BDX_CPLD_JTAG_TCK

GPIO15	1	0	SOC_FPGA_CLK
GPIO16	1	0	FM_THROTTLE_PCH_N/ FM_THROTTLE_N
GPIO17	1	1	BMC present detect
GPIO18	1	0	XDP_NOA14_PCH/ BDX_CPLD_JTAG_TMS
GPIO19	1	BI-DIR	XDP_NOA9_PCH
GPIO20	1	0	FM_SMI_ACTIVE_PCH_N/ FM_SMI_ACTIVE_CPLD_N
GPIO21	1	BI-DIR	XDP_NOA8_PCH
GPIO22	1	0	SCLOCK
GPIO23	0	X	NC
GPIO24	0	0	NC
GPIO25	1	1	1PPS_CPU
GPIO26	1	1	SYS_CPLD_INT_CPU
GPIO27	1	1	SOC_FPGA_DIN
GPIO28	1	0	SOC_FPGA_DOUT
GPIO29	1	0	IP_UART0_SOUT
GPIO30	1	1	IP_UART0_SIN
GPIO31	1	1	SMB_PWR_ALERT
GPIO32	X	X	NC
GPIO33	X	X	NC
GPIO35	1	0	FM_NMI_EVENT_PCH_N/ FM_NMI_EVENT_CPLD_N
GPIO36	1	0	ADR_STATUS_RD
GPIO37	1	1	ADR_STATUS_CLR
GPIO38	0	0	SLOAD
GPIO39	0	0	SDATAOUT0
GPIO40	0	BI	XDP_NOA1_PCH
GPIO41	1	0	XDP_NOA2_PCH/ CPLD_CONFIG_CLK
GPIO42	1	BI	XDP_NOA3_PCH/

			CPLD_CONFIG_DATA
GPIO43	1	0	XDP_NOA4_PCH / ADR_MCU_INIT
GPIO44	0	1	NC
GPIO45	1	1	CPLD23_INT_CPU
GPIO46	1	0	CPU_JTAG_RST
GPIO48	1	0	SDATAOUT1
GPIO49	1	0	FM_CPU_PROCHOT_PCH_N/ FM_PROCHOT_N
GPIO50	X	X	NC
GPIO51	1	1	4.7k pull to 3.3V
GPIO52	1	1	CPU_SV
GPIO53	1	1	1k pull to gnd
GPIO54	X	X	NC
GPIO55	1	1	FM_BIOS_RCRV_BOOT_N
GPIO57	1	1	FM_ME_RCRV_N
GPIO58	0	X	SML1_CLK
GPIO59	1	BI	XDP_NOA0_PCH
GPIO60	0	X	SML0ALERT#
GPIO61	X	X	NC
GPIO62	0	X	SUSCLK_33K
GPIO65	0	X	NC
GPIO67	0	X	NC
GPIO68	1	1	CPLD interrupt
GPIO69	0	X	NC
GPIO70	0	X	NC
GPIO71	0	X	NC
GPIO72	1	1	1K pull to 3.3V
GPIO74	0	X	SML1ALERT#/TEMP_ALERT#.
GPIO75	0	X	SML1DATA

4. Sub-system of BCM5720

4.1. Ethernet Controller for Management Port

There is a Ethernet controller, Broadcom BCM5720, used in Azurite to connect the management PHY (BCM54616S).

The BCM5720 combines dual tri-speed IEEE 802.3 compliant MACs with dual 1000BASE-X/SGMII SerDes transceivers or dual 10/100/1000 Ethernet transceivers. The device provides a PCIe v2.1 compliant host interface, which can operate at 5GTs or 2.5GTs/s x2 link width. The management PHY BCM54616S support one 10/ 100/ 1000M RJ45 and GE SFP combo port.

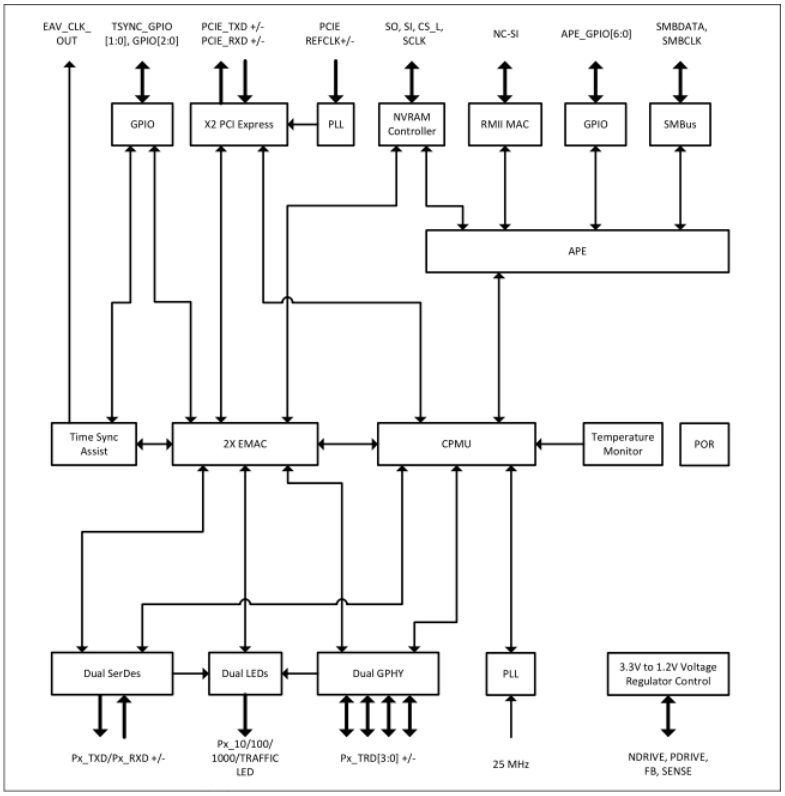


Figure 4-1 BCM5720 Block Diagram

The BMC5720 communicates CPU via PCIE GEN2 x2, and connect to the management port PHY BCM54616S on main board via SGMII interface.

The NCSI interface is used to connect the BMC module to support share NIC function.

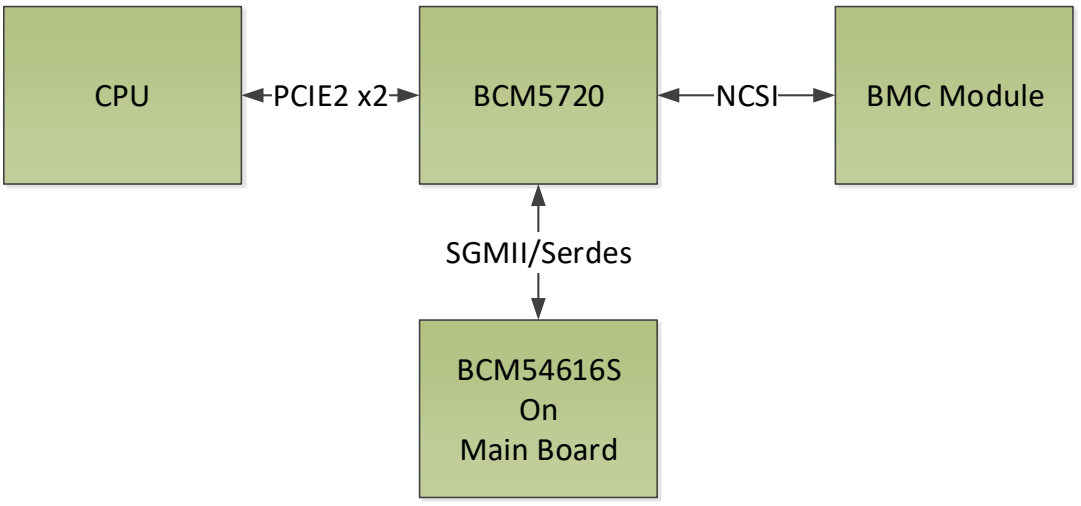


Figure 4-2 BCM5720 Topology

4.2. Interrupt

CPLD in switch board will collect all interrupts in switch board from different devices, and then pass to CPU. Those devices are as below.

MAC (BCM56980)
MGMT PHY(BCM54616S)
Thermal sensor(LM75)
Fan
IDT 82P33731
QSFP56-DD transceiver

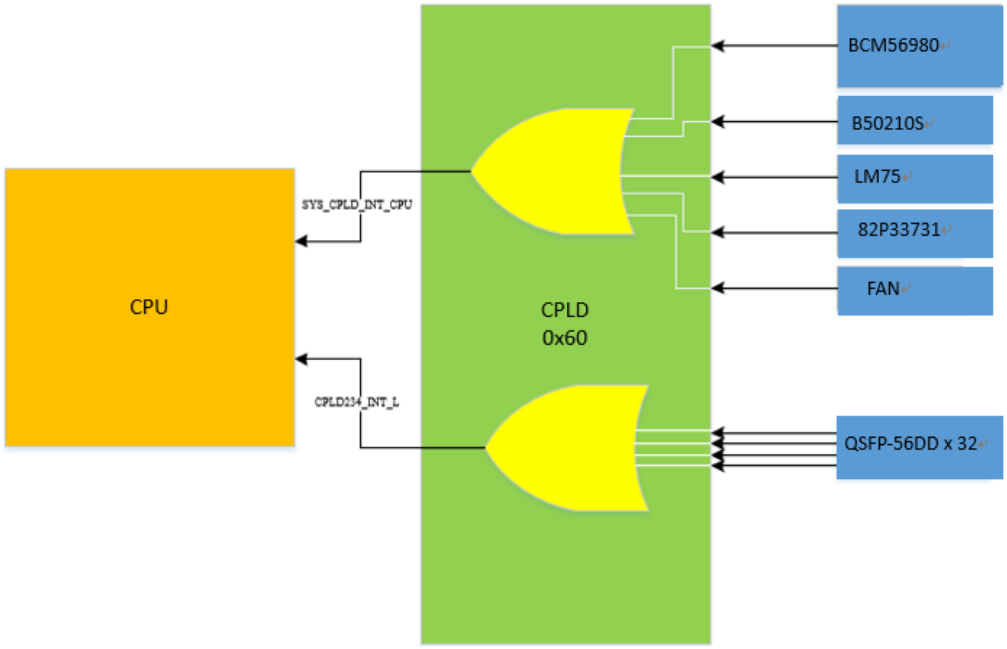


Figure 4-3 Interrupt Connection (未完成)

4.3. Thermal system

4.3.1. Temperature sensor

There are three temperature sensors in AS9700-32X system, and the locations are as the picture below. CPU can access the sensor via I2C interface, and the sensor has the interrupt signal connect with CPLD for over-temp event application.

The temperature sensor solution is “LIN LM75BD 2.8-5.5V TEMP MINOTOR SO8 LT/LF NXP”

The thermal alarm will be 70 degree at initial value and it is via thermal sensor’s interrupt to CPU module. The temperature value will be optimized after thermal test result.

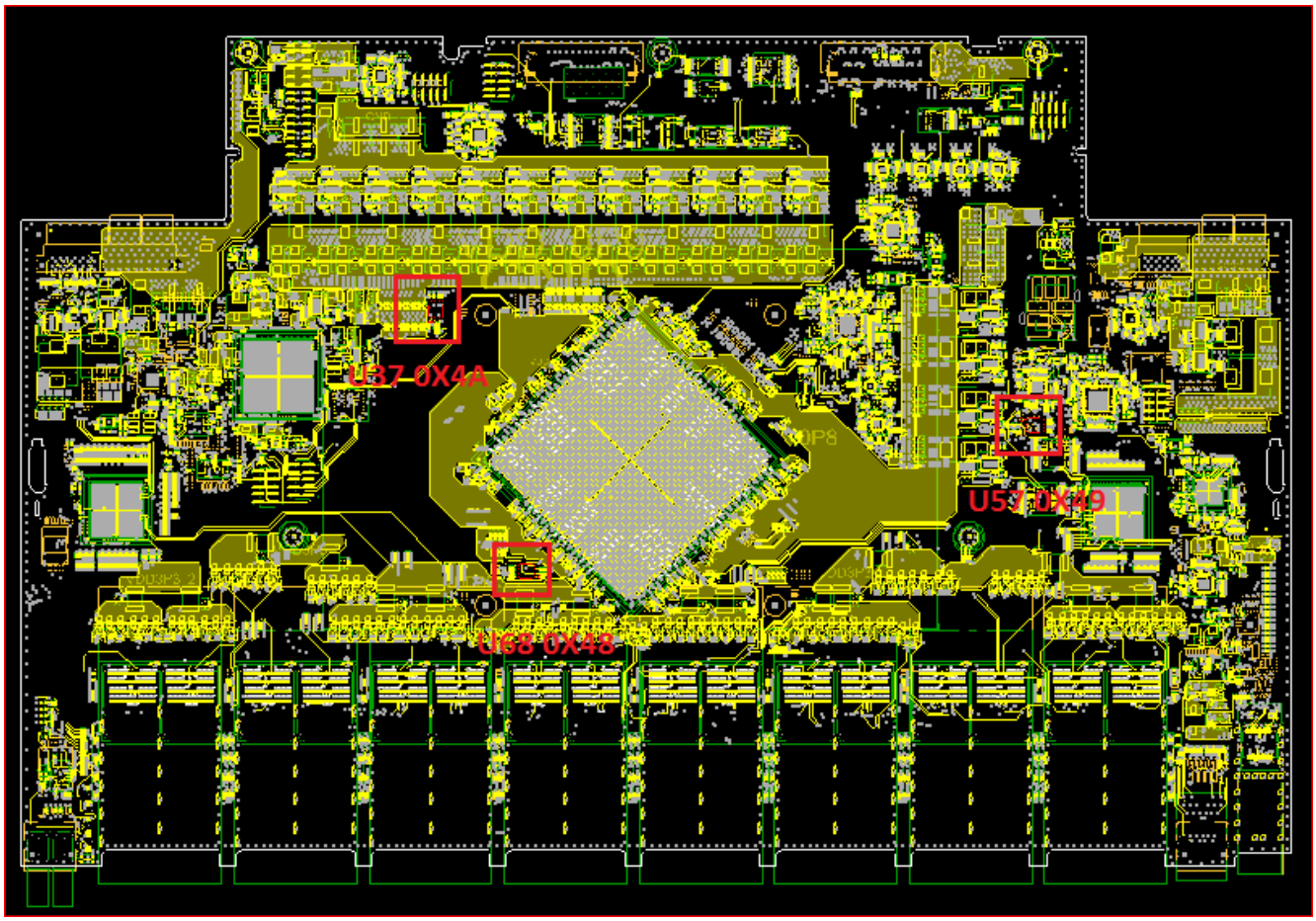


Figure 4-4 Switch board - Temp sensor location

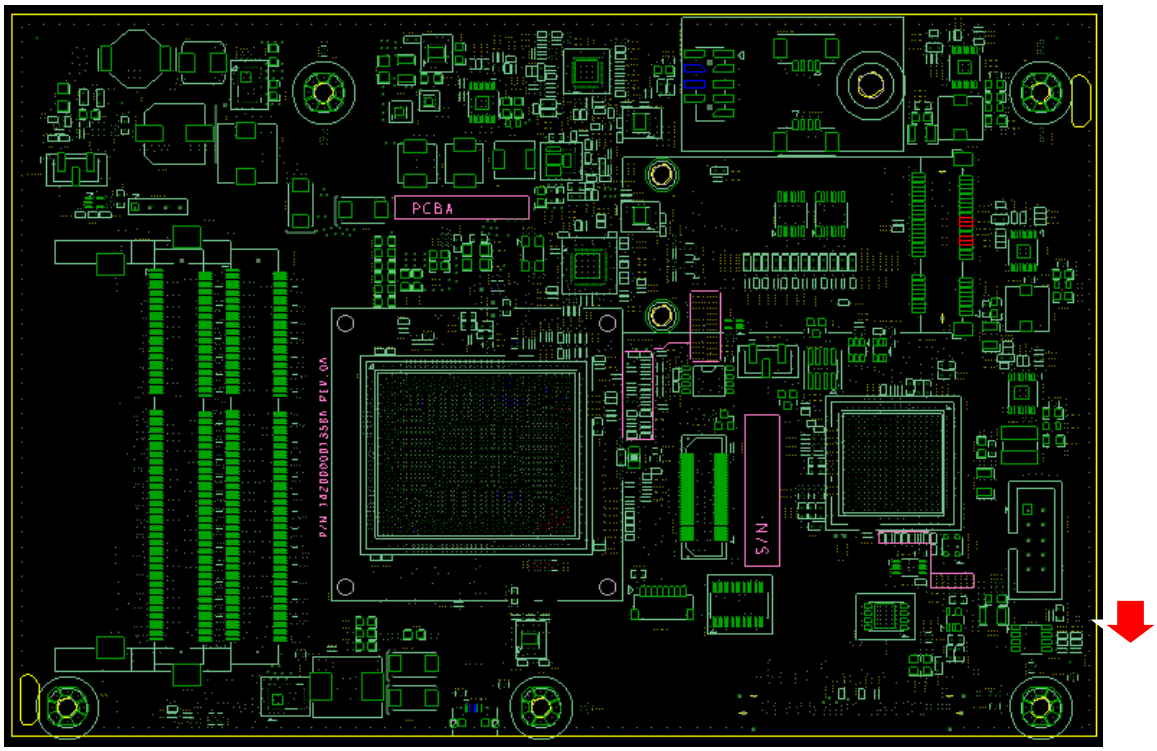


Figure 4-5 CPU board - Temp sensor location

4.3.2. Fan controller system

The Fan board has a CPLD to do the fan controller function. The CPLD on the Fan board can control the Fan's PWM signal for adjust Fan speed and count the Fan's Tach signal for Fan speed reporting. CPU can read the thermal sensor to get thermal information, and then adjust Fan speed to reduce system's thermal. The Fan's CPLD had included I2C thermal watchdog to avoid system shutdown. If the register count to zero, the Fan speed will be set to high speed.

The CPLD information is "CPLD 5M1270ZF256C5N 3.3V FBGA256 LT/LF ALTERA"

4.4. IDT 82P33731

4.4.1. Configurations of IDT 82P33731

Pin Number	Pin Name	Function Description
B11 C11	MPU_MODE1/ I2CM_SCL MPU_MODE0/ I2CM_SDA	During reset, these pins determine the default value of the MPU_SEL_CNFG[1:0] bits as follows: 00: I2C mode 01 ~ 10: Reserved 11: I2C master (EEPROM) mode I2CM_SCL: Serial Clock Line

		In I2C master mode, the serial clock is output on this pin. I2CM_SDA: Serial Data Input for I2C Master Mode In I2C master mode, this pin is used as the for the serial data.
K8	MS/SL	MS/SL: Master / Slave Selection This pin, together with the MS_SL_CTRL bit, controls whether the device is configured as the Master or as the Slave. The signal level on this pin is reflected by the MASTER_SLAVE bit.
H1 J1 J2	XO_FREQ0/ LOS0 XO_FREQ1/ LOS1 XO_FREQ2/ LOS2	XO_FREQ0 ~ XO_FREQ2: These pins set the oscillator frequency. XO_FREQ[2:0] Oscillator Frequency (MHz) 000 10.000 001 12.800 010 13.000 011 19.440 100 20.000 101 24.576 110 25.000 111 30.720 LOS0 ~ LOS2 - These pins are used to disqualify input clocks. See input clocks section for more details. After reset, this pin takes on the operation of LOS0-LOS2

5. Switch Sub-system of BCM56980

The BCM56980 supports high-bandwidth, glueless network connectivity up to 12.8 TB/s on a single chip. It incorporates 32 BlackhawkCore, where each BlackhawkCore can operate at 200G/ 400Gbps. The device also supports an x4 PCIe interface that can operate at Gen 3.0 speed to local CPU.

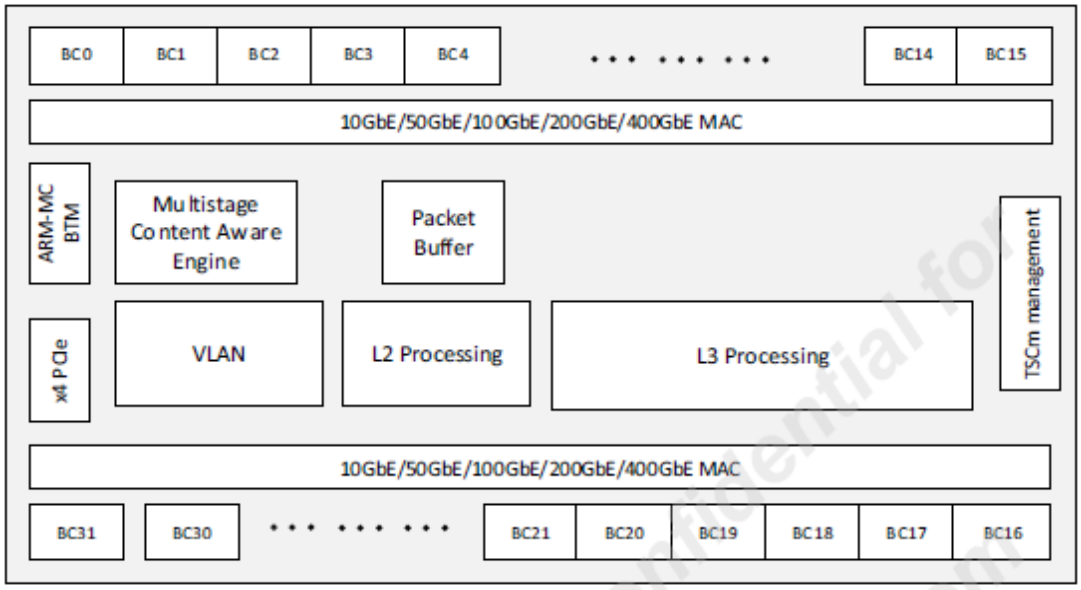


Figure 5-1 BCM56980 Block Diagram

5.1. Port Mapping

Table 5-1 AS9716-32X port mapping

Port mapping Date: 2018/03/20 Ver: V01 Author: Chaohua Chung				TH3 has ITM X2, Pipe x 8 Balckhawk x 32, Merlin x 1			
ITM number	Pipe Number	SerDes Core number	Physical Port Number	BC-X Lane-X	QSFP-DD TX (From Mac)	QSFP-DD RX (To Mac)	Front Port
0	0	Blackhawk 0	1	0	1	5	21
0	0	Blackhawk 0	2	1	4	4	21
0	0	Blackhawk 0	3	2	8	2	21
0	0	Blackhawk 0	4	3	7	6	21
0	0	Blackhawk 0	5	4	3	8	21
0	0	Blackhawk 0	6	5	2	7	21
0	0	Blackhawk 0	7	6	5	1	21
0	0	Blackhawk 0	8	7	6	3	21

Port mapping Date: 2018/03/20 Ver: V01 Author: Chaohua Chung				TH3 has ITM X2, Pipe x 8 Balckhawk x 32, Merlin x 1			
ITM number	Pipe Number	SerDes Core number	Physical Port Number	BC-X Lane-X	QSFP-DD TX (From Mac)	QSFP-DD RX (To Mac)	Front Port
0	0	Blackhawk 1	9	0	7	4	22
0	0	Blackhawk 1	10	1	6	8	22
0	0	Blackhawk 1	11	2	3	7	22
0	0	Blackhawk 1	12	3	1	3	22
0	0	Blackhawk 1	13	4	5	1	22
0	0	Blackhawk 1	14	5	2	5	22
0	0	Blackhawk 1	15	6	4	6	22
0	0	Blackhawk 1	16	7	8	2	22
0	0	Blackhawk 2	17	0	1	7	23
0	0	Blackhawk 2	18	1	3	3	23
0	0	Blackhawk 2	19	2	5	4	23
0	0	Blackhawk 2	20	3	6	2	23
0	0	Blackhawk 2	21	4	4	8	23
0	0	Blackhawk 2	22	5	7	6	23
0	0	Blackhawk 2	23	6	2	1	23
0	0	Blackhawk 2	24	7	8	5	23
0	0	Blackhawk 3	25	0	1	7	24
0	0	Blackhawk 3	26	1	5	3	24
0	0	Blackhawk 3	27	2	2	8	24
0	0	Blackhawk 3	28	3	7	1	24
0	0	Blackhawk 3	29	4	8	2	24
0	0	Blackhawk 3	30	5	3	6	24
0	0	Blackhawk 3	31	6	4	4	24
0	0	Blackhawk 3	32	7	6	5	24
0	1	Blackhawk 4	33	0	8	5	10
0	1	Blackhawk 4	34	1	7	1	10
0	1	Blackhawk 4	35	2	4	6	10
0	1	Blackhawk 4	36	3	2	3	10
0	1	Blackhawk 4	37	4	6	8	10
0	1	Blackhawk 4	38	5	5	4	10
0	1	Blackhawk 4	39	6	1	2	10
0	1	Blackhawk 4	40	7	3	7	10

Port mapping Date: 2018/03/20 Ver: V01 Author: Chaohua Chung				TH3 has ITM X2, Pipe x 8 Balckhawk x 32, Merlin x 1			
ITM number	Pipe Number	SerDes Core number	Physical Port Number	BC-X Lane-X	QSFP-DD TX (From Mac)	QSFP-DD RX (To Mac)	Front Port
0	1	Blackhawk 5	41	0	7	6	9
0	1	Blackhawk 5	42	1	8	5	9
0	1	Blackhawk 5	43	2	6	2	9
0	1	Blackhawk 5	44	3	4	4	9
0	1	Blackhawk 5	45	4	1	8	9
0	1	Blackhawk 5	46	5	3	7	9
0	1	Blackhawk 5	47	6	2	1	9
0	1	Blackhawk 5	48	7	5	3	9
0	1	Blackhawk 6	49	0	4	8	11
0	1	Blackhawk 6	50	1	7	4	11
0	1	Blackhawk 6	51	2	6	2	11
0	1	Blackhawk 6	52	3	5	3	11
0	1	Blackhawk 6	53	4	1	7	11
0	1	Blackhawk 6	54	5	8	6	11
0	1	Blackhawk 6	55	6	2	1	11
0	1	Blackhawk 6	56	7	3	5	11
0	1	Blackhawk 7	57	0	5	8	12
0	1	Blackhawk 7	58	1	6	7	12
0	1	Blackhawk 7	59	2	2	3	12
0	1	Blackhawk 7	60	3	8	1	12
0	1	Blackhawk 7	61	4	3	2	12
0	1	Blackhawk 7	62	5	1	4	12
0	1	Blackhawk 7	63	6	4	6	12
0	1	Blackhawk 7	64	7	7	5	12
1	2	Blackhawk 8	65	0	2	6	2
1	2	Blackhawk 8	66	1	8	2	2
1	2	Blackhawk 8	67	2	7	5	2
1	2	Blackhawk 8	68	3	4	1	2
1	2	Blackhawk 8	69	4	1	4	2
1	2	Blackhawk 8	70	5	3	8	2
1	2	Blackhawk 8	71	6	6	7	2
1	2	Blackhawk 8	72	7	5	3	2

Port mapping Date: 2018/03/20 Ver: V01 Author: Chaohua Chung				TH3 has ITM X2, Pipe x 8 Balckhawk x 32, Merlin x 1			
ITM number	Pipe Number	SerDes Core number	Physical Port Number	BC-X Lane-X	QSFP-DD TX (From Mac)	QSFP-DD RX (To Mac)	Front Port
1	2	Blackhawk 9	73	0	8	2	1
1	2	Blackhawk 9	74	1	3	4	1
1	2	Blackhawk 9	75	2	6	6	1
1	2	Blackhawk 9	76	3	4	5	1
1	2	Blackhawk 9	77	4	7	8	1
1	2	Blackhawk 9	78	5	1	7	1
1	2	Blackhawk 9	79	6	2	3	1
1	2	Blackhawk 9	80	7	5	1	1
1	2	Blackhawk 10	81	0	2	7	3
1	2	Blackhawk 10	82	1	5	3	3
1	2	Blackhawk 10	83	2	6	8	3
1	2	Blackhawk 10	84	3	7	4	3
1	2	Blackhawk 10	85	4	1	2	3
1	2	Blackhawk 10	86	5	8	6	3
1	2	Blackhawk 10	87	6	4	5	3
1	2	Blackhawk 10	88	7	3	1	3
1	2	Blackhawk 11	89	0	6	8	4
1	2	Blackhawk 11	90	1	5	5	4
1	2	Blackhawk 11	91	2	4	7	4
1	2	Blackhawk 11	92	3	2	3	4
1	2	Blackhawk 11	93	4	7	4	4
1	2	Blackhawk 11	94	5	1	6	4
1	2	Blackhawk 11	95	6	8	1	4
1	2	Blackhawk 11	96	7	3	2	4
1	3	Blackhawk 12	97	0	8	3	5
1	3	Blackhawk 12	98	1	1	7	5
1	3	Blackhawk 12	99	2	2	6	5
1	3	Blackhawk 12	100	3	3	2	5
1	3	Blackhawk 12	101	4	6	1	5
1	3	Blackhawk 12	102	5	7	8	5
1	3	Blackhawk 12	103	6	4	4	5
1	3	Blackhawk 12	104	7	5	5	5

Port mapping Date: 2018/03/20 Ver: V01 Author: Chaohua Chung				TH3 has ITM X2, Pipe x 8 Balckhawk x 32, Merlin x 1			
ITM number	Pipe Number	SerDes Core number	Physical Port Number	BC-X Lane-X	QSFP-DD TX (From Mac)	QSFP-DD RX (To Mac)	Front Port
1	3	Blackhawk 13	105	0	1	2	6
1	3	Blackhawk 13	106	1	3	6	6
1	3	Blackhawk 13	107	2	6	5	6
1	3	Blackhawk 13	108	3	5	1	6
1	3	Blackhawk 13	109	4	2	7	6
1	3	Blackhawk 13	110	5	7	3	6
1	3	Blackhawk 13	111	6	4	4	6
1	3	Blackhawk 13	112	7	8	8	6
1	3	Blackhawk 14	113	0	5	3	7
1	3	Blackhawk 14	114	1	6	4	7
1	3	Blackhawk 14	115	2	1	7	7
1	3	Blackhawk 14	116	3	3	8	7
1	3	Blackhawk 14	117	4	7	6	7
1	3	Blackhawk 14	118	5	8	2	7
1	3	Blackhawk 14	119	6	2	5	7
1	3	Blackhawk 14	120	7	4	1	7
1	3	Blackhawk 15	121	0	1	1	8
1	3	Blackhawk 15	122	1	5	2	8
1	3	Blackhawk 15	123	2	8	4	8
1	3	Blackhawk 15	124	3	3	6	8
1	3	Blackhawk 15	125	4	7	5	8
1	3	Blackhawk 15	126	5	2	7	8
1	3	Blackhawk 15	127	6	6	3	8
1	3	Blackhawk 15	128	7	4	8	8
1	4	Blackhawk 16	129	0	1	5	13
1	4	Blackhawk 16	130	1	3	2	13
1	4	Blackhawk 16	131	2	8	4	13
1	4	Blackhawk 16	132	3	4	6	13
1	4	Blackhawk 16	133	4	7	8	13
1	4	Blackhawk 16	134	5	2	7	13
1	4	Blackhawk 16	135	6	5	1	13
1	4	Blackhawk 16	136	7	6	3	13

Port mapping Date: 2018/03/20 Ver: V01 Author: Chaohua Chung				TH3 has ITM X2, Pipe x 8 Balckhawk x 32, Merlin x 1			
ITM number	Pipe Number	SerDes Core number	Physical Port Number	BC-X Lane-X	QSFP-DD TX (From Mac)	QSFP-DD RX (To Mac)	Front Port
1	4	Blackhawk 17	137	0	7	4	14
1	4	Blackhawk 17	138	1	6	8	14
1	4	Blackhawk 17	139	2	1	7	14
1	4	Blackhawk 17	140	3	5	3	14
1	4	Blackhawk 17	141	4	3	6	14
1	4	Blackhawk 17	142	5	4	2	14
1	4	Blackhawk 17	143	6	2	5	14
1	4	Blackhawk 17	144	7	8	1	14
1	4	Blackhawk 18	145	0	3	7	15
1	4	Blackhawk 18	146	1	6	3	15
1	4	Blackhawk 18	147	2	5	8	15
1	4	Blackhawk 18	148	3	1	4	15
1	4	Blackhawk 18	149	4	7	2	15
1	4	Blackhawk 18	150	5	8	6	15
1	4	Blackhawk 18	151	6	4	5	15
1	4	Blackhawk 18	152	7	2	1	15
1	4	Blackhawk 19	153	0	6	7	16
1	4	Blackhawk 19	154	1	8	8	16
1	4	Blackhawk 19	155	2	2	4	16
1	4	Blackhawk 19	156	3	5	1	16
1	4	Blackhawk 19	157	4	3	3	16
1	4	Blackhawk 19	158	5	7	5	16
1	4	Blackhawk 19	159	6	4	6	16
1	4	Blackhawk 19	160	7	1	2	16
1	5	Blackhawk 20	161	0	6	7	18
1	5	Blackhawk 20	162	1	7	6	18
1	5	Blackhawk 20	163	2	8	5	18
1	5	Blackhawk 20	164	3	4	1	18
1	5	Blackhawk 20	165	4	3	2	18
1	5	Blackhawk 20	166	5	2	4	18
1	5	Blackhawk 20	167	6	1	3	18
1	5	Blackhawk 20	168	7	5	8	18

Port mapping Date: 2018/03/20 Ver: V01 Author: Chaohua Chung				TH3 has ITM X2, Pipe x 8 Balckhawk x 32, Merlin x 1			
ITM number	Pipe Number	SerDes Core number	Physical Port Number	BC-X Lane-X	QSFP-DD TX (From Mac)	QSFP-DD RX (To Mac)	Front Port
1	5	Blackhawk 21	169	0	4	1	17
1	5	Blackhawk 21	170	1	2	5	17
1	5	Blackhawk 21	171	2	1	8	17
1	5	Blackhawk 21	172	3	8	3	17
1	5	Blackhawk 21	173	4	3	6	17
1	5	Blackhawk 21	174	5	6	2	17
1	5	Blackhawk 21	175	6	7	4	17
1	5	Blackhawk 21	176	7	5	7	17
1	5	Blackhawk 22	177	0	5	8	19
1	5	Blackhawk 22	178	1	3	6	19
1	5	Blackhawk 22	179	2	1	2	19
1	5	Blackhawk 22	180	3	6	4	19
1	5	Blackhawk 22	181	4	8	7	19
1	5	Blackhawk 22	182	5	4	5	19
1	5	Blackhawk 22	183	6	2	1	19
1	5	Blackhawk 22	184	7	7	3	19
1	5	Blackhawk 23	185	0	7	8	20
1	5	Blackhawk 23	186	1	2	4	20
1	5	Blackhawk 23	187	2	5	7	20
1	5	Blackhawk 23	188	3	6	3	20
1	5	Blackhawk 23	189	4	1	2	20
1	5	Blackhawk 23	190	5	8	6	20
1	5	Blackhawk 23	191	6	3	5	20
1	5	Blackhawk 23	192	7	4	1	20
0	6	Blackhawk 24	193	0	1	2	26
0	6	Blackhawk 24	194	1	4	6	26
0	6	Blackhawk 24	195	2	2	5	26
0	6	Blackhawk 24	196	3	7	1	26
0	6	Blackhawk 24	197	4	8	7	26
0	6	Blackhawk 24	198	5	6	3	26
0	6	Blackhawk 24	199	6	3	4	26
0	6	Blackhawk 24	200	7	5	8	26

Port mapping Date: 2018/03/20 Ver: V01 Author: Chaohua Chung				TH3 has ITM X2, Pipe x 8 Balckhawk x 32, Merlin x 1			
ITM number	Pipe Number	SerDes Core number	Physical Port Number	BC-X Lane-X	QSFP-DD TX (From Mac)	QSFP-DD RX (To Mac)	Front Port
0	6	Blackhawk 25	201	0	1	6	25
0	6	Blackhawk 25	202	1	4	4	25
0	6	Blackhawk 25	203	2	8	2	25
0	6	Blackhawk 25	204	3	7	5	25
0	6	Blackhawk 25	205	4	3	8	25
0	6	Blackhawk 25	206	5	2	7	25
0	6	Blackhawk 25	207	6	5	1	25
0	6	Blackhawk 25	208	7	6	3	25
0	6	Blackhawk 26	209	0	5	4	28
0	6	Blackhawk 26	210	1	8	6	28
0	6	Blackhawk 26	211	2	7	2	28
0	6	Blackhawk 26	212	3	4	1	28
0	6	Blackhawk 26	213	4	1	8	28
0	6	Blackhawk 26	214	5	2	5	28
0	6	Blackhawk 26	215	6	6	7	28
0	6	Blackhawk 26	216	7	3	3	28
0	6	Blackhawk 27	217	0	3	2	27
0	6	Blackhawk 27	218	1	2	6	27
0	6	Blackhawk 27	219	2	6	5	27
0	6	Blackhawk 27	220	3	4	1	27
0	6	Blackhawk 27	221	4	7	8	27
0	6	Blackhawk 27	222	5	8	3	27
0	6	Blackhawk 27	223	6	1	7	27
0	6	Blackhawk 27	224	7	5	4	27
0	7	Blackhawk 28	225	0	2	1	30
0	7	Blackhawk 28	226	1	3	4	30
0	7	Blackhawk 28	227	2	4	7	30
0	7	Blackhawk 28	228	3	7	3	30
0	7	Blackhawk 28	229	4	6	2	30
0	7	Blackhawk 28	230	5	8	8	30
0	7	Blackhawk 28	231	6	5	5	30
0	7	Blackhawk 28	232	7	1	6	30

Port mapping Date: 2018/03/20 Ver: V01 Author: Chaohua Chung				TH3 has ITM X2, Pipe x 8 Balckhawk x 32, Merlin x 1			
ITM number	Pipe Number	SerDes Core number	Physical Port Number	BC-X Lane-X	QSFP-DD TX (From Mac)	QSFP-DD RX (To Mac)	Front Port
0	7	Blackhawk 29	233	0	7	6	29
0	7	Blackhawk 29	234	1	1	4	29
0	7	Blackhawk 29	235	2	8	5	29
0	7	Blackhawk 29	236	3	3	2	29
0	7	Blackhawk 29	237	4	6	8	29
0	7	Blackhawk 29	238	5	4	7	29
0	7	Blackhawk 29	239	6	5	1	29
0	7	Blackhawk 29	240	7	2	3	29
0	7	Blackhawk 30	241	0	1	2	32
0	7	Blackhawk 30	242	1	3	4	32
0	7	Blackhawk 30	243	2	7	5	32
0	7	Blackhawk 30	244	3	8	1	32
0	7	Blackhawk 30	245	4	5	3	32
0	7	Blackhawk 30	246	5	2	7	32
0	7	Blackhawk 30	247	6	6	8	32
0	7	Blackhawk 30	248	7	4	6	32
0	7	Blackhawk 31	249	0	7	4	31
0	7	Blackhawk 31	250	1	8	8	31
0	7	Blackhawk 31	251	2	3	3	31
0	7	Blackhawk 31	252	3	1	7	31
0	7	Blackhawk 31	253	4	6	2	31
0	7	Blackhawk 31	254	5	5	6	31
0	7	Blackhawk 31	255	6	4	5	31
0	7	Blackhawk 31	256	7	2	1	31
0	1	Merlin 0 Lane 0 (Management)	257				
1	5	Merlin 0 Lane 2 (Management)	258				

Figure 5-2 Port Mapping

5.1.1. 400G QSFP56-DD connection

AS9700-32X is PHY-less system, BCM56980 connects with QSFP56-DD directly and CPU control transceiver's I2C and status via accessing CPLD. The QSFP56-DD ports support optical transceiver and DAC and power class up to 14W.

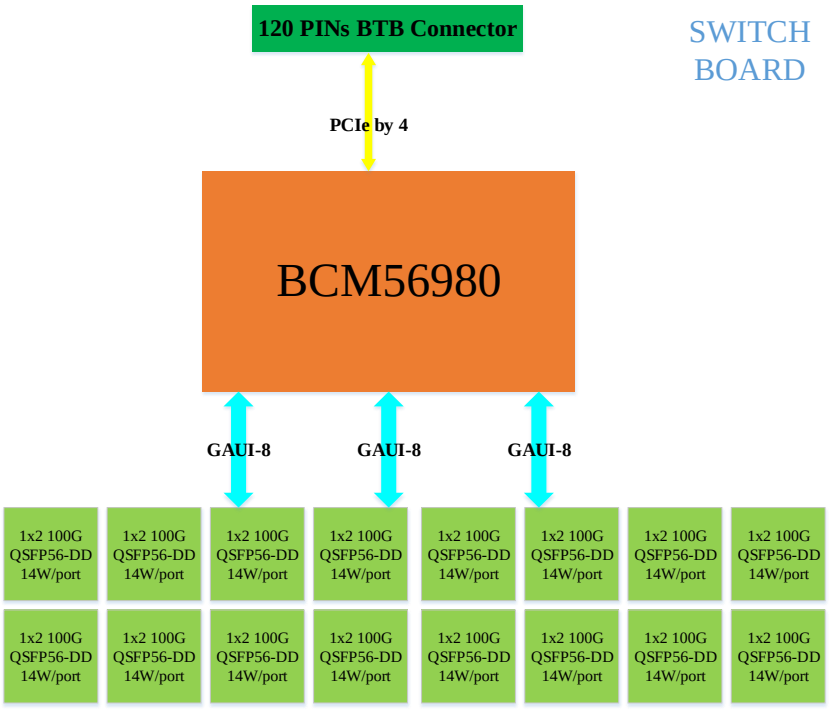


Figure 5-3 400G QSFP56-DD Connection

Table 3- Power Classification

Power Class	Max Power (W)
1	1.0
2	3.5
3	7.0
4	8.0
5	10
6	12
7	14
8	>14

Figure 5-4 QSFP56-DD Power Classification

5.1.2. 10G MUX connection

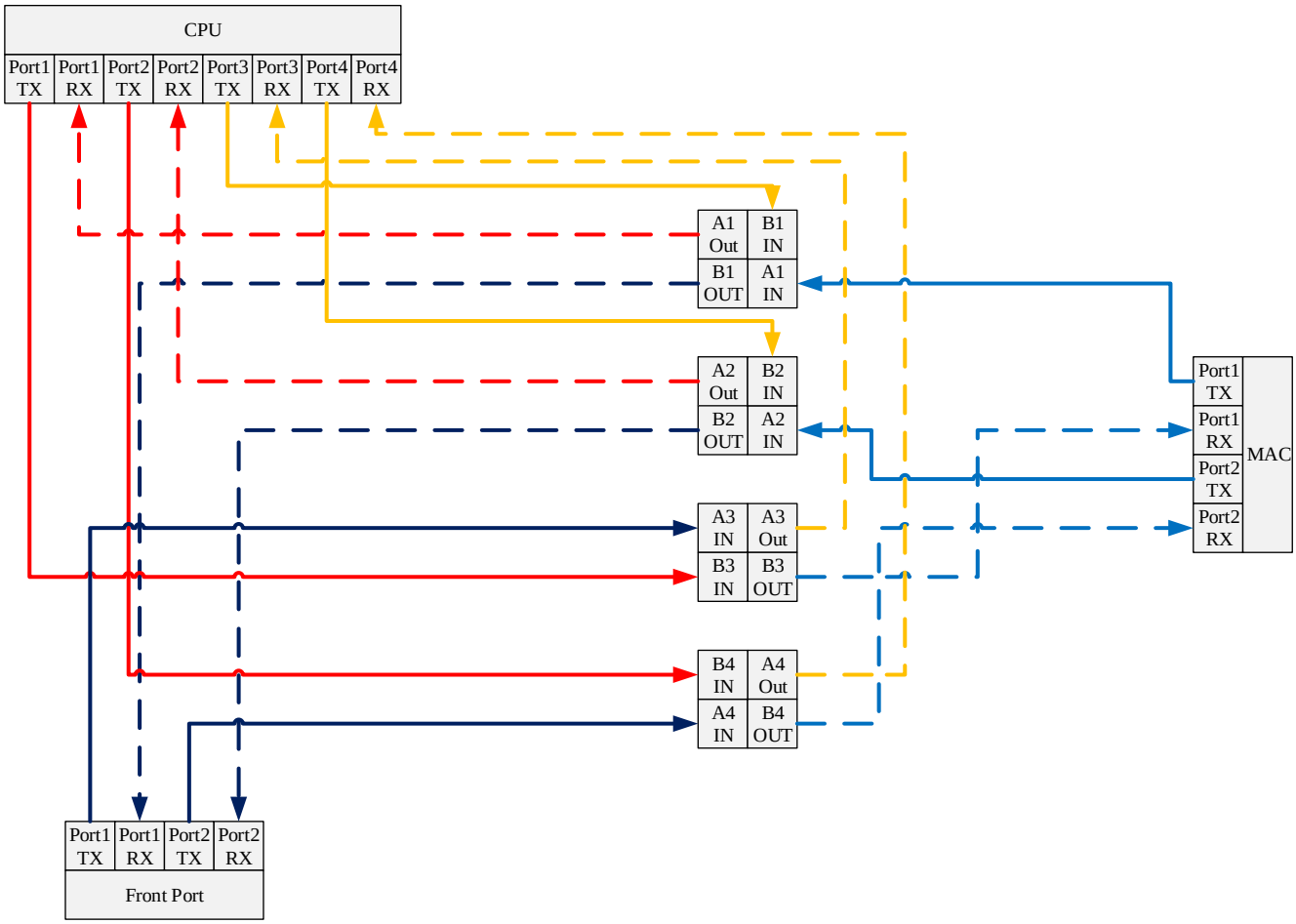


Figure 5-5 10G MUX connection

Table 5-2 Ture table for Broadwell-DE

CPU has 10G port x 2 (Broadwell-DE)			
MAC to CPU	Port1	A1 IN	A1 OUT
MAC to CPU	Port2	A2 IN	A2 OUT
CPU to MAC	Port1	B3 IN	B3 OUT
CPU to MAC	Port2	B4 IN	B4 OUT
MAC to Front Port	Port1	A1 IN	B1 OUT
MAC to Front Port	Port2	A2 IN	B2OUT
Front port to MAC	Port1	A3 IN	B3 OUT
Front port to MAC	Port2	A4 IN	B4 OUT

Table 5-3 Ture table for Denverton

CPU has10G port x 4 (Denverton)			
MAC to CPU	Port1	A1 IN	A1 OUT

CPU has10G port x 4 (Denverton)			
MAC to CPU	Port2	A2 IN	A2 OUT
CPU to MAC	Port1	B3 IN	B3 OUT
CPU to MAC	Port2	B4 IN	B4 OUT
CPU to Front port	Port3	B1 IN	B1 OUT
CPU to Front port	Port4	B2 IN	B2 OUT
Front port to CPU	Port3	A3 IN	A3 OUT
Front port to CPU	Port 4	A4 IN	B4 OUT

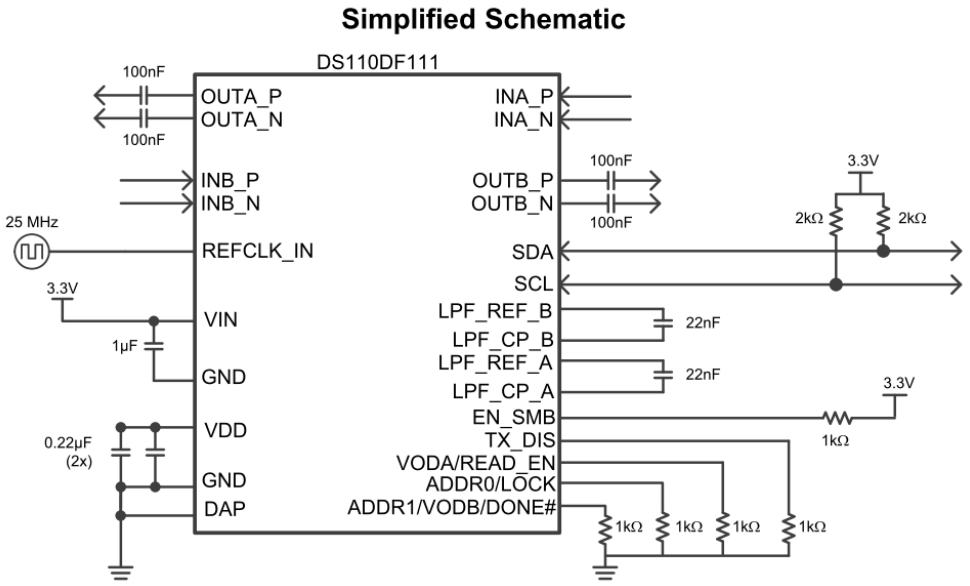


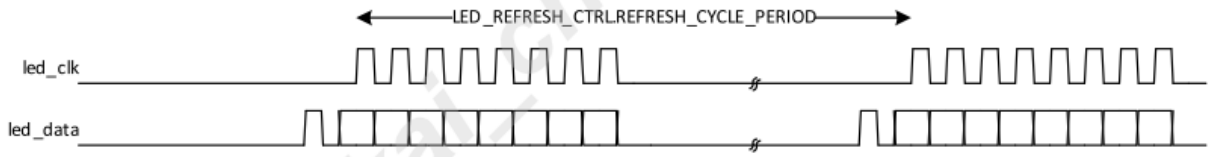
Figure 5-6 TI DS110DF111 block diagram

5.2. LED interface

BCM56980 Programming Guide CH3.2 describe detail LED interface. (56980-PG103)
The BCM56980's three separate LED interfaces: LED-0, LED-1, LED-2, LED-3, and LED-4.
LED-1 and LED-2 are connected to CPLD2. LED of Port 1~16 are driving by CPLD2.
LED-3 and LED-4 are connected to CPLD2. LED of Port 17~32 are driving by CPLD3.
Port status information includes link status, transmit and receive activity, and speed settings

Figure 8: Timing relationship of led_clk and led_data

Figure 9: led_clk/led_data Refresh Interval



The interface to the LED status indicators is implemented through a serial protocol carried out on two pins: LED_CLK and LED_DATA. If there are n LED status lights, it takes nclock cycles to shift the data out of the LED interface. The shifted-out LED data is out-of-phase with respect to the LED_CLK. After all n bits have been shifted out, the LED_CLK and LED_DATA lines go idle until the next time the LED status is refreshed. An external shift register is responsible for holding the state of the LED status between scan (refresh) events.

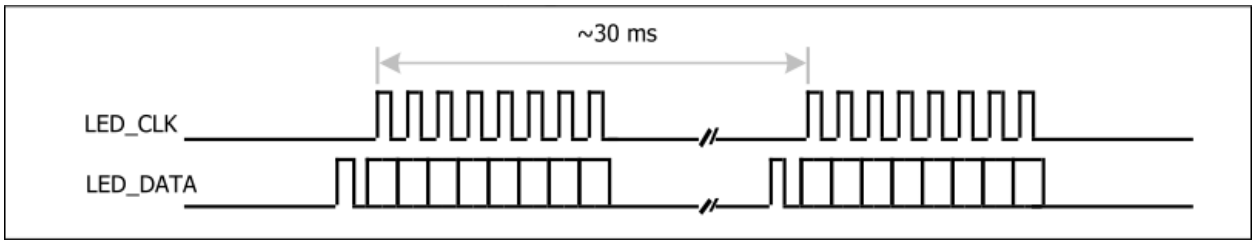
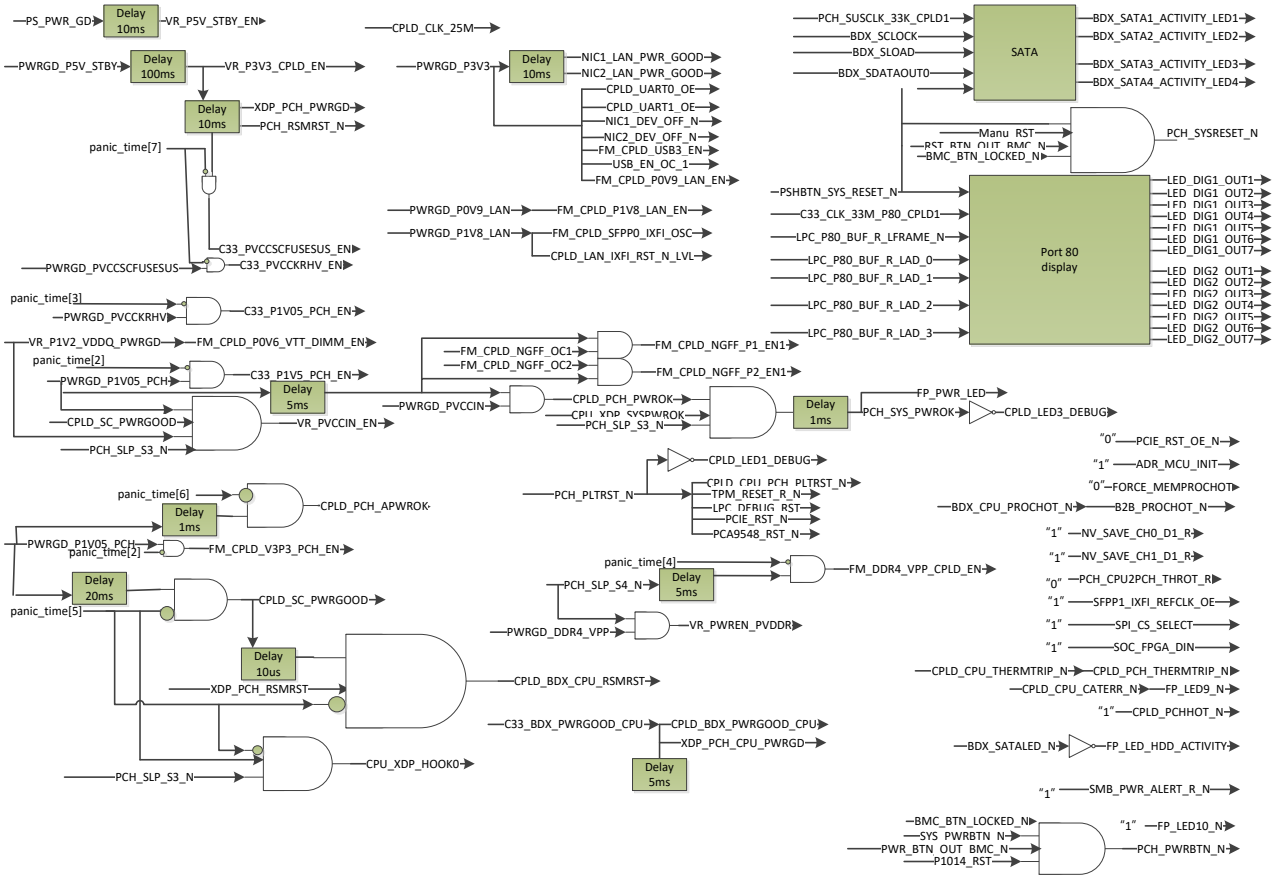


Figure 5-7 LED bus

6. CPLD
6.1. CPU CPLD

Figure 6-1 CPU CPLD block diagram



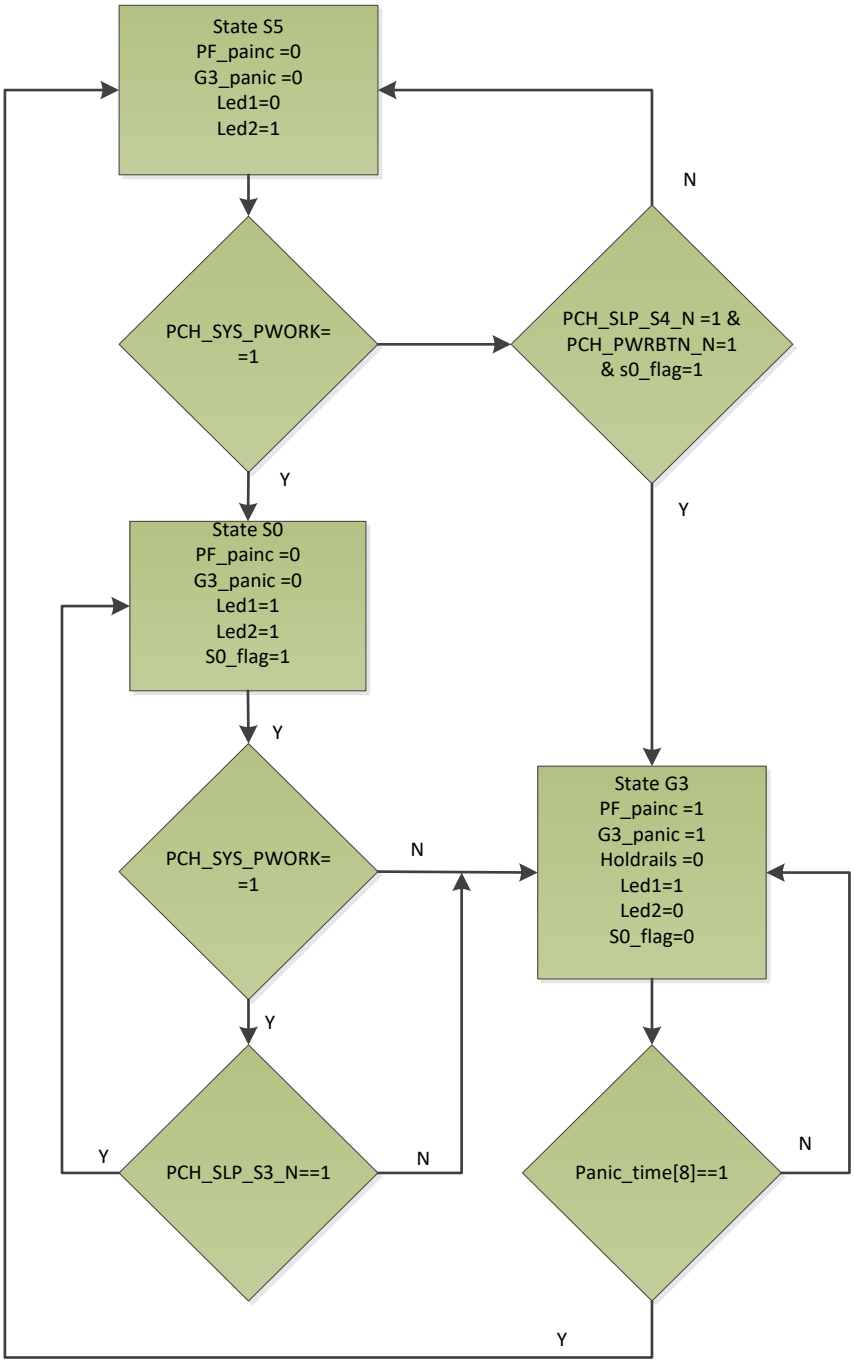
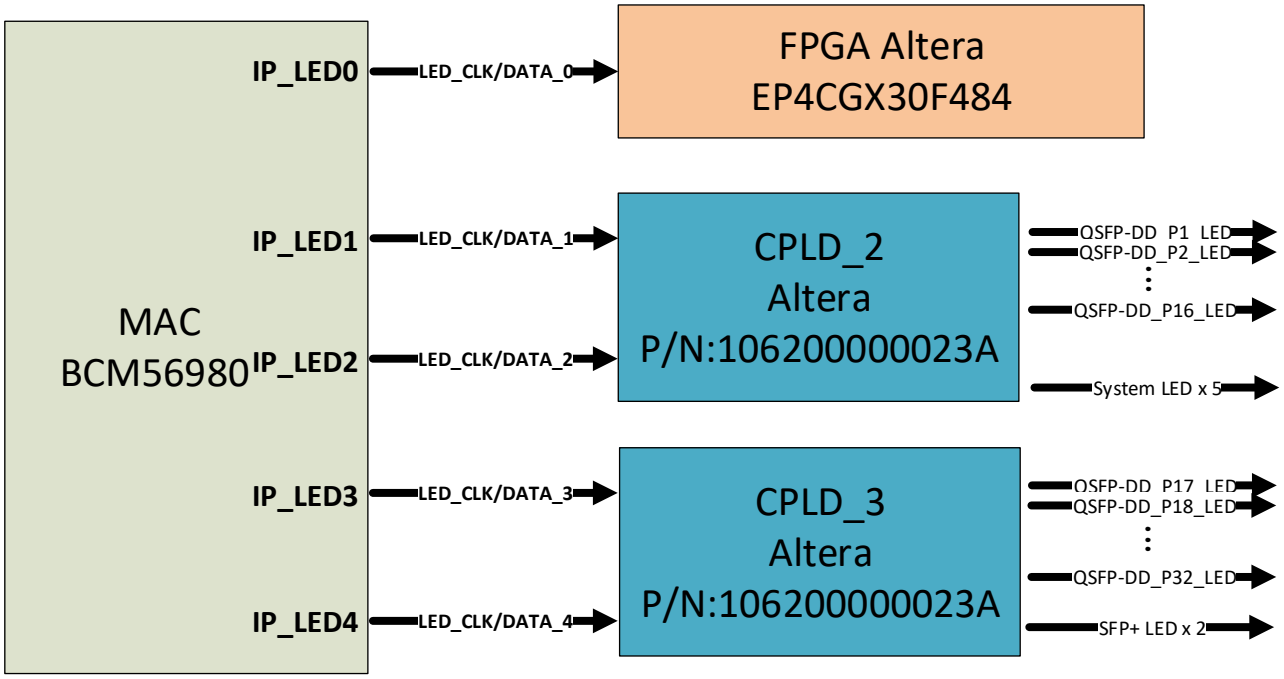


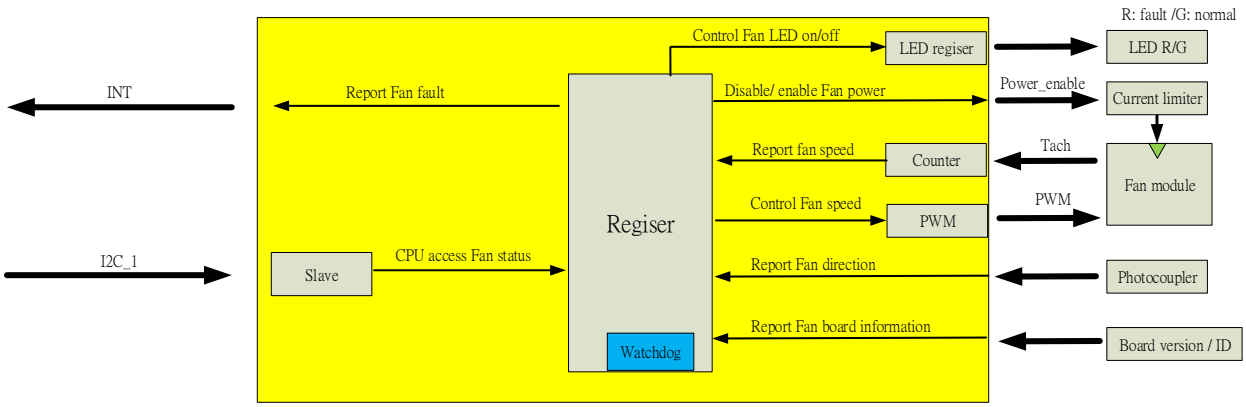
Figure 6-2 power sequence flow chat

6.2. MB CPLD

Switch board use one FPGA and two CPLDs.
FPGA handle system reset, interrupt, power sequence, PSU status..etc.
CPLD handle QSFP-DD control signals and LED driving.
Fan board has one CPLD for Fan direction, Speed control, Speed reporting…etc.



6.3. Fan CPLD



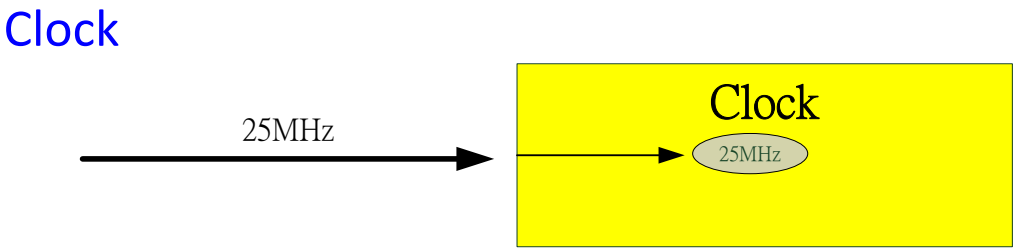
The CPU can access FAN CPLD via I2C interface to get the fan status.

The Fan CPLD has the register to control Fan PWM signal for fan speed control, and the counter for fan speed reporting. There has a fan power control to enable/ disable Fan power rail.

The CPLD will detect fan speed to check fan status if any issue. And CPLD will inform CPU by fan interrupt signal if there has fan fail occur or watchdog time out.

The fan LED will report the fan status via Red/ Green LED.

The watchdog timer is the thermal protection to avoid the CPU hang up. If watchdog timer count to zero, Fan CPLD will be pull-up the Fan speeds for system thermal protection.



The CPLD reference clock is from 25MHz.

6.4. CPLD Field upgrade information

The system support CPLD field upgrade function for main CPLD and Fan CPLD.

6.4.1.1. JTAG connection

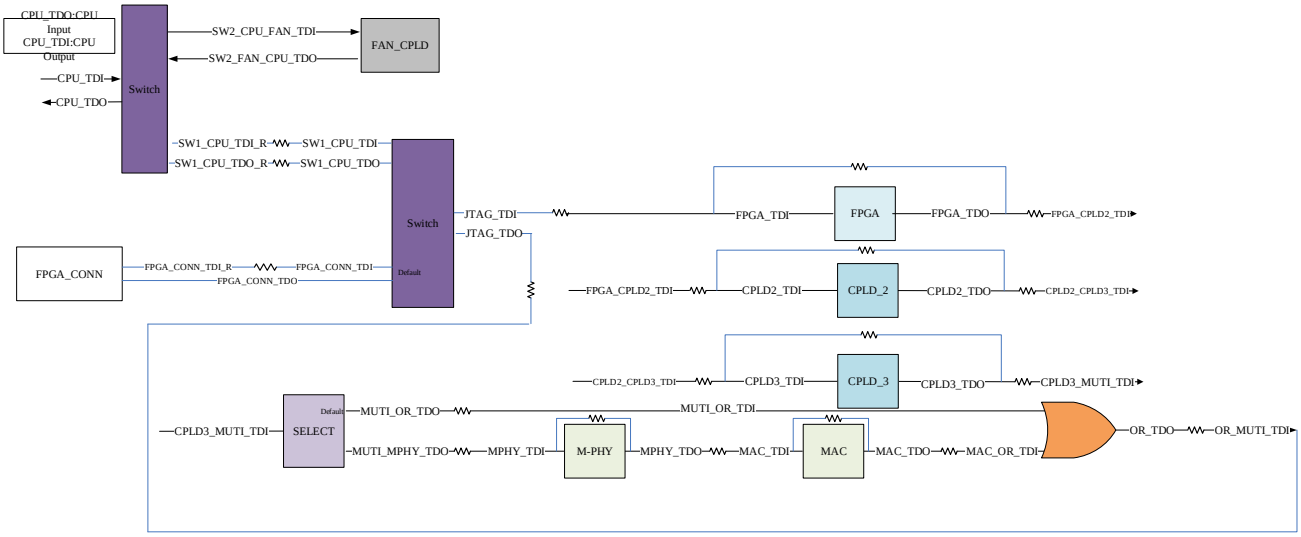


Figure 6-3 JTAG chain

7. Power Consumption

The total estimated power budget described in Table 6-1 is around 1249W on the 32 x 400G switchboard with CPU system.

All calculating data are based on the maximum power dissipation in the spec of components.

Total switch power consumption:

Power Consumption Estimation Table																
Voltage(V) / Current(mA)				ROV										(W)/device	Quantity	Total(W)
	1.8	1.2	0.6	0.88	0.8	1.05	1.3	1.7	1.5	3.3	5	2.5	12			
BDXDE	21000	3000				13813	500	350	162	487				58.99875	1	58.99875
NOR Flash										80				0.264	4	1.056
M.2 SSD										1060				3.498	1	3.498
B50210S										108.48				0.357984	1	0.357984
DDR4		4500	151									1065		8.1531	2	16.3062
CPLD										500				1.65	2	3.3
MISC.										100				0.33	1	0.33
BCM56980	500	4600		397700	47200					300				395.146	1	395.146
QSFP56-DD										4242				13.9986	32	447.9552
USB											1000			5	1	5
LED										6				0.0198	40	0.792
FAN CPLD										350				1.155	1	1.155
OCXO										1060				3.498	1	3.498
82P33731	89.5									984				3.4083	1	3.4083
SFP										450				1.485	1	1.485
Sub Current(mA)	21590	16600	302	397700	47200	13813	500	350	162	142203	1000	2130				942.28643
Efficiency=90%																1046.9849
FAN													2800	33.6	6	201.6
Total Watts														0	0	1248.5849

Table 7-1 Power Consumption Table

8. PSU

Vendor : ACBel

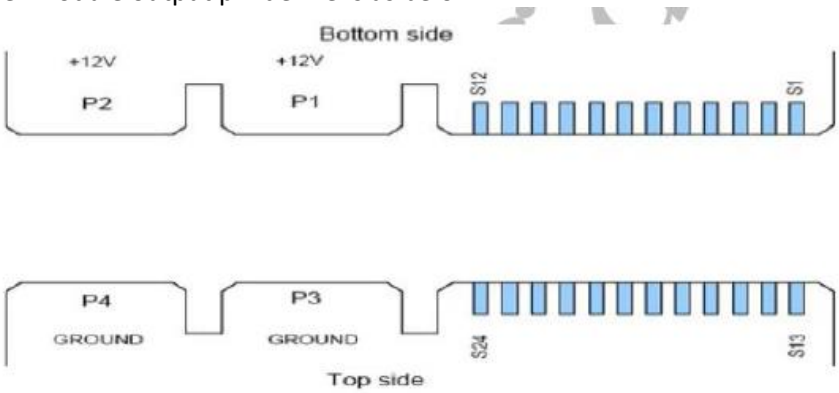
Output : 1300W maximum

Dimension : L321 x W50.5 x H39.9 (mm)

Comply with IPC9592

8.1. Pinout

The power module output pin define is as below.



Pin Number	Name	I/O	Active	Pin Length
P1 & P2 (Bottom)	+12V	I/O	Analog	Standard
P3 & P4 (Top)	RTN	I/O	Analog	Standard
S1	+12V SENSE	I	Analog	Standard
S2	+12V RTN SENSE	O	Analog	Standard
S3	12V I-Share	I/O	Analog	Standard
S4	SMB_ALERT#	O	Digital	Standard
S5	SDA	I/O	Digital	Standard
S6	SCL	I/O	Digital	Standard
S7	PS_KILL#	I	Low	Standard
S8	PSON#	I	Low	Short
S9	PWOK	O	High	Standard
S10	A1	I	Digital	Standard
S11	+5VSB	I/O	Analog	Standard
S12	+5VSB	I/O	Analog	Standard
S13	PDB_FAULT	I	Digital	Standard
S14	Present#	O	Low	Standard
S15	A0	I	Digital	Standard
S16	PDB_ALERT	I	Analog	Standard
S17	AC_OK	O	Analog	Standard
S18	N/A	I	Low	Standard
S19	N/A	I	High	Standard
S20	N/A	-	-	Standard
S21	N/A	-	-	Standard
S22	A2	I	Digital	Standard
S23	+5VSB	I/O	Analog	Standard
S24	+5VSB	I/O	Analog	Standard

8.2. Dimension

Nominal Dimensions

Height : 39.9mm (fits in 1U rack in vertical installation);

Width : 50.5mm

Depth : 321mm

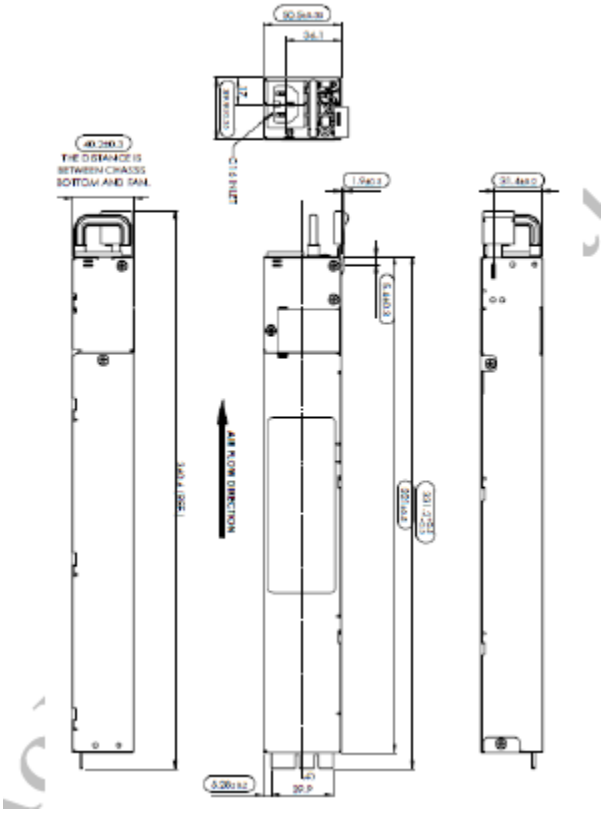
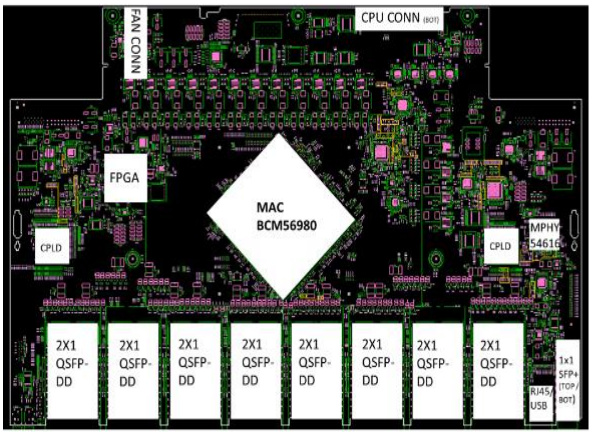


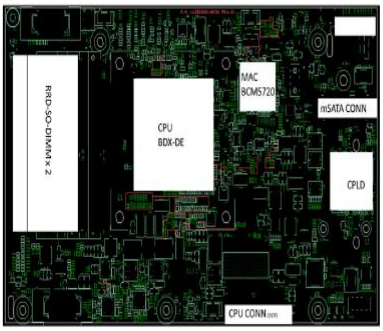
Figure 8-1 PSU Dimension

PCB

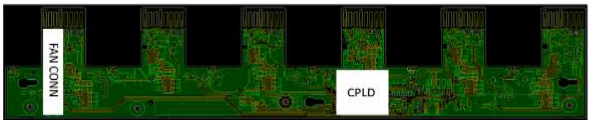
The AS9700-32X design includes 4 unique PCB assemblies. Information of stack-up, dimension and placement are included below.



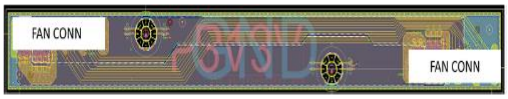
CPU Module PCB



Fan PCB



Bridge PCB



Stack-up
CPU

Date: 2015/1/6 14:21
P/N: DFM-98
Layers: LAYER 12
Tg: 180
TU-872LK

Layer Name	Plane Description	Remain Copper 1 % ↑	Material	reduce after pressd	finish Thickness	Er	Single-end Impedance	Single-end Width	Single-end Impedance	Single-end Width	Differential Impedance	Differential Width/Space	Differential Impedance	Differential Width/Space	Differential Impedance	Differential Width/Space	Differential Impedance	Differential Width/Space	Differential Impedance	Differential Width/Space	Differential Impedance	Differential Width/Space	Differential Impedance	Differential Width/Space	Ref. Pin
	solder mask				0.50																				
Layer 1	Signal		1/3oz HTE +Plating		1.40		40	7	50	4.5	68	8/6	80	6/7	63	9/5	83	5/5	85	5/5.5	90	5/8	100	4/7	L2
	PREPREG		1067		2.41	3.2																			
Layer 2	POWER/GND	85	1/2oz HTE	0.09	0.60																				
	Core		0.0762		3.00	3.25																			
Layer 3	Signal	65	1/2oz HTE	0.21	0.60		40	6	50	4	68	8/8	80	5/4.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	L2&L4
	PREPREG		1078_1078HR		6.20	3.25																			
Layer 4	POWER/GND	85	1/2oz HTE	0.09	0.60																				
	Core		0.0762		3.00	3.25																			
Layer 5	Signal	65	1/2oz HTE	0.21	0.60		40	6	50	4	68	8/8	80	5/4.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	L4&L6
	PREPREG		1078_1078HR		5.90	3.25																			
Layer 6	POWER/GND	85	2oz HTE	0.39	2.60																				
	Core		0.1334		21.00	3.8																			
Layer 7	POWER/GND	85	2oz HTE	0.39	2.60																				
	PREPREG		1078_1078HR		5.90	3.25																			
Layer 8	Signal	65	1/2oz HTE	0.21	0.60		40	6	50	4	68	8/8	80	5/4.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	L7&L9
	Core		0.0762		3.00	3.25																			
Layer 9	POWER/GND	85	1/2oz HTE	0.09	0.60																				
	PREPREG		1078_1078HR		6.20	3.25																			
Layer 10	Signal	65	1/2oz HTE	0.21	0.60		40	6	50	4	68	8/8	80	5/4.5	63	8/4	83	5/6	85	4/4	90	4/5	100	4/15	L9&L11
	Core		0.0762		3.00	3.25																			
Layer 11	POWER/GND	85	1/2oz HTE	0.09	0.60																				
	PREPREG		1067		2.41	3.2																			
Layer 12	Signal		1/3oz HTE +Plating		1.40		40	7	50	4.5	68	8/6	80	6/7	63	9/5	83	5/5	85	5/5.5	90	5/8	100	4/7	L11
	solder mask				0.50																				
Total Thickness=	1.93			1.90	75.92																				

Main Switch board

Accton Tech 24 Layer Stack up Proposal

Layer #	A/W Code	Type	Customer Requirement: Cu Thickness (mil)	SE 50 ohms: Linewidth (mils)	DIFF 90ohms: Linewidth (mils)	DIFF 90ohms: Airgap (mils)	DIFF 92ohms: Linewidth (mils)	DIFF 92ohms: Airgap (mils)	DIFF 100ohms: Linewidth (mils)	DIFF 100ohms: Airgap (mils)	HCS Proposal (07/11/2017) -> (29/11/2017): Estimated Thickness (um)	Cu Weight (oz)	Cu Foil Type	Estimated Thickness (mils)	Estimated Layer Cu Ratio (%)	Construction	Dk @ 1 Ghz	Df @ 1 Ghz	For Reference: Dk @ 10 Ghz	For Reference: Df @ 10 Ghz	For Reference: Dk @ 15 Ghz	For Reference: Df @ 15 Ghz	SE 50 ohms: Line width (mils)	SE 50 ohms: Air-gap (mils)	DIFF 90ohms: Line width (mils)	DIFF 90ohms: Air-gap (mils)	DIFF 90ohms (LW 7.4mil): Line width (mils)	DIFF 90ohms (LW 7.4mil): Air-gap (mils)	DIFF 90ohms (LW 7.6mil): Line width (mils)	DIFF 90ohms (LW 7.6mil): Air-gap (mils)	DIFF 90ohms (LW 7.8mil): Line width (mils)	DIFF 90ohms (LW 7.8mil): Air-gap (mils)	DIFF 95ohms: Line width (mils)	DIFF 95ohms: Air-gap (mils)	DIFF 100ohms: Line width (mils)	DIFF 100ohms: Air-gap (mils)	DIFF (4.25/3.5/4.25): Line width (mils)	DIFF (4.25/3.5/4.25): Air-gap (mils)	Est. Impedance value (ohms)
		Soldermask	1								25			1.0																								
1	TOP	0.5oz Cu Foil+	1.7								50	12um+plating	MTE	2.0									11.3	8.7	4.8	--	--	--	--	--	--	8.1	5.4	7.4	5.6	--	--	--
		Prepreg									135			5.3	#1035-72% + #1078-64%		3.13	0.00130	3.11	0.0021	3.10	0.0023																	
2	GND	1.0 oz Cu	1.3			REFERENCE LAYER					32	1.0	HVLP	1.3	80%																								
	Core 1	CORE									152			6.0		2X 1078	3.18	0.0014	3.16	0.0021	3.15	0.0023																	
3	S	0.5 oz Cu	0.6								16	0.5	HVLP	0.6	20%								6.7	7.1	5.9	7.4	7.1	7.6	8.1	7.8	9.6	6.5	6.5	6.1	6.9	4.25	3.50	105
		Prepreg									137			5.4		2x 1078-64%	3.18	0.0014	3.16	0.0021	3.15	0.0023																	
4	GND	1.0 oz Cu	1.3			REFERENCE LAYER					32	1.0	HVLP	1.3	80%																								
	Core 2	CORE									152			6.0		2X 1078	3.18	0.0014	3.16	0.0021	3.15	0.0023																	
5	S	0.5 oz Cu	0.6								16	0.5	HVLP	0.6	20%								6.7	7.1	5.9	7.4	7.1	7.6	8.1	7.8	9.6	6.5	6.5	6.1	6.9	4.25	3.50	105
		Prepreg									137			5.4		2x 1078-64%	3.18	0.0014	3.16	0.0021	3.15	0.0023																	
6	GND	1.0 oz Cu	1.3			REFERENCE LAYER					32	1.0	HVLP	1.3	80%																								
	Core 3	CORE									152			6.0		2X 1078	3.18	0.0014	3.16	0.0021	3.15	0.0023																	
7	S	0.5 oz Cu	0.6								16	0.5	HVLP	0.6	20%								6.7	7.1	5.9	7.4	7.1	7.6	8.1	7.8	9.6	6.5	6.5	6.1	6.9	4.25	3.50	105
		Prepreg									137			5.4		2x 1078-64%	3.18	0.0014	3.16	0.0021	3.15	0.0023																	
8	GND	1.0 oz Cu	1.3			REFERENCE LAYER					32	1.0	HVLP	1.3	80%																								
	Core 4	CORE									152			6.0		2X 1078	3.18	0.0014	3.16	0.0021	3.15	0.0023																	
9	S	0.5 oz Cu	0.6								16	0.5	HVLP	0.6	20%								6.4	7.1	6.3	7.4	7.9	7.6	9.1	7.8	11.2	6.5	6.9	6.0	7.0	4.25	3.50	104
		Prepreg									130			5.1	#1035-72% + #1078-64%		3.13	0.0013	3.11	0.0021	3.10	0.0023																	
10	GND	1.0 oz Cu	1.3			REFERENCE LAYER					30	12um+plating	MTE	1.2	80%																								
		Prepreg									132			5.2	#1035-72%+#1078-69%		3.07	0.0012	3.05	0.0020	3.04	0.0022																	
11	V	2.0 oz Cu	2.6								66	2.0	RTP	2.6	80%								--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--
	Core 5	CORE									76			3.0		1x 1078	3.18	0.0014	3.16	0.0021	3.15	0.0023																	
12	V	2.0 oz Cu	2.6			REFERENCE LAYER					66	2.0	RTP	2.6	80%								--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--
		Prepreg									154			6.1		2x 1078-69%	3.07	0.0012	3.05	0.0020	3.04	0.0022																	
13	V	2.0 oz Cu	2.6			REFERENCE LAYER					66	2.0	RTP	2.6	80%								--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--
	Core 6	CORE									76			3.0		1x 1078	3.18	0.0014	3.16	0.0021	3.15	0.0023																	
14	V	2.0 oz Cu	2.6			REFERENCE LAYER					66	2.0	RTP	2.6	80%								--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--
		Prepreg									132			5.2	#1035-72%+#1078-69%		3.07	0.0012	3.05	0.0020	3.04	0.0022																	
15	GND	1.0 oz Cu	1.3			REFERENCE LAYER					30	12um+plating	MTE	1.2	80%																								
		Prepreg									130			5.1	#1035-72% + #1078-64%		3.13	0.00130	3.11	0.0021	3.10	0.0023																	
16	S	0.5 oz Cu	0.6								16	0.5	HVLP	0.6	20%								6.4	7.1	6.3	7.4	7.9	7.6	9.1	7.8	11.2	6.5	6.9	6.0	7.0	4.25	3.50	104
	Core 7	CORE									152			6.0		2X 1078	3.18	0.0014	3.16	0.0021	3.15	0.0023																	
17	GND	1.0 oz Cu	1.3			REFERENCE LAYER					32	1.0	HVLP	1.3	80%																								
		Prepreg									137			5.4		2x 1078-64%	3.18	0.0014	3.16	0.0021	3.15	0.0023																	
18	S	0.5 oz Cu	0.6								16	0.5	HVLP	0.6	20%								6.7	7.1	5.9	7.4	7.1	7.6	8.1	7.8	9.6	6.5	6.5	6.1	6.9	4.25	3.50	105
	Core 8	CORE									152			6.0		2X 1078	3.18	0.0014	3.16	0.0021	3.15	0.0023																	
19	GND	1.0 oz Cu	1.3			REFERENCE LAYER					32	1.0	HVLP	1.3	80%																								
		Prepreg									137			5.4		2x 1078-64%	3.18	0.0014	3.16	0.0021	3.15	0.0023																	
20	S	0.5 oz Cu	0.6								16	0.5	HVLP	0.6	20%								6.7	7.1	5.9	7.4	7.1	7.6	8.1	7.8	9.6	6.5	6.5	6.1	6.9	4.25	3.50	105
	Core 9	CORE									152			6.0		2X 1078	3.18	0.0014	3.16	0.0021	3.15	0.0023																	
21	GND	1.0 oz Cu	1.3			REFERENCE LAYER					32	1.0	HVLP	1.3	80%																								
		Prepreg									137			5.4		2x 1078-64%	3.18	0.0014	3.16	0.0021	3.15	0.0023																	
22	S	0.5 oz Cu	0.6								16	0.5	HVLP	0.6	20%								6.7	7.1	5.9	7.4	7.1	7.6	8.1	7.8	9.6	6.5	6.5	6.1	6.9	4.25	3.50	105
	Core 10	CORE									152			6.0		2X 1078	3.18	0.0014	3.16	0.0021	3.15	0.0023																	
23	GND	1.0 oz Cu	1.3			REFERENCE LAYER					32	1.0	HVLP	1.3	80%																								
		Prepreg									135			5.3	#1035-72% + #1078-64%		3.13	0.00130	3.11	0.0021	3.10	0.0023																	
24	BOT	Cu Foil+plating	1.7								50	12um+plating	MTE	2.0	20%								11.3	8.7	4.8	--	--	--	--	--	--	8.1	5.4	7.4	5.6	--	--	--
		Soldermask	1								25			1.0																								
Requested thickness			3.0								4.00	mm		157.3	mils (Soldermask to soldermask over copper)																								

Bridge board

Date: 2017/10/12 09:23

P/N:

Layers: LAYER 4

Tg: 150 NP155F、HTE-590、IT158、EM-825

Layer Name	Plane Description	Remain Copper (%)	reduce after pressed	Material Thickness	finish Thickness	tolerance	Er	Single-end		Differential		Ref. Pin
								Impedance	Width	Impedance	Width/Space	
	solder mask			0.50	0.50							
Layer 1	Signal			1.70	1.70			50	8	100	5.5/5	L2
	PREPREG			4.60	4.42	+/-1	3.85					
Layer 2	POW/GND	86	0.17	1.20	1.20							
	Core			48.66	48.66	+/-10%	4.4					
Layer 3	POW/GND	86	0.17	1.20	1.20							
	PREPREG			4.60	4.42	+/-1	3.85					
Layer 4	Signal			1.70	1.70			50	8	100	5.5/5	L3
	solder mask			0.50	0.50							
Total Thickness= 1.63			0.36	64.66	64.30							

Fan board

Date： 2014/1/13 20:54

P/N：

Layers： LAYER 4

Tg： 150 NP155F、HTE-590、IT158、EM-825

Layer Name	Plane Description	Remain Copper (%)	reduce after pressed	Material Thickness	finish Thickness	tolerance	成本	Er	Single-end 50ohm		differential 100ohm		Ref.
									Impedance	Width	Impedance	Width/Space	
	solder mask			0.5									
Layer1	Signal			1.4					50	8	100	5.5/5	L2
	PREPREG			4.6	4.425	+/-1	1.16	3.85					
Layer2	POW/GND	86%	0.175	1.25									
	CORE			76.34	76.34	+/-10%	25.48	4					
Layer3	POW/GND	86%	0.175	1.25									
	PREPREG			4.6	4.425	+/-1	1.16	3.85					
LAYER 4	Signal			1.4					50	8	100	5.5/5	L3
	solder mask			0.5									
Total Thickness= 2.32 mm			0.35	91.84	91.49		27.8						

8.3. PCB Dimension

8.3.1. CPU PCB Dimension

The CPU PCB dimension is 210 x 123.5 mm. T= 1.93mm

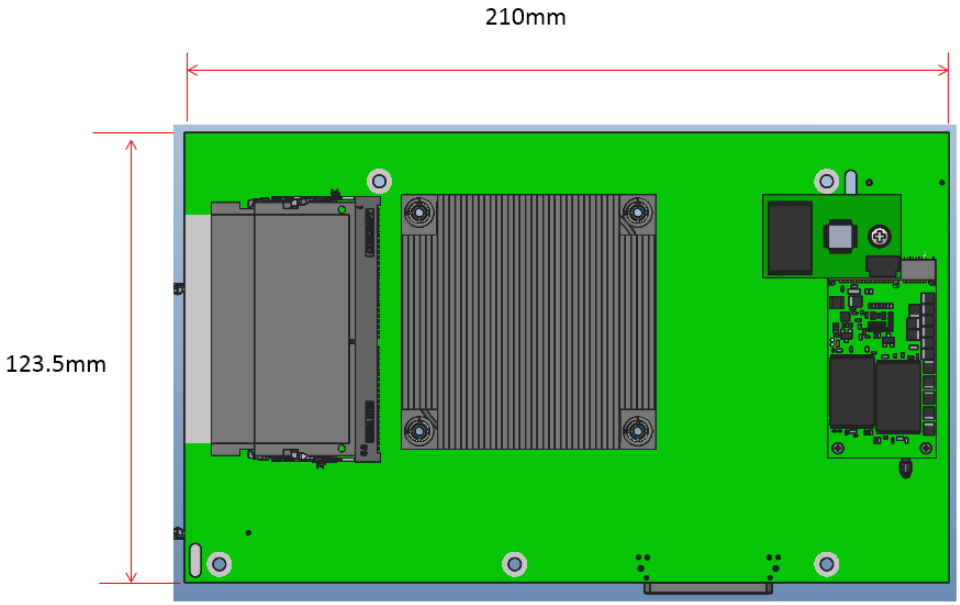


Figure 8-2 CPU board PCB Dimension

Figure 8-3 Switch board PCB Dimension

8.3.2. Switch Board PCB Dimension

The Switch PCB dimension is 413.5 x 269 mm. T=4.0mm

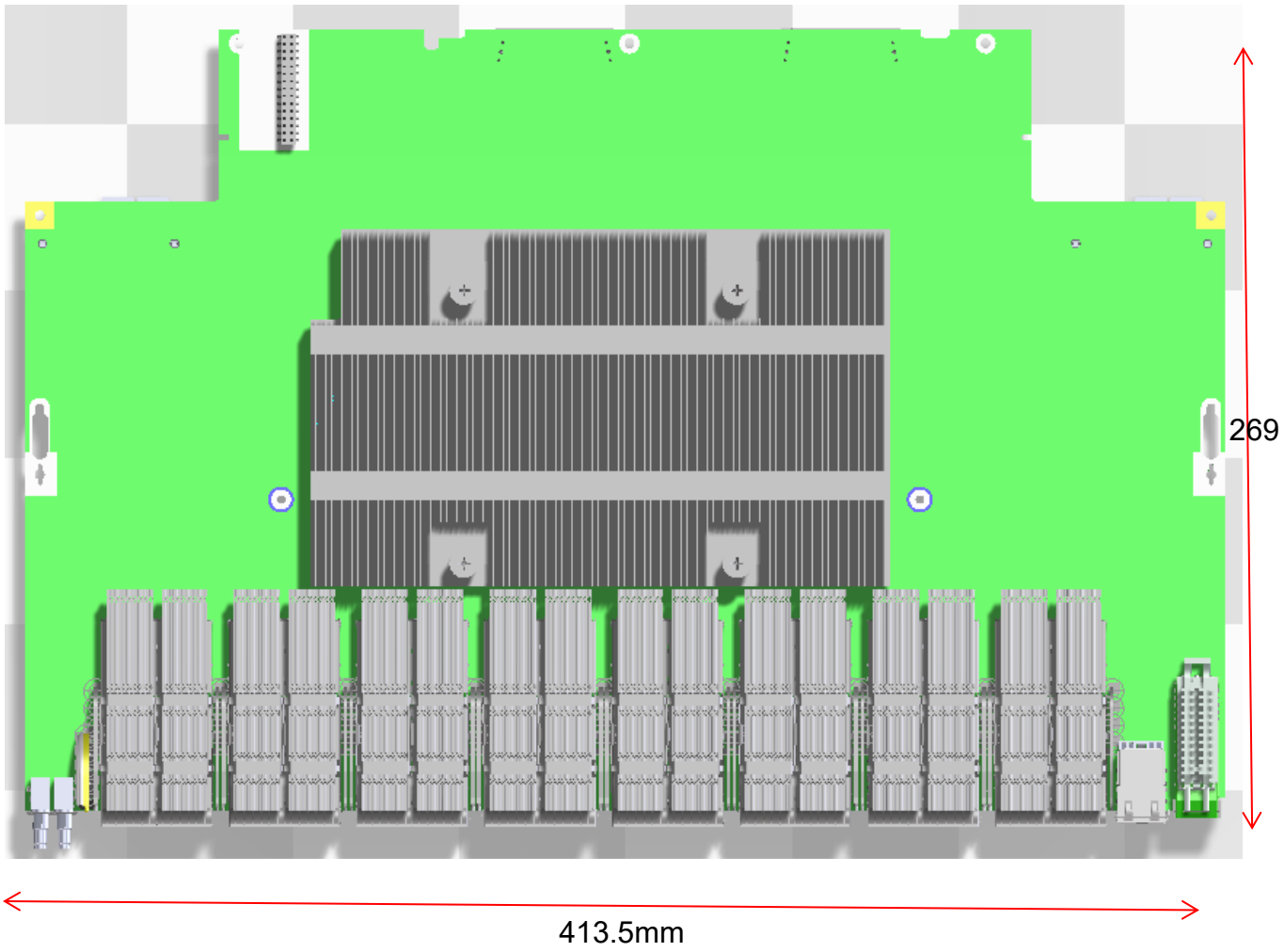


Figure 8-4 Switch board PCB Dimension

8.3.3. Bridge board PCB Dimension

The Bridge board PCB dimension is 208.62 x 24 mm. T=1.63mm

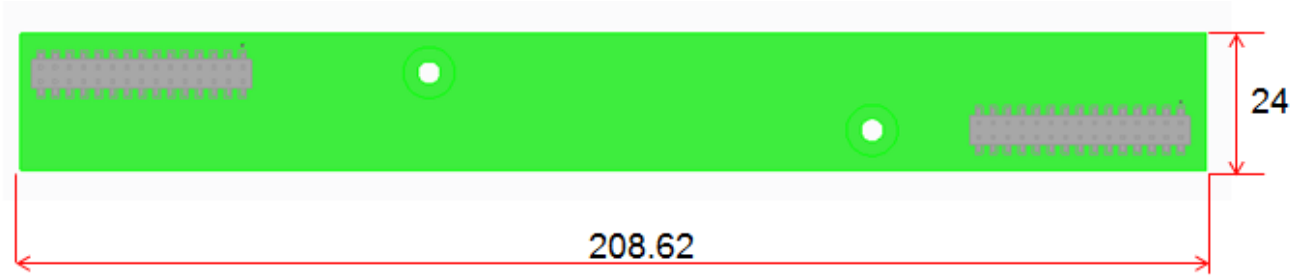


Figure 8-5 Bridge board PCB Dimension

8.3.4. Fan board PCB Dimension

Fan board PCB dimension is 281 x 57.9 mm. T=2.36mm

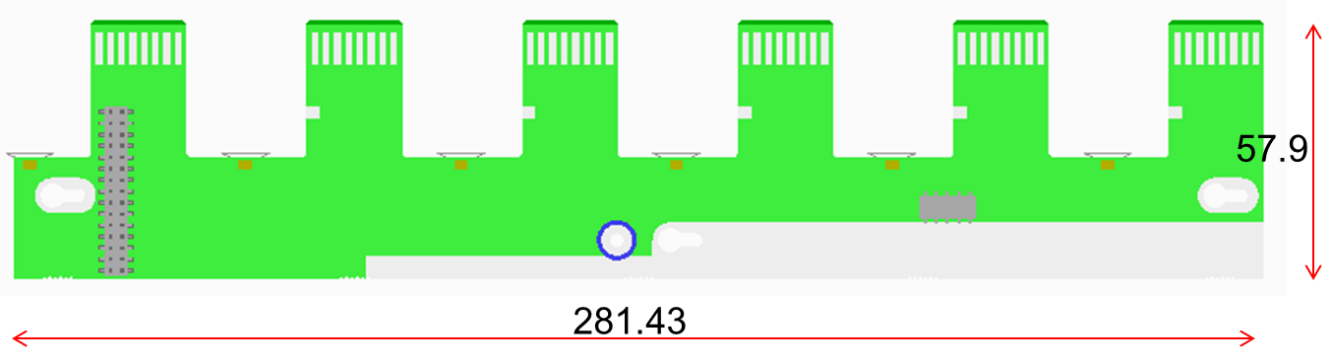


Figure 8-6 Fan board PCB Dimension

9. Mechanical

9.1. Dimension

Height: 43.1mm (maximum)

Width: 438.4mm

Depth: 536mm

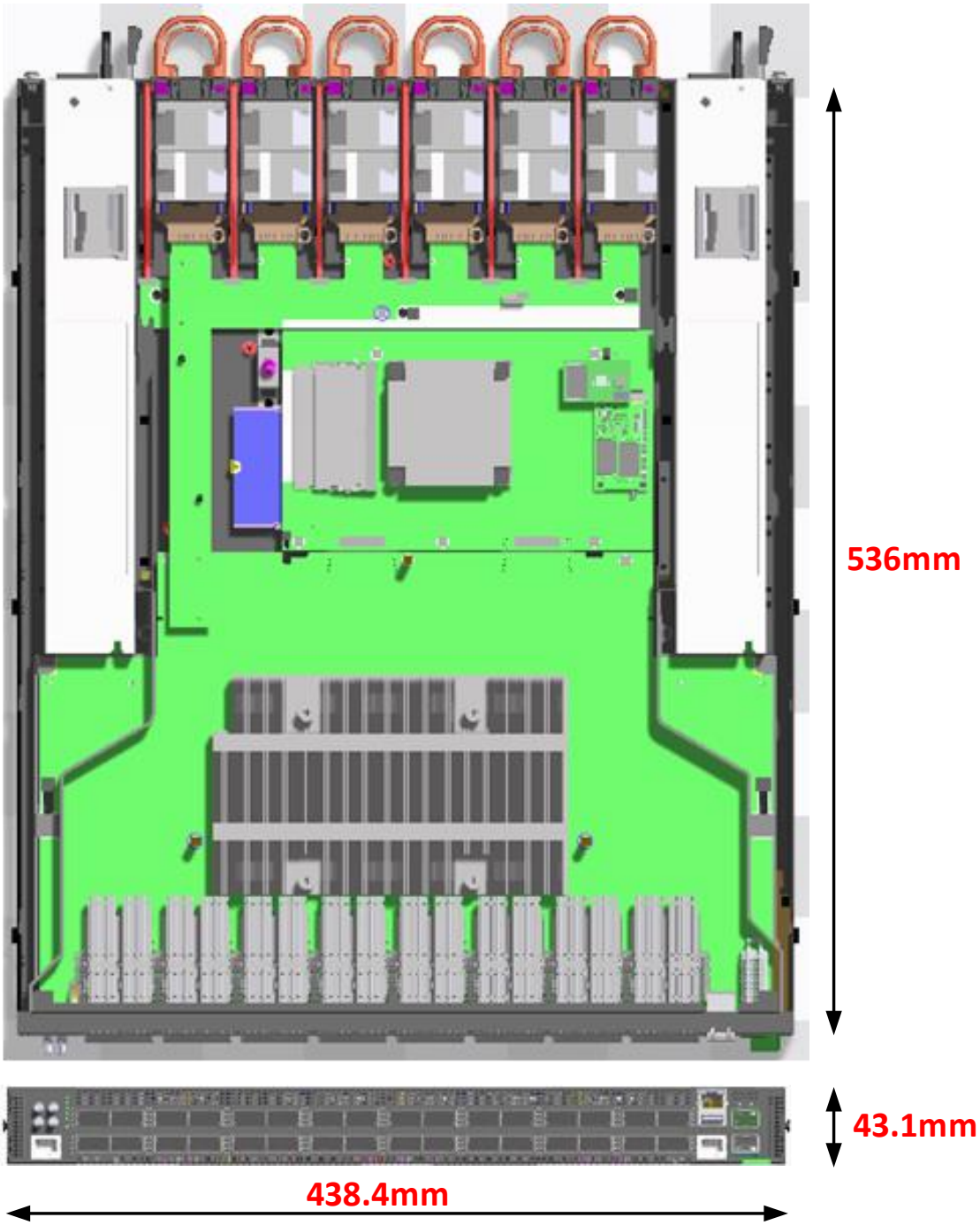


Figure 9-1 Mechanical Dimension

9.2. Mechanical Placement

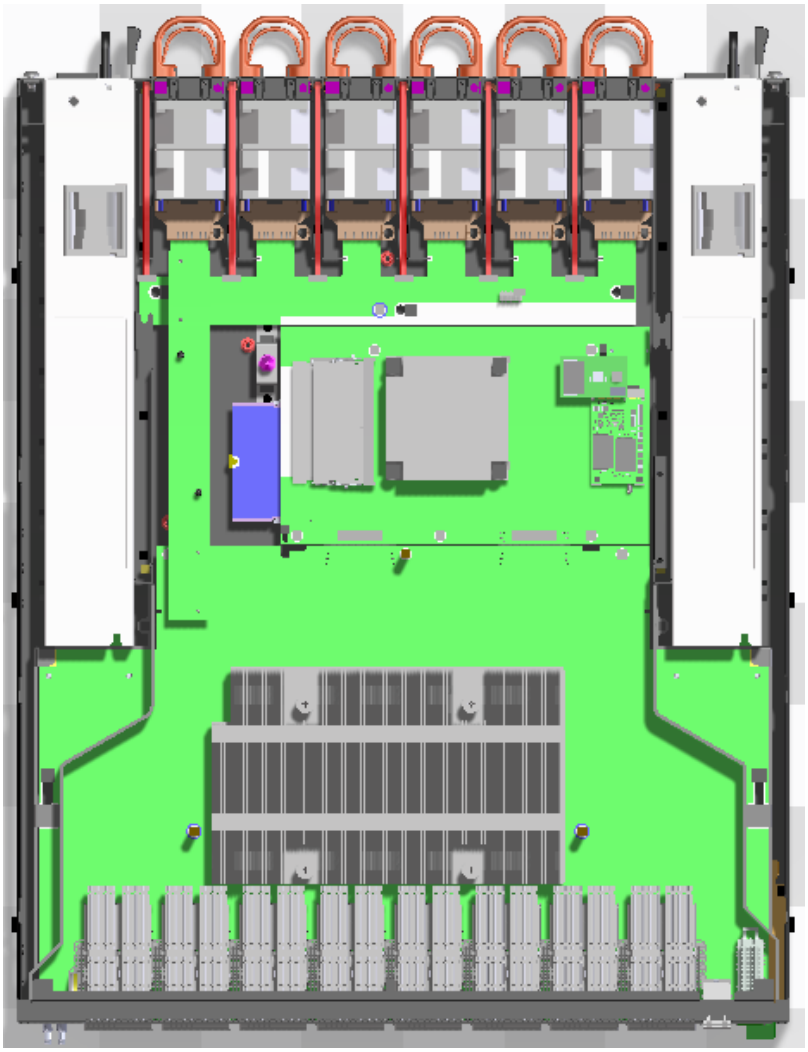


Figure 9-2 Mechanical Placement (Top)

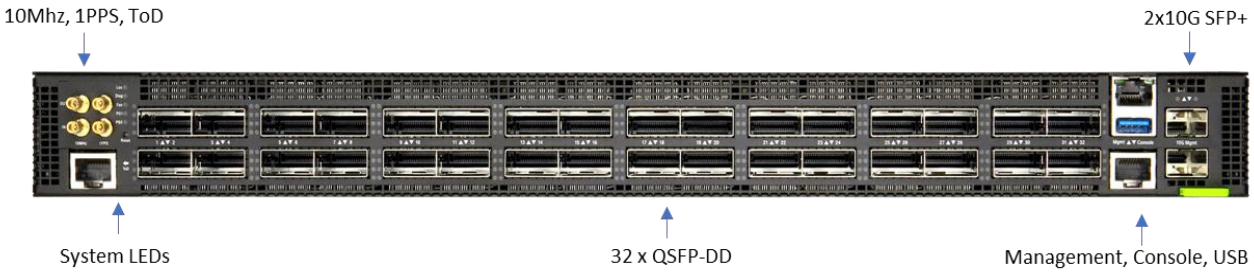


Figure 9-3 Mechanical Placement (Front)

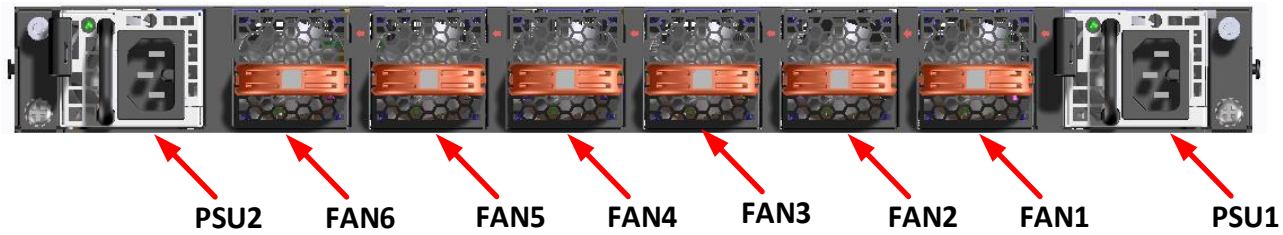


Figure 9-4 Mechanical Placement (Rear)

9.3. Cooling Method

9.3.1. Fan module

AS9700-32X system supports two kinds Fan module.

Front to back Fan module with **red** color
Back to Front Fan module with **blue** color
FAN vendor : AVC
Dimension : 40 x 40 x 56 mm

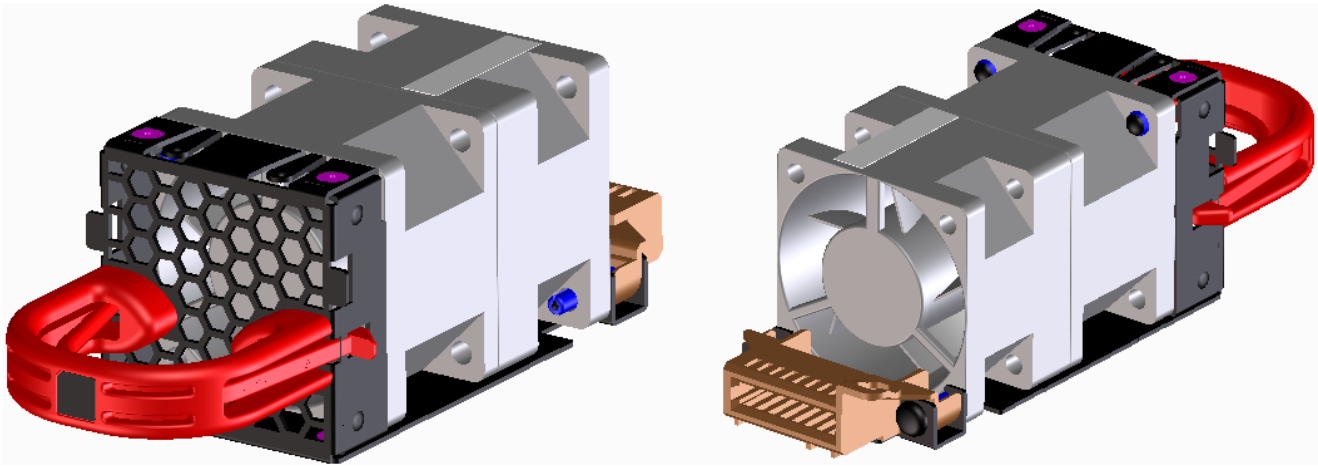


Figure 9-5 Fan module-F2B

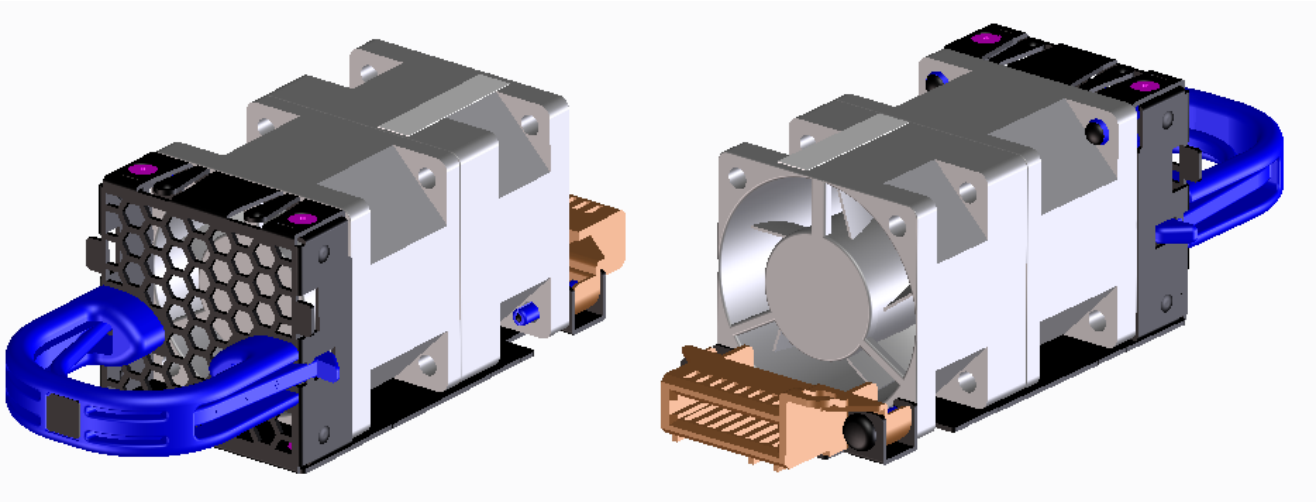


Figure 9-6 Fan module-B2F

ITEM		SPEC.	
RATED VOLTAGE		12	VDC
OPERATION VOLTAGE		7.0 ~ 13.2	VDC
START UP VOLTAGE		7.0	VDC
RATED CURRENT		2.26 (2.76 MAX.)	A (AVERAGE)
CURRENT ON LABEL		2.76	A
START PEAK CURRENT		5.0 (6.5 MAX.)	A
RATED POWER		27.12 (33.12 MAX.)	W
SPEED	4030	22500±10%	R.P.M
	4026	19500±10%	R.P.M
SPEED CONTROL TYPE		PWM CONTROLLER	
SIGNAL OUTPUT		FREQUENCY GENERATOR (FG)	
MAX. AIR FLOW (AT ZERO STATIC PRESSURE)		1.073 (0.965 MIN.) 37.89 (34.10 MIN.)	M^3/MIN CFM
MAX. AIR PRESSURE (AT ZERO FLOW)		108.75(88.08 MIN.) 4.281 (3.468 MIN.)	mm-H2O inch-H2O
ACOUSTICAL NOISE		70.0 (74.0 MAX.)	dB-A

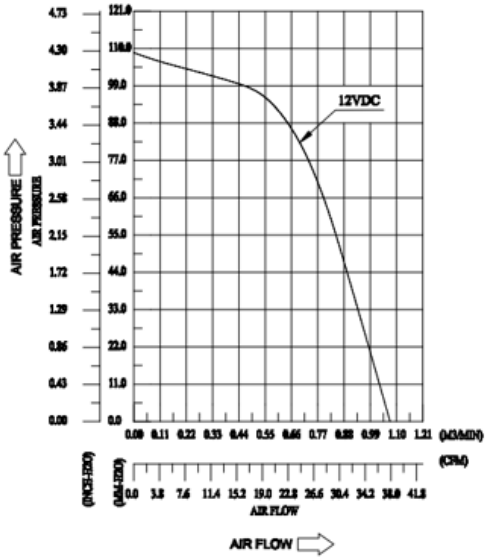


Figure 9-7 Fan information

9.3.2. Heatsink

The materials and size of MAC heat sink shown below.

Dimension : 200x120x15.5 mm

Fastener : Screw x 4

Base : Vapor chamber

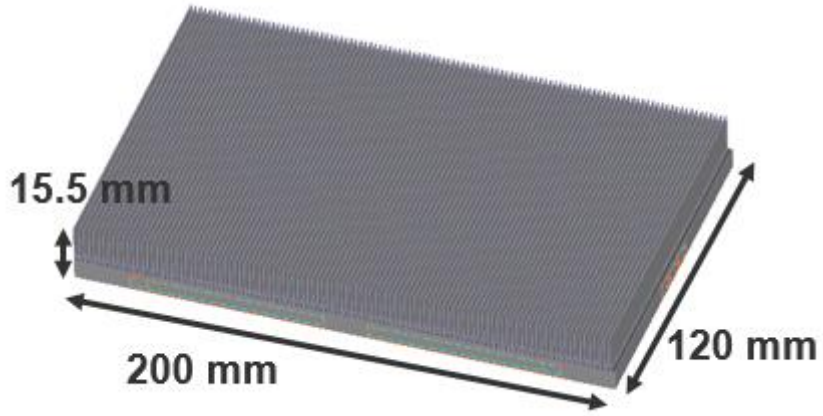


Figure 9-8 MAC heatsink dimension

The size of CPU heat sink shown below.

Dimension : 70 x 70 x 17 mm

Fastener : Screw x 4

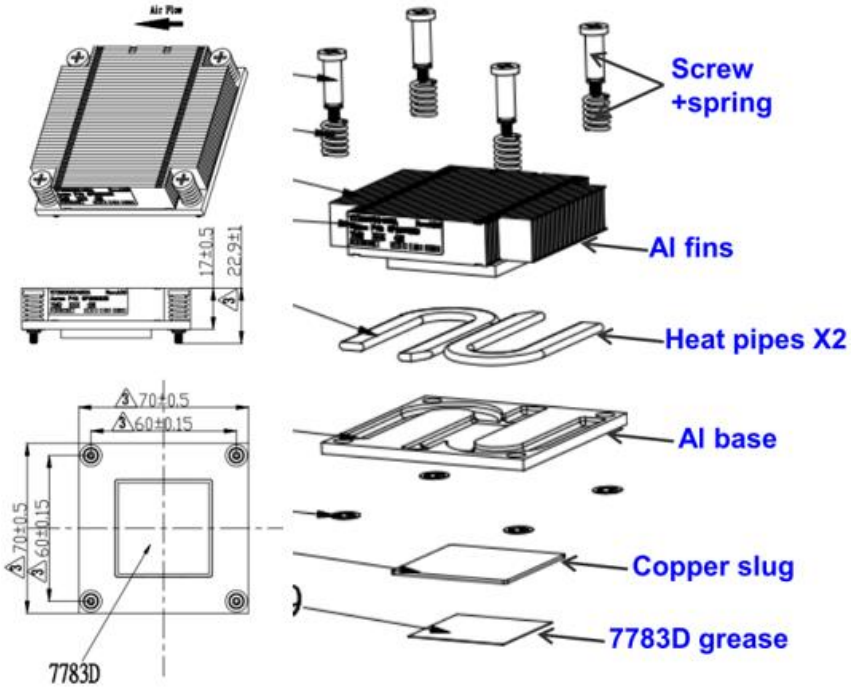


Figure 9-9 CPU heatsink dimension

9.3.3. QSFP56-DD cage

The QSFP56-DD heat sink on top side shown below.

119A00000542A CAGE QSFP-DD H-SINK 1X2P LP-8 90F H19.3 SPRING P-FIT12 TE

TE part number: 2324313-3

Dimension: 38.25 x 81.79 x 19.5 mm

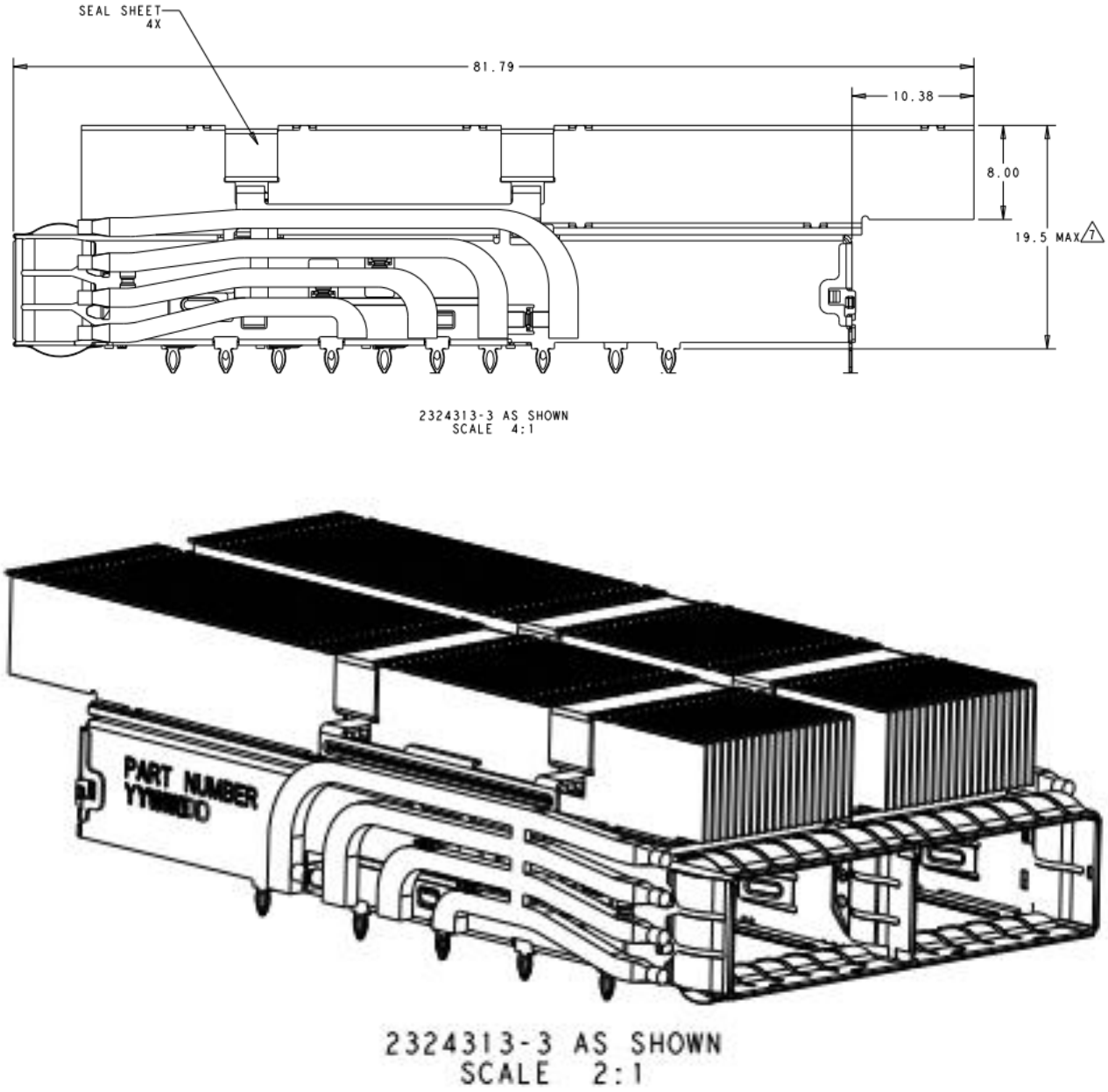


Figure 9-10 Top side QSFP56-DD heatsink dimension

The QSFP56-DD bottom side shown below.

119A00000534A CAGE QSFP-DD H-SINK 1X2P LP-8 90F H15.3 SPRING P-FIT17 TE

TE part number: 2324313-4

Dimension : 38.25 x 95.89 x 15.3 mm

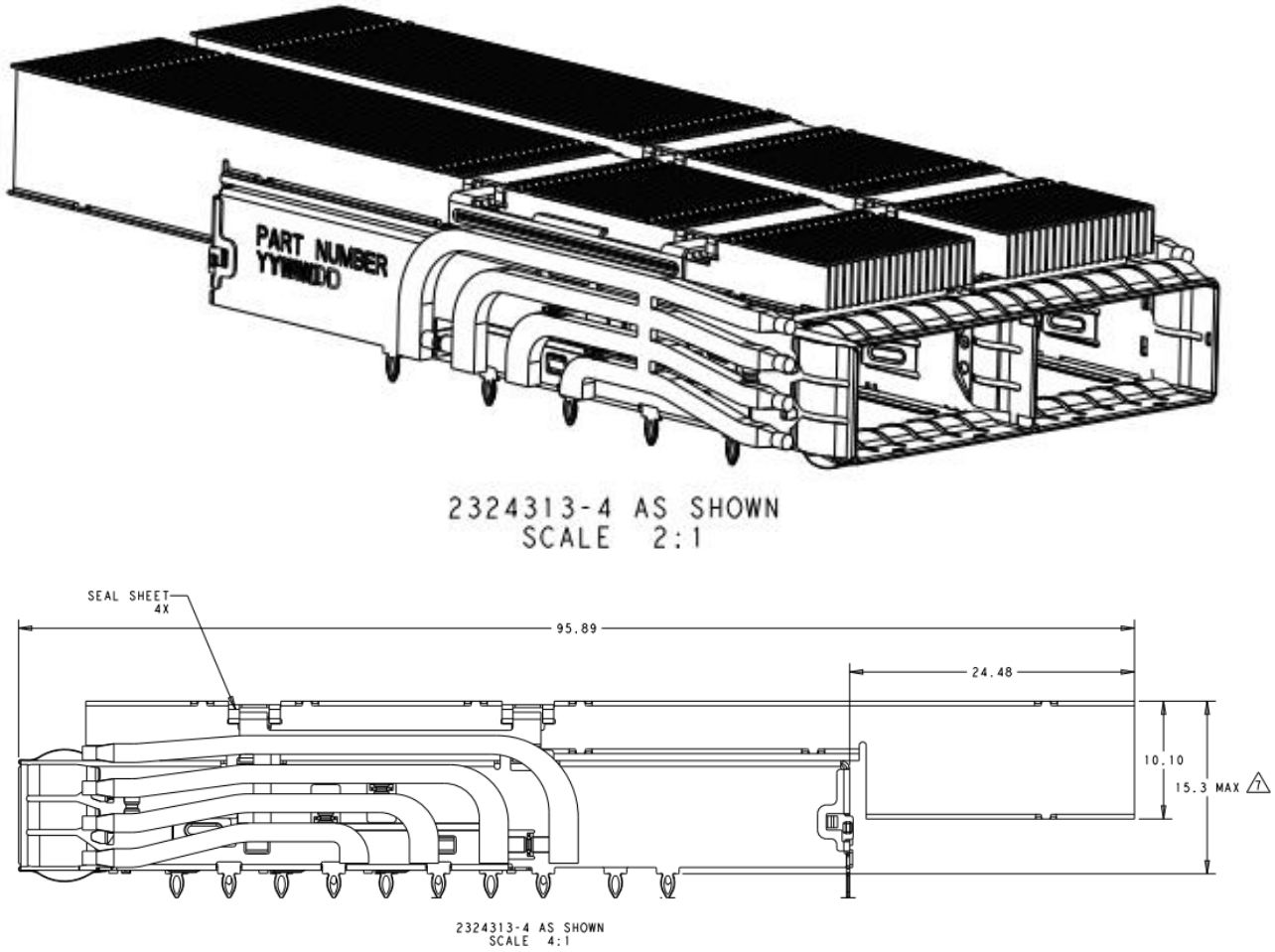
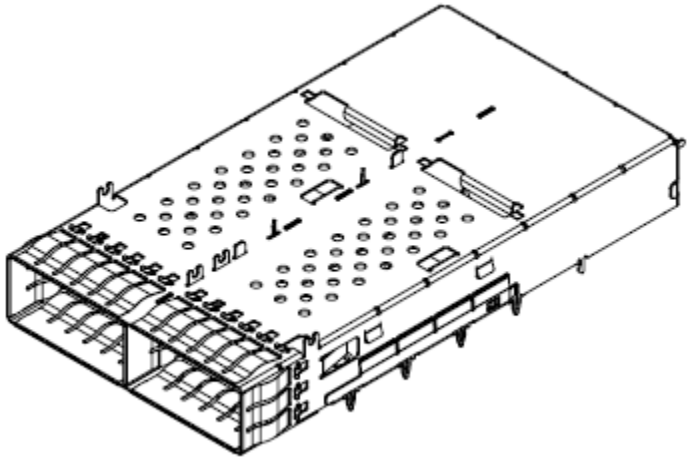
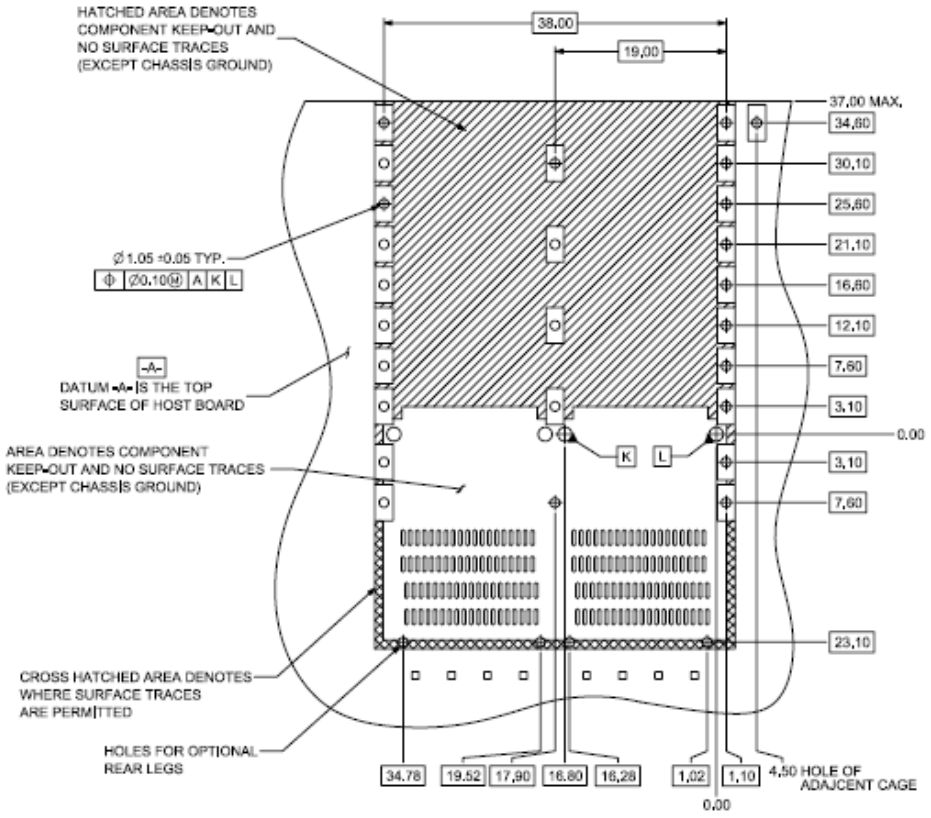


Figure 9-11 Bottom side QSFP56-DD heatsink dimension





10. Misc

10.1. Connector

10.1.1. CPU Board to Board Connector

The board to board connector between CPU board and switch board is SAMTEC BSH-060-01-F-D-RA-WT and BTH-060-01-F-D-RA-WT-K.

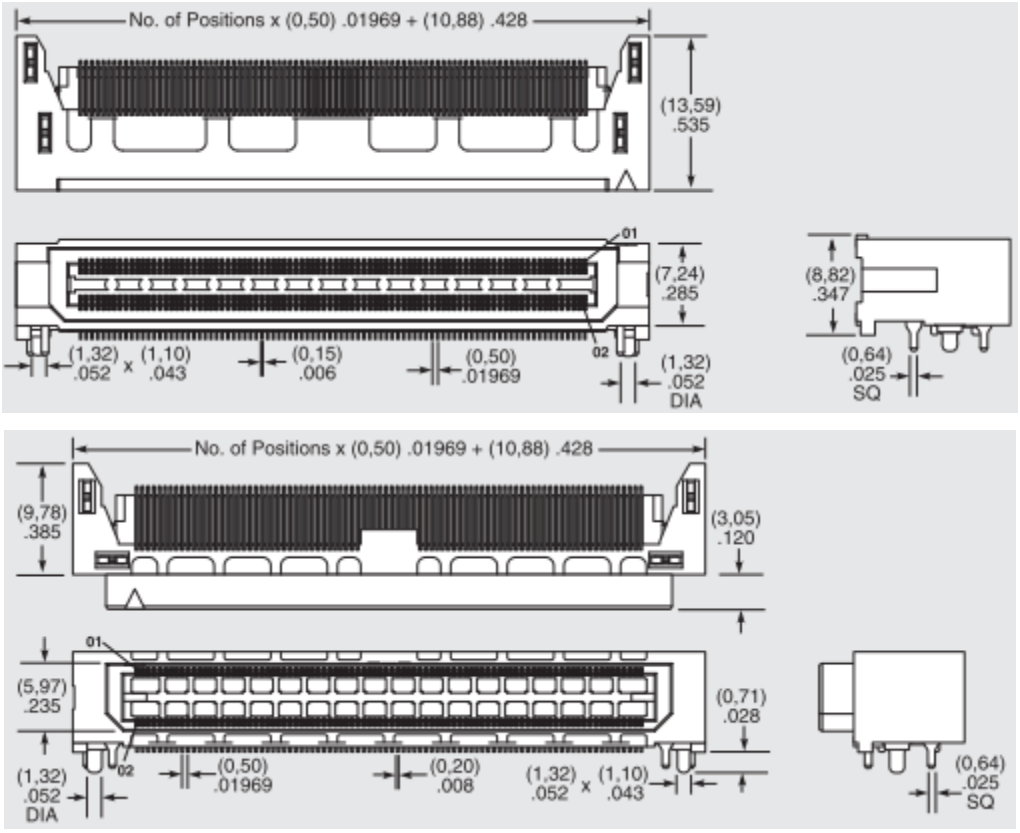


Figure 10-1 CPU to MAC Board to Board Connector Dimension

Table 10-1 CPU Board to Board Connector Pin map

ES7632BT 120 Pin	ES7632BT 120 Pin	General Function	CONNECTOR	PIN #	PIN #		General Function	ES7632BT 120 Pin	ES7632BT 120 Pin
(I)LM75BD_SCLK	IN	TEMP_ANODE	IN/OUT	119	120	OUT	I2C_2_SCL	IN	I2C_1_SCL
(IO)LM75BD_SDA	IN/OUT	TEMP_CATHODE	IN/OUT	117	118	IN	MGMT_RS232_DCD	IN	CPU_PROCHOT
GND		GND	-	115	116	IN/OUT	GPIO		Not Used
CPU_MPHY_SGMII_TX_0_S_P	OUT	MPHY_SGMII_TX_P	OUT	113	114	IN/OUT	I2C_2_SDA	IN/OUT	I2C_1_SDA
CPU_MPHY_SGMII_TX_0_S_N	OUT	MPHY_SGMII_TX_N	OUT	111	112	IN/OUT	GPIO		Not Used
GND		GND	-	109	110	IN	INTERRUPT		GND
MPHY_CPU_SGMII_RX_0_S_N	IN	MPHY_SGMII_RX_N	IN	107	108	IN	INTERRUPT	OUT	PCIE_OOB_TX_P
MPHY_CPU_SGMII_RX_0_S_P	IN	MPHY_SGMII_RX_P	IN	105	106	OUT	MGMT_RS232_DTR	OUT	PCIE_OOB_TX_N
GND		GND	-	103	104	IN/OUT	PROCHOT#		GND
CPU_MPHY_MDC	OUT	GPIO(MPHY_MDC)	OUT	101	102	IN/OUT	GPIO	IN	PCIE_OOB_RX_P
Not Used		INTERRUPT(MPHY)	IN	99	100	OUT	THRMTRIP#	IN	PCIE_OOB_RX_N
CPU_MPHY_MDIO	IN/OUT	GPIO(MPHY_MDIO)	IN/OUT	97	98	IN	INTERRUPT		GND
GND		GND	-	95	96	IN	MGMT_RS232_RXD	IN	UART1_RX
IP_UART0_SOUT	IN	GPIO	IN/OUT	93	94	IN	MGMT_RS232_CTS	IN	UART1_CTS
CPLD23_INT_CPU	IN		IN	91	92	IN	INTERRUPT	IN	CPU_TDI
1PPS_CPU	IN	GPIO	IN/OUT	89	90	OUT	MGMT_RS232_TXD	OUT	UART1_TX
GND		GND	-	87	88	IN	INTERRUPT	IN	MAC_INT_L
GND		GND	-	85	86	-	GND		GND
CPU_XFI_EC_TX_0P	OUT	DIFF_PAIR_TX_0_P	OUT	83	84	IN/OUT	MGMT_USB_N	IN/OUT	USB2_N
CPU_XFI_EC_TX_0N	OUT	DIFF_PAIR_TX_0_N	OUT	81	82	IN/OUT	MGMT_USB_P	IN/OUT	USB2_P
GND		GND	-	79	80	-	GND		GND
GND		GND	-	77	78	OUT	HWIO	OUT	UCD9090_ALERT_L
CPU_XFI_EC_RX_0P	IN	DIFF_PAIR_RX_0_P	IN	75	76	OUT	MGMT_RS232_RTS	OUT	UART1_RTS
CPU_XFI_EC_RX_0N	IN	DIFF_PAIR_RX_0_N	IN	73	74	OUT	HWIO	OUT	RESET_SYS_CPLD
GND		GND	-	71	72	IN/OUT	GPIO	OUT	CPU_TMS
GND		GND	-	69	70	OUT	JTAG_TRST#	OUT	CPU_JTAG_RST
CPU_XFI_EC_RX_2P	IN	DIFF_PAIR_RX_1_P	IN	67	68	OUT	HWIO	IN	P1014_RST
CPU_XFI_EC_RX_2N	IN	DIFF_PAIR_RX_1_N	IN	65	66	IN/OUT	GPIO	OUT	CPU_TDO
GND		GND	-	63	64	IN/OUT	GPIO	OUT	CPU_TCK
GND		GND	-	61	62	IN/OUT	GPIO	OUT	IP_UART0_SIN
CPU_XFI_EC_TX_2P	OUT	DIFF_PAIR_TX_1_P	OUT	59	60	IN/OUT	I2C_0_SDA		Not Used
CPU_XFI_EC_TX_2N	OUT	DIFF_PAIR_TX_1_N	OUT	57	58	OUT	I2C_0_SCL		Not Used
GND		GND	-	55	56	IN	INTERRUPT	IN	SYS_CPLD_INT_CPU
GND		GND	-	53	54	OUT	HWIO	IN	USB1_PWRFAULT
CPU_PEX_PCIEA_TX_0_P	OUT	PCIE_TX_2_P	OUT	51	52	IN	RESET_MODULE_REQ#	IN	Manu_RST
CPU_PEX_PCIEA_TX_0_N	OUT	PCIE_TX_2_N	OUT	49	50	OUT	I2C_1_SCL	OUT	I2C_0_SCL
GND		GND	-	47	48	IN/OUT	I2C_1_SDA	IN/OUT	I2C_0_SDA
GND		GND	-	45	46	OUT	RESET_SYS_REQ#	OUT	RESET_MAC
CPU_PEX_PCIEA_TX_1_N	OUT	PCIE_TX_3_P	OUT	43	44	IN	SYS_PWR_GOOD	OUT	CPU_THERMALTRIP
CPU_PEX_PCIEA_TX_1_P	OUT	PCIE_TX_3_N	OUT	41	42	OUT	HWIO	OUT	USB1_VBUS
GND		GND	-	39	40	-	GND		GND
GND		GND	-	37	38	-	GND		GND
PEX_CPU_PCIEA_RX_0_N	IN	PCIE_RX_2_P	IN	35	36	OUT	PCIE_TX_0_P	OUT	CPU_PEX_PCIEB_TX_0_P
PEX_CPU_PCIEA_RX_0_P	IN	PCIE_RX_2_N	IN	33	34	OUT	PCIE_TX_0_N	OUT	CPU_PEX_PCIEB_TX_0_N
GND		GND	-	31	32	-	GND		GND
GND		GND	-	29	30	-	GND		GND
PEX_CPU_PCIEA_RX_1_N	IN	PCIE_RX_3_P	IN	27	28	IN	PCIE_RX_0_P	IN	PEX_CPU_PCIEB_RX_0_P
PEX_CPU_PCIEA_RX_1_P	IN	PCIE_RX_3_N	IN	25	26	IN	PCIE_RX_0_N	IN	PEX_CPU_PCIEB_RX_0_N
GND		GND	-	23	24	-	GND		GND
GND		GND	-	21	22	-	GND		GND
CPU_PEX_PCIEB_TX_1_N	OUT	PCIE_TX_1_P	OUT	19	20	IN	PCIE_RX_1_P	IN	PEX_CPU_PCIEB_RX_1_P
CPU_PEX_PCIEB_TX_1_P	OUT	PCIE_TX_1_N	OUT	17	18	IN	PCIE_RX_1_N	IN	PEX_CPU_PCIEB_RX_1_N
GND		GND	-	15	16	-	GND		GND
GND		GND	-	13	14	-	GND		GND
GND		GND	-	11	12	-	GND		GND
VCC12		12VDC	-	9	10	-	12VDC		VCC12
VCC12		12VDC	-	7	8	-	12VDC		VCC12
VCC5P0		5VDC	-	5	6	-	12VDC		VCC12
VCC5P0		5VDC	-	3	4	-	12VDC		VCC12
VCC5P0		5VDC	-	1	2	-	12VDC		VCC12

10.1.2. PSU Connector

9392-D0000-030-P832K-R7-B4SS24P04P1xB7Dx-P--1070130提供.pdf

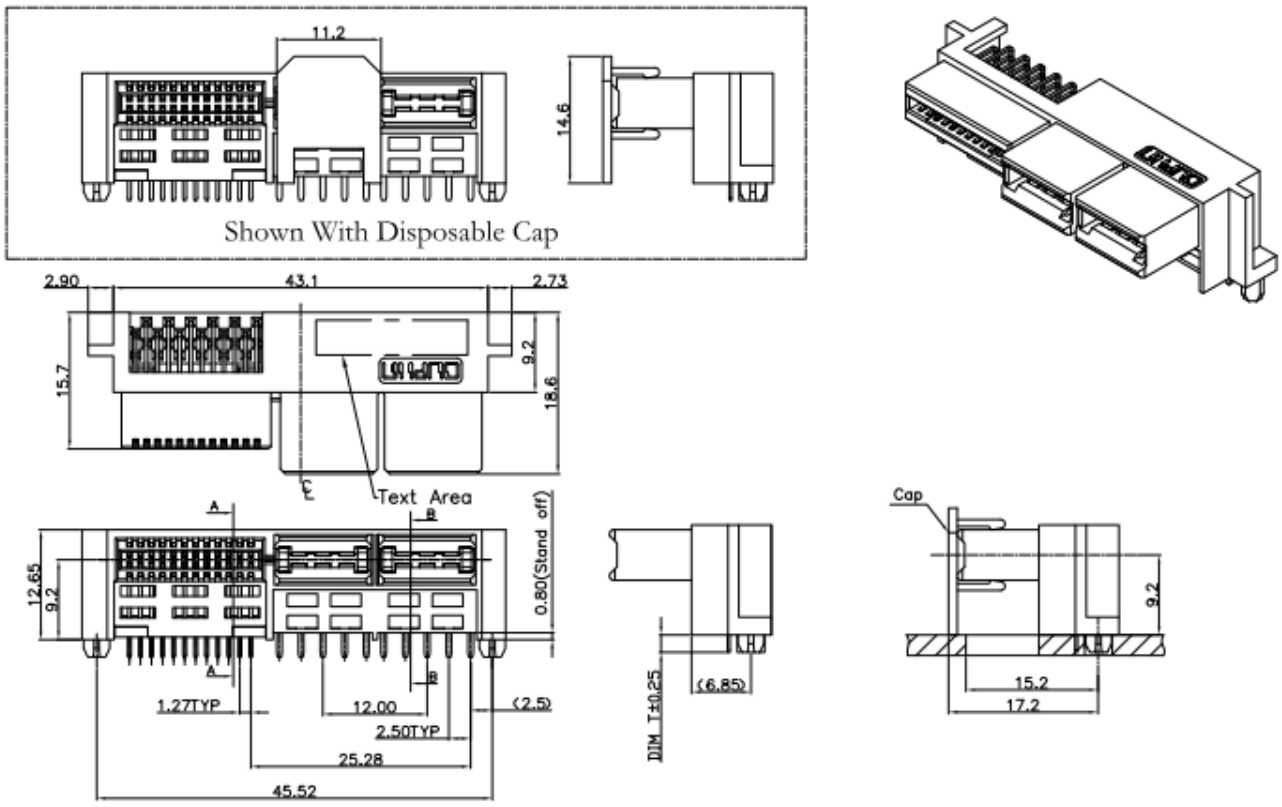


Figure 10-2 1300W PSU connector

10.1.3. Bridge / Fan board Connector

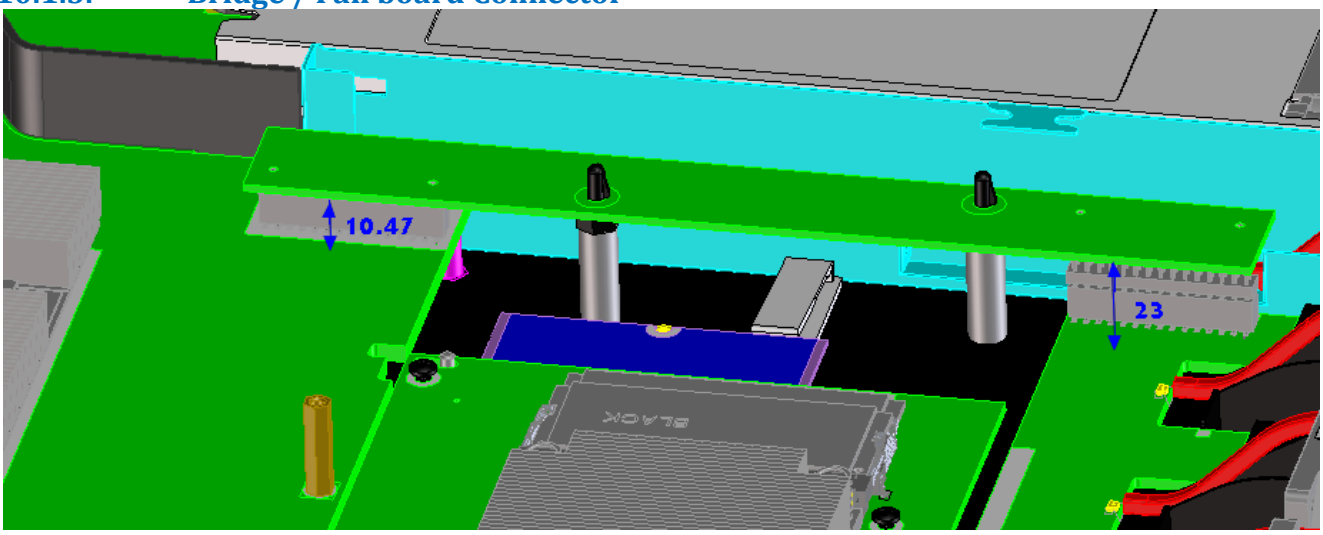


Figure 10-3 Bridge board match height drawing

Table 10-2 Bridge & Fan board Connectors

AS9700-32X			
SKU	**Vendor part number**	**Current rating**	**Match Height**
MB	**SSM-115-S-DV-A-K-TR**	**3A**	
FAN Board	**DH32-FB030RL54N-1**		
Bridge board (Mainboard side)	**DH109-MLB030RL54N-3**	**3A**	**10.47mm**
Bridge board (Fan board side)	**DH61-MLB030RL54N-7**	**3A**	**23mm**

Software Support

The AS9700-32X supports a base software package composed of the following components:

BIOS support

The AS9700-32X Supports AMI AptioV BIOS version A01 or greater with the x86 CPU module

ONIE

See https://github.com/opencomputeproject/onie/tree/master/machine/accton for the latest supported version

Open Network Linux

See http://opennetlinux.org/ for latest supported version

Specifications

Power Consumption

The total estimated system power consumption of the AS9700-32X is ~1200 Watts. This is based upon worst case power assumptions for traffic, optics used, and environmental conditions. Typical power consumption will be less.

Environmental

- 0 to 40 Degrees C operating range
- -40 to 40 Degrees C storage temperate range
- Humidity 5% to 95% non-condensing (operational and storage)
- Vibration – IEC 68-2-36, IEC 68-2-6
- Shock – IEC 68-2-29
- Acoustic Noise Level – Under 60dB in 40 degree C
- Altitude - 15,000 (4572 meters) tested operational altitude

Safety

- UL/ Canada
- CB (Issued by TUV/RH)
- China CCC

Electromagnetic Compatibility

- CE
- EN55022 Class A
- EN55024
- EN61000-3-2
- EN61000-3-3
- FCC Title 47, Part 15, Subpart B Class A
- VCCI Class A
- CCC

ROHS

Restriction of Hazardous Substances (6/6)

Compliance with Environmental procedure 020499-00 primarily focused on Restriction of Hazardous Substances (ROHS Directive 2002/95/EC) and Waste and Electrical and Electronic Equipment (WEEE